Lab manual – PCB and Prototyping Workshop [4048 Rev 2021]

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Index

VISION AND MISSION

Government Polytechnic College, Perumbavoor Vision and Mission
Vision To excel as a centre of skill education moulding professionals who sincerely strive for the betterment of society.
Mission • To impart state of the art knowledge and skill to the graduate and moulding them to be competent, committed and responsible for the well being of society. • To apply technology in the traditional skills, thereby enhancing the living standard of the community

Department of Electronics & Communication Engineering
Vision To excel as a centre of skill education in Electronics and Communication Engineering, moulding professionals who sincerely strive for the betterment of themselves and society.
Mission • To impart state of the art knowledge, skill and attitude to the students and contributing to their sustainable development. • To merge technologies in the field of Electronics and Communication Engineering with occupational skills, thereby improving quality of living.

Exp: 1	PEO, PO and PSOs of the Program	Date :

Program Educational Outcome (PEOs)

PEO1: Secure successful careers in manufacturing, testing, maintenance, development and marketing in Electronics and Communication Engineering.

PEO2: Acquire knowledge and competency in the domain to develop innovative, cost effective and socially acceptable solutions to engineering problems in a multi disciplinary work environment.

PEO3: Develop strong fundamental knowledge that prepares them for professional careers/higher studies with attitude for lifelong learning.

PEO4: Instill the attitude to be sensitive to ethical, societal and environmental issues while pursuing their professional duties.

PEO5: Possess leadership qualities and be effective communicator to work efficiently with diverse teams, promote and practice appropriate ethical practices.

Program Outcomes (POs)

PO1: Basic and Discipline specific knowledge: Apply knowledge of basic mathematics, science and engineering fundamentals and engineering specialization to solve the engineering problems.

PO2: Problem analysis: Identify and analyse well-defined engineering problems using codified standard methods.

PO3: Design/ development of solutions: Design solutions for well-defined technical problems and assist with the design of systems components or processes to meet specified needs.

PO4: Engineering Tools, Experimentation and Testing: Apply modern engineering tools and appropriate technique to conduct standard tests and measurements.

PO5: Engineering practices for society, sustainability and environment: Apply appropriate technology in context of society, sustainability, environment and ethical practices.

PO6: Project Management: Use engineering management principles individually, as a team member or a leader to manage projects and effectively communicate about well-defined engineering activities.

PO7: Life-long learning: Ability to analyse individual needs and engage in updating in the context of technological changes**.**

Program Specific Outcome (PSO):

PSO1: Specialization knowledge: Apply concepts and knowledge in the field of semiconductor devices, communication and networking technologies, embedded systems.

PSO2: Professional growth: Generate ideas from the knowledge of engineering specialization leading to professional growth.

PSO3: Entrepreneurship: Apply knowledge and understanding of engineering principles to initiate entrepreneurship ventures.

Exp: 2	Safety procedures	Date :

SAFETY PROCEDURES

Problem Statement:

The safety instructions are presented to the attention of the students as a mean of preventing accidents while performing experiments and activities in the communication lab of the department.The purpose is to draw attention to the risks involved in lab activities to prevent human suffering and damage to equipment.

Safety in the laboratory:

Working in the lab is not allowed without following electricity precautions displayed.

No individual work is allowed in the lab.

Laboratory in charge is responsible for the arrangements of your lab activities; Listen carefully to his/her instructions and follow them.

To do and not to do:

Inform the lab in charge about dangerous conditions and faults in the lab or nearby environment.

Do not do any action that may harm people or equipments in the lab.

Do not misuse any of the tools or instrumentsbelong to the lab.

Strict discipline should be maintained in the laboratory.

Turn off cell phones before entering the lab.

At the end and beginning of laboratory, follow 5S procedures and leave the work table clean and tidy.

Electrical Safety:

Consult Electrical Engineering section available in the campus for electrical safety queries.

The lab equipment is powered from electrical sockets installed on the tables. Do not use equipment that is powered from a damaged socket.

Do not use equipment that is powered from flexible cable with damaged insulation or if it’s plug is not assembled properly.

Do not repair or disassemble electrical equipment including replacement of fuses installed in the equipment.

Do not open the main fuse box, unless it is an emergency and you need to switch off main circuit breaker.

Emergency Switches:

The laboratory has circuit breakers, which is located in the main panel. Identify the place.
In an emergency condition,switch off circuit breakers immediately.

Result

Familiarization of safety precautions performed.

	Signature of Lab in charge	Remarks
Readiness to do experiment		
Completion of Experiment		

Exp: 3	Handling ESD	Date :

HANDLING ELECTROSTATIC DISCHARGE (ESD)

Problem Statement:

Familiarize ESD handling procedures in the laboratory

Theory

In handling electronic devices, datasheets cautions about ESD (Electrostatic Discharge) precautions. These devices are prone to damage because of electrostatic charges made by human body. These charges may be up to 4000 volts and cause damage without being noticed. It is recommended to follow ESD precautions on handling of these devices.

Points for the elimination of ESD damage to electronic components

1. Make sure you have a reliable ground point available near the table.
2. Do not wear clothing which generates static electric charges every time you move.
3. Do not handle static generating objects while working on electronics.
4. Store all chips and other components in appropriate anti-static containers.
5. Keep all ESD sensitive components and spares in anti-static envelopes for storage.
6. Be sure to turn off the power and remove the power plug from all equipment before working repairing or assembling.
7. Do not plug in or remove equipments while the power is on.

Result

Familiarization of ESD protection procedures performed.

	Signature of Lab in charge	Remarks
Readiness to do experiment		
Completion of Experiment		

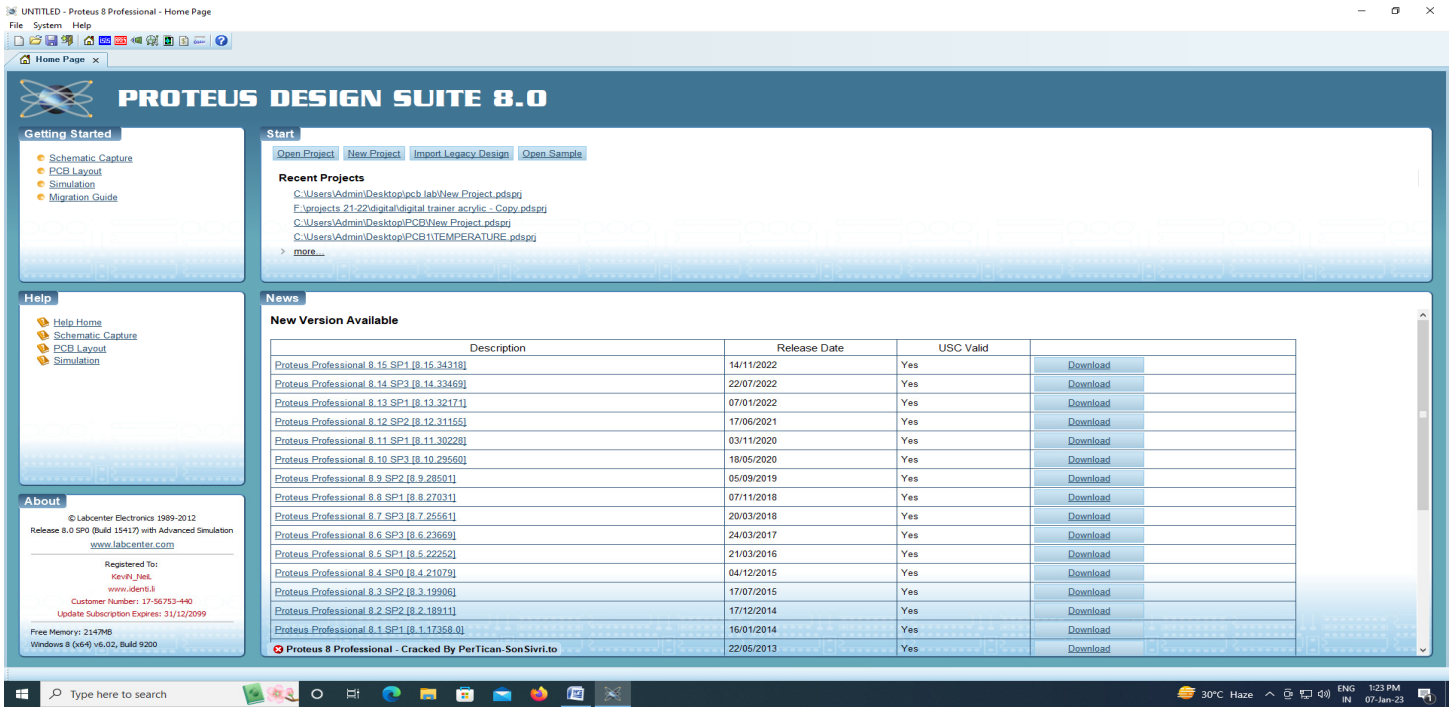
Exp: 4	Creating Proteus Project	Date :

Time : 30 minutes

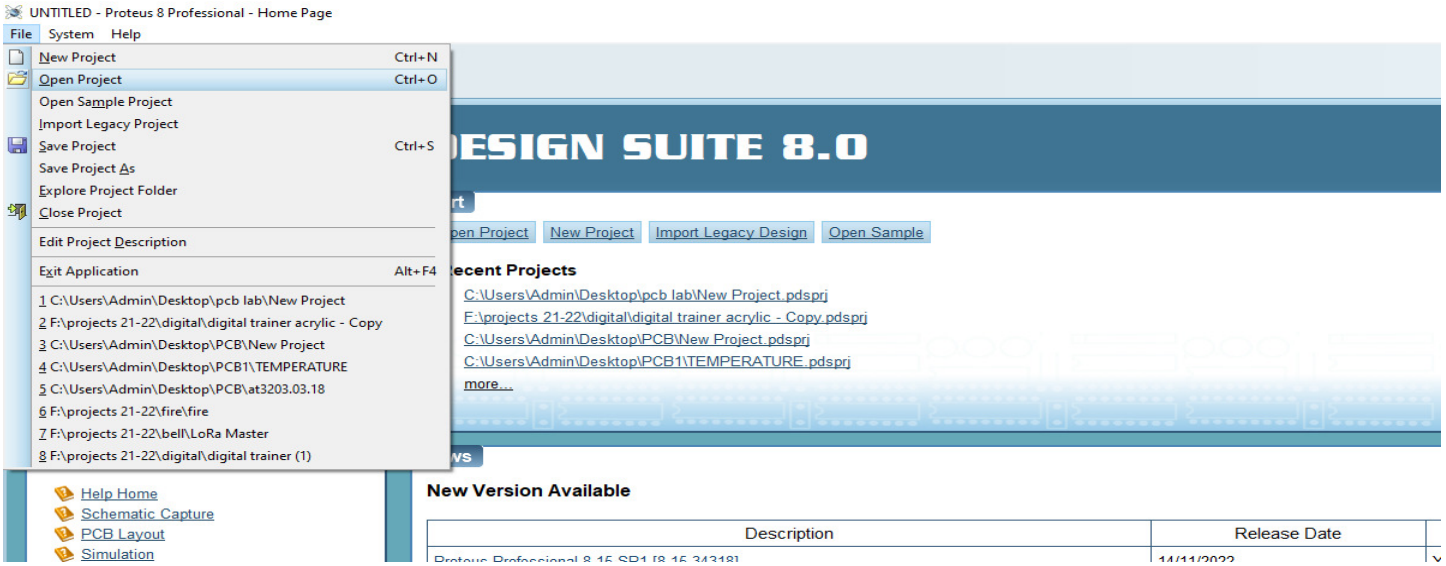
Problem Statement: Create Proteus project for Schematic capture, single or Double sided PCB.

Procedure:

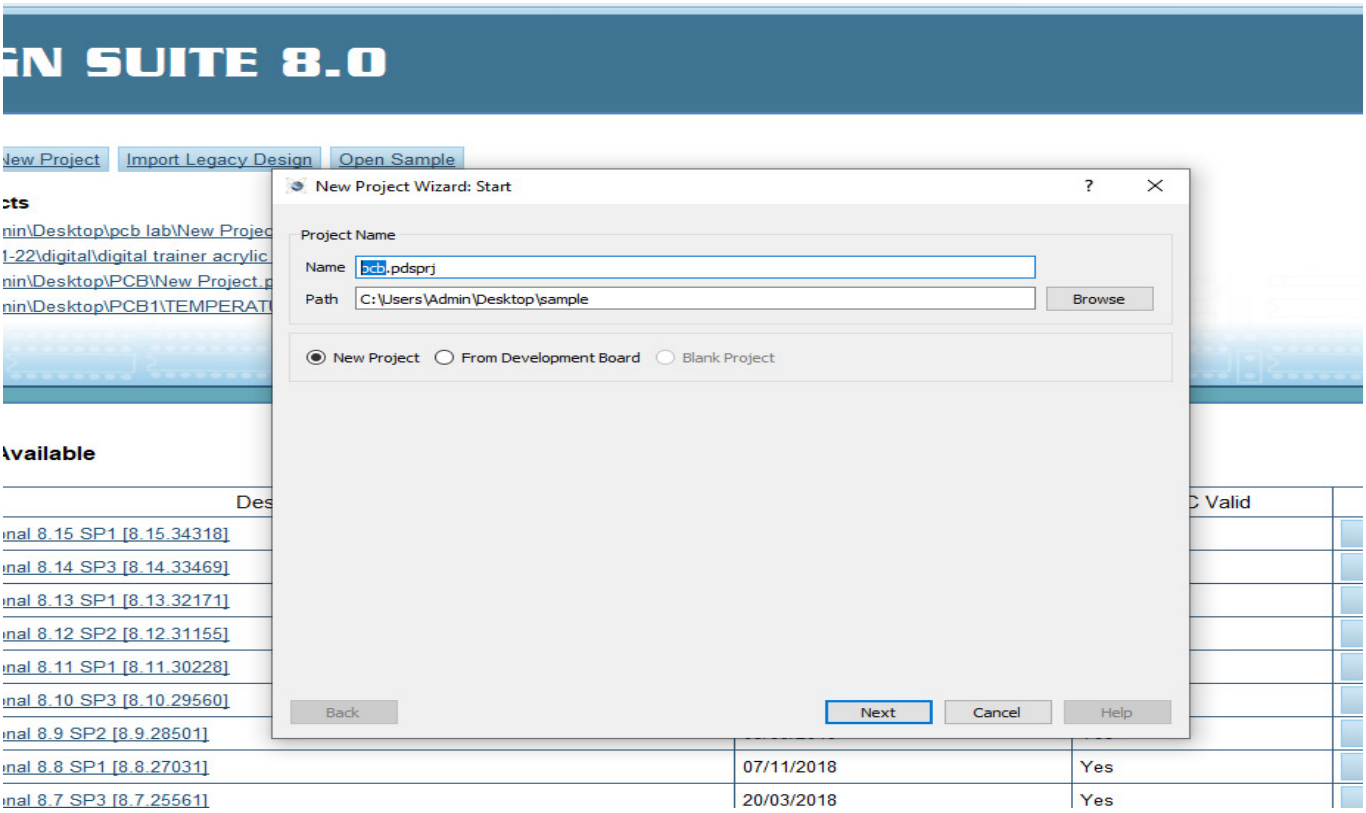
1. **Do one time installation of Proteus 8**



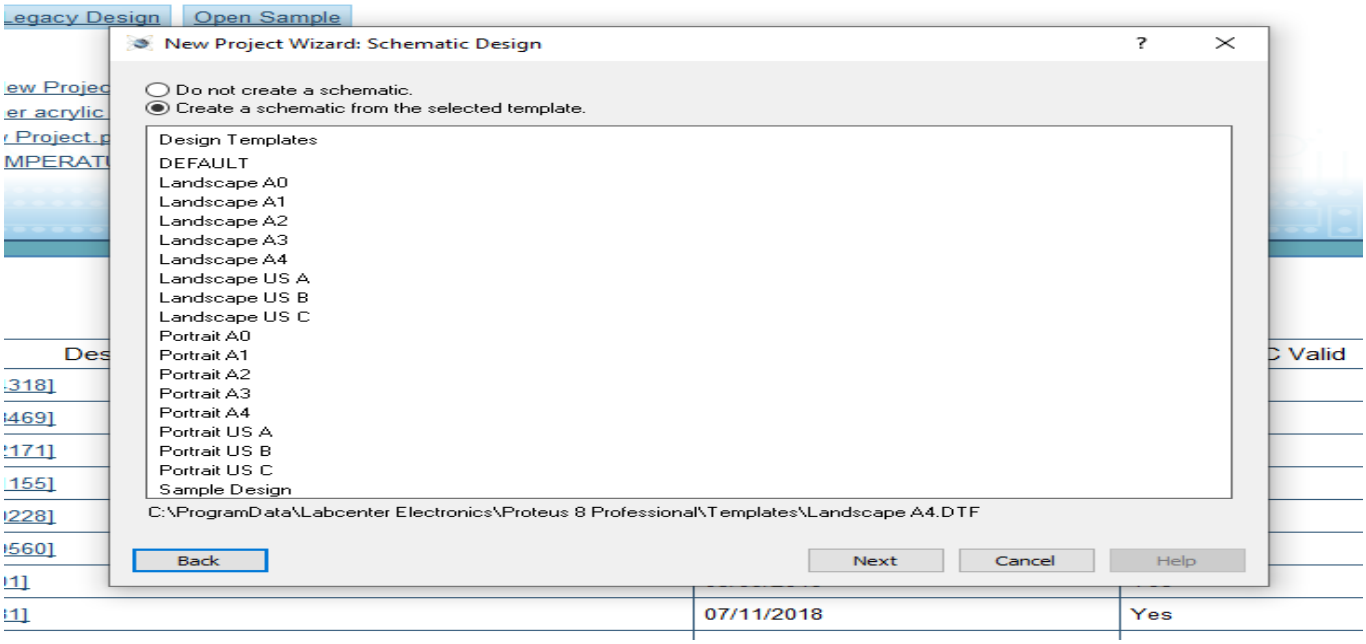
2. **From file menu select New Project**



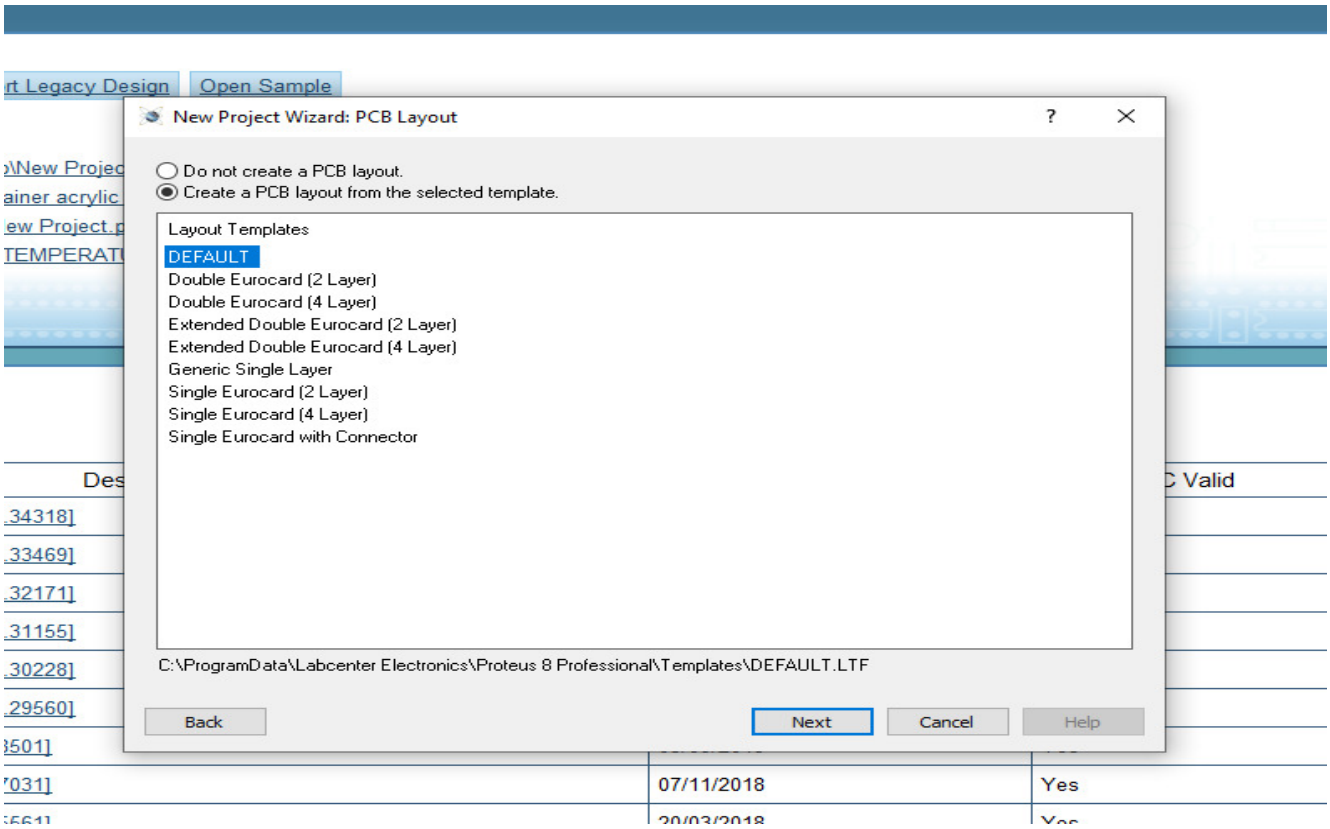
3. **Browse a suitable folder and provide file name**



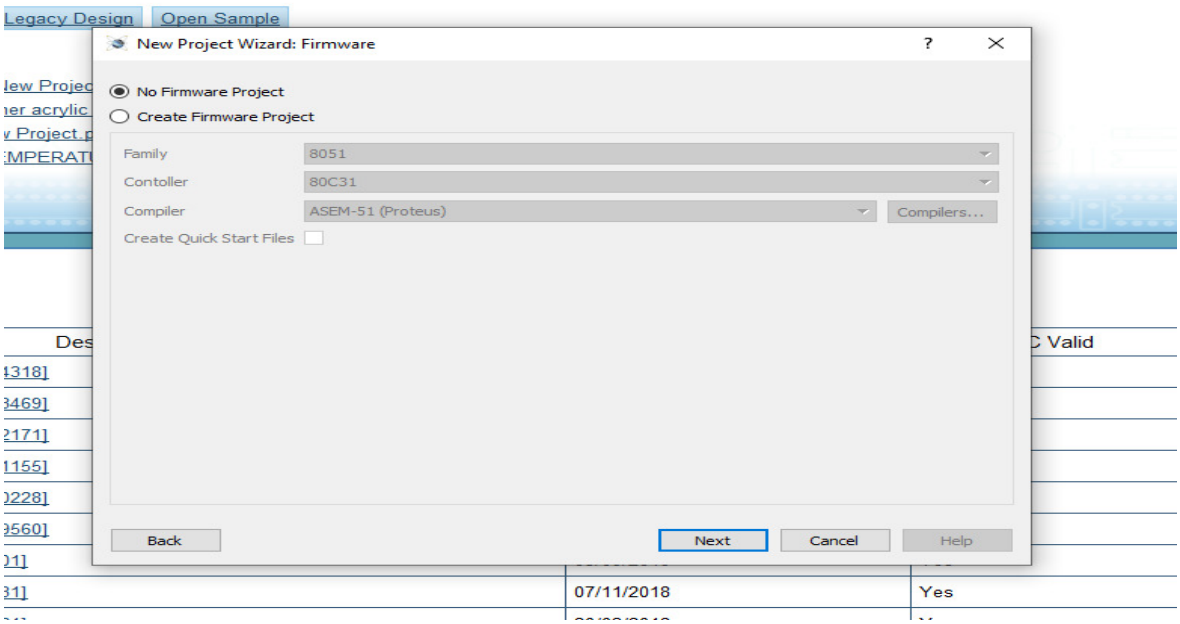
4. **Tick Create a schematic from the selected template and click next**



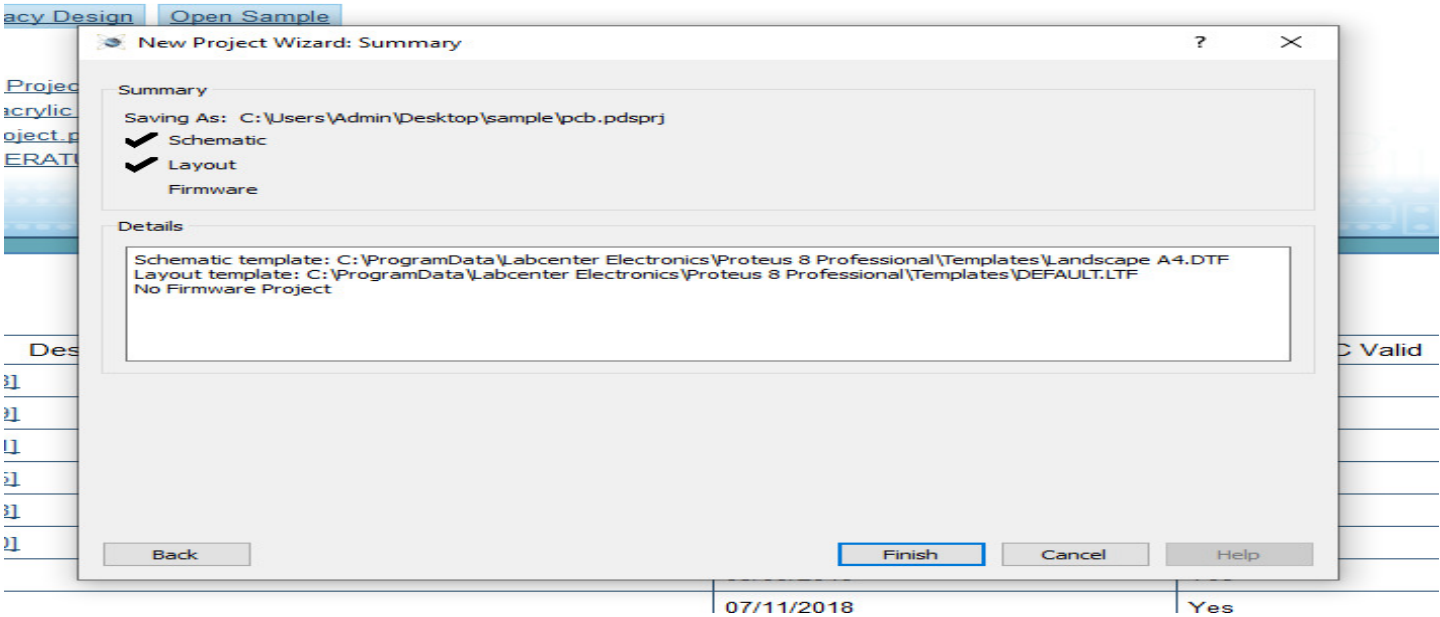
5. **Tick Create a pcb lay out from the selected template and click next. Default is for double sided PCB and Deneric Single layer for single layer PCB.**



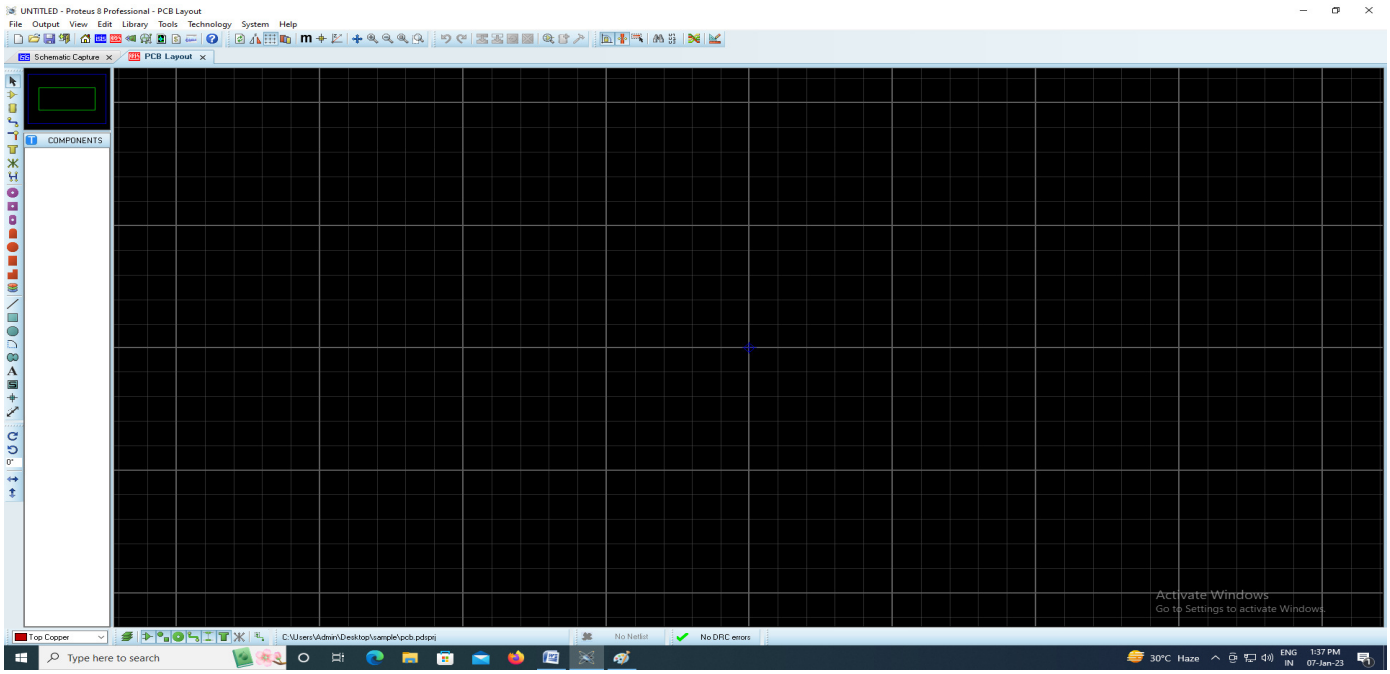
6. **Click Next for no simulation**



7. **Click on finish**



8. **The Project is ready**



Result

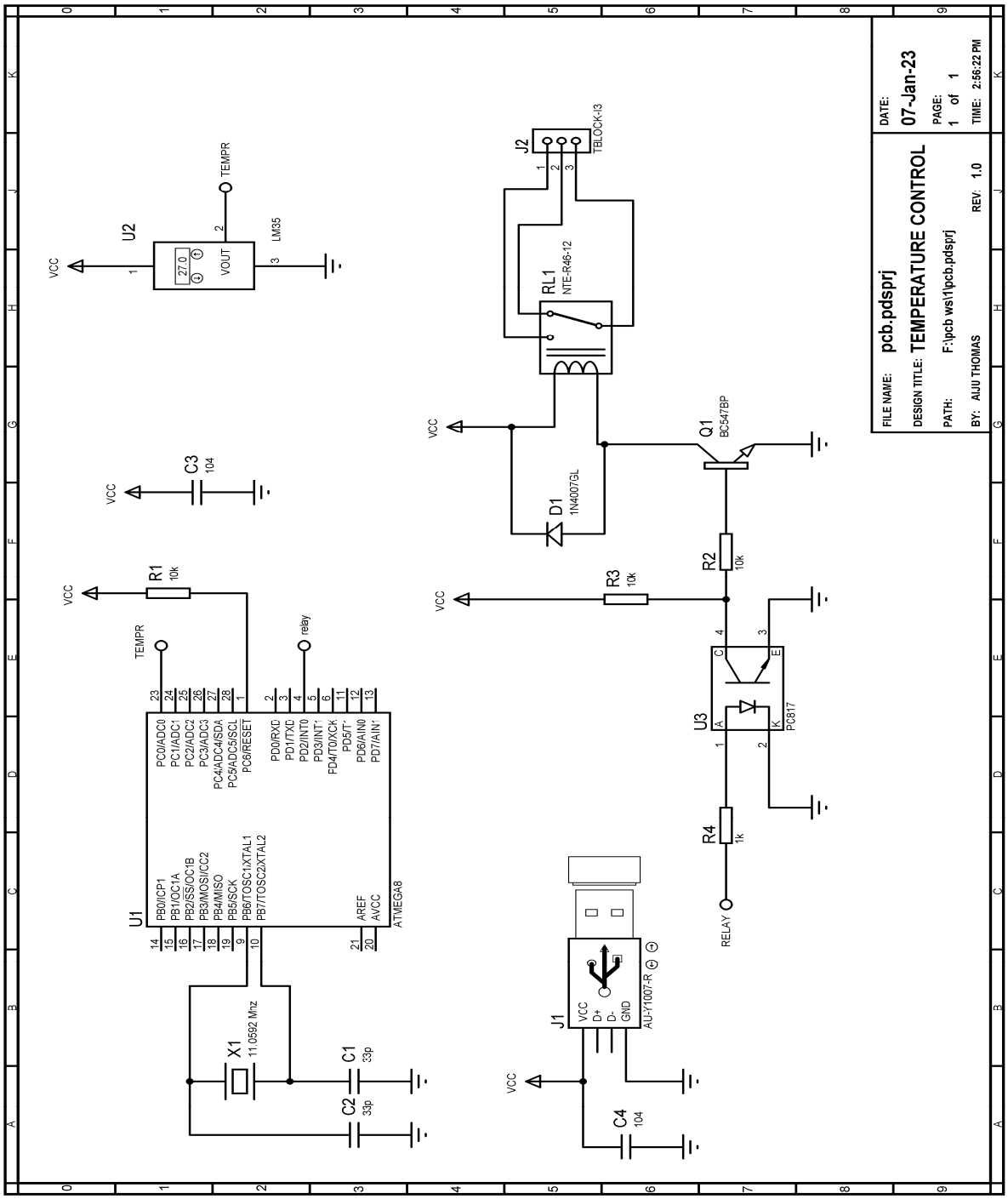
Proteus Project is created for schematic capture and for the required single or double sided PCB

Lab in charge	**Signature of the lab incharge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

Exp: 5	Prepare Schematic capture for the given circuit	Date :

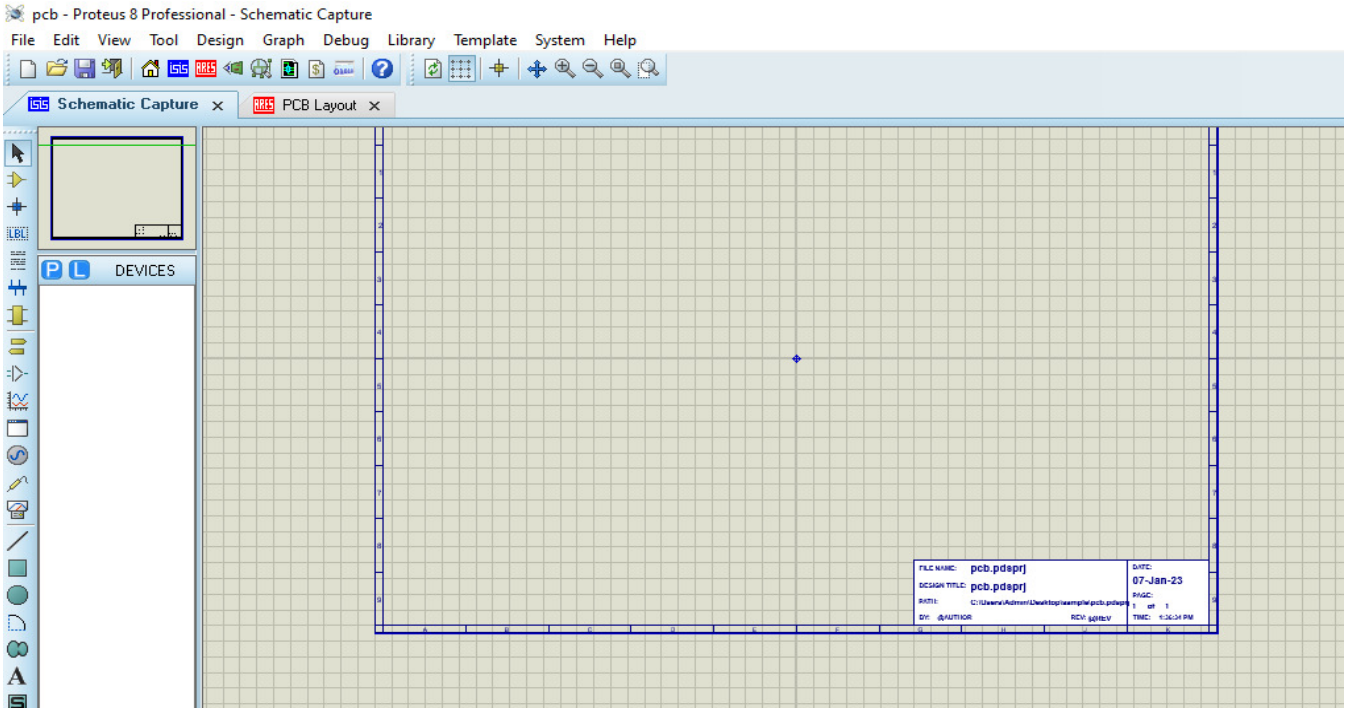
Time : 2 hours

Problem Statement: Prepare Schematic capture for the given microcontroller circuit

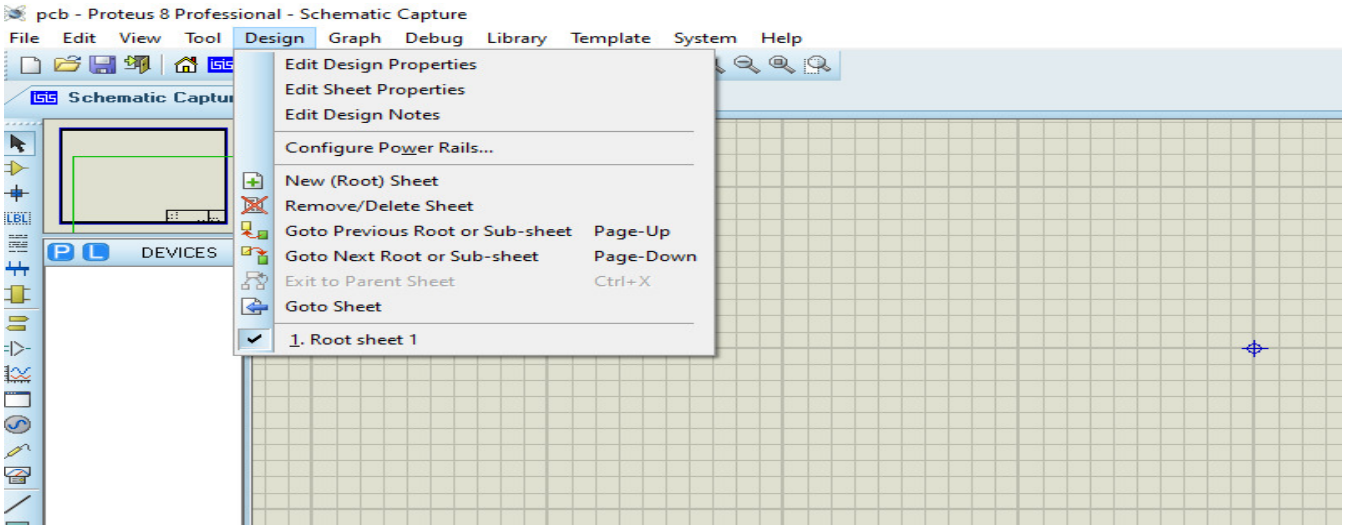


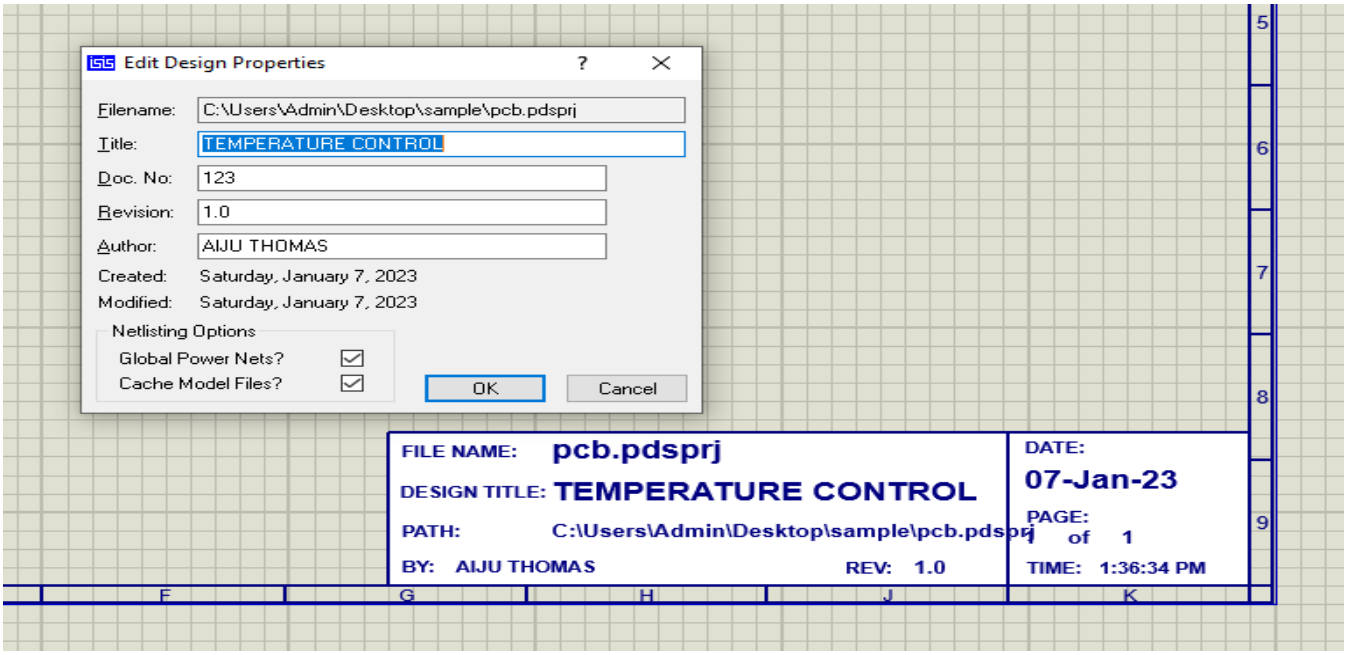
Procedure:

1. **Create suitable project and select schematic capture tab**



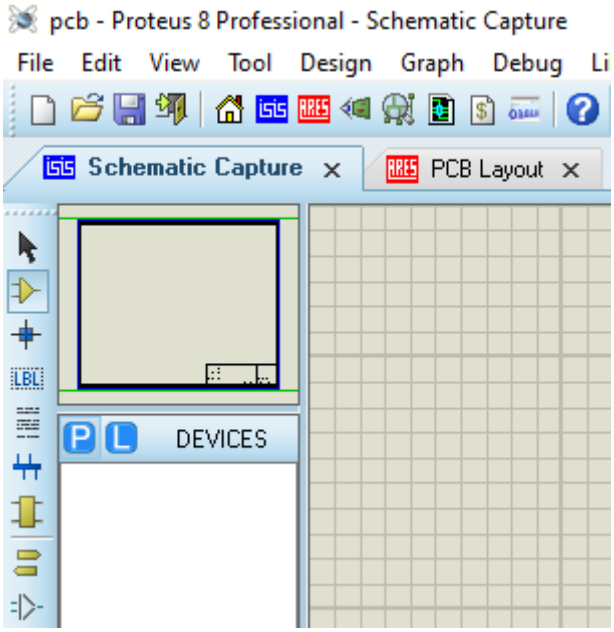
2. **Edit design properties and update the name plate.**



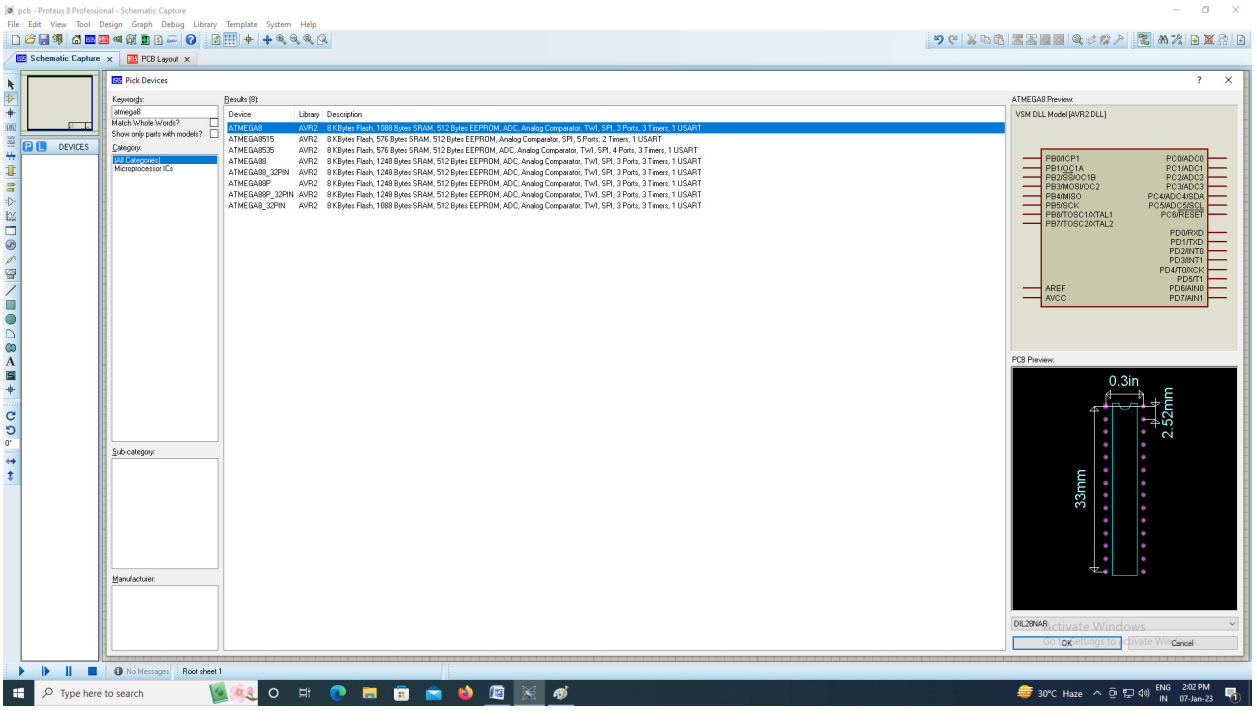


3. **Click OK. Use external mouse point to the specific place in the screen and scroll for zoom in and out. Make sure that you save the project inbetween.**

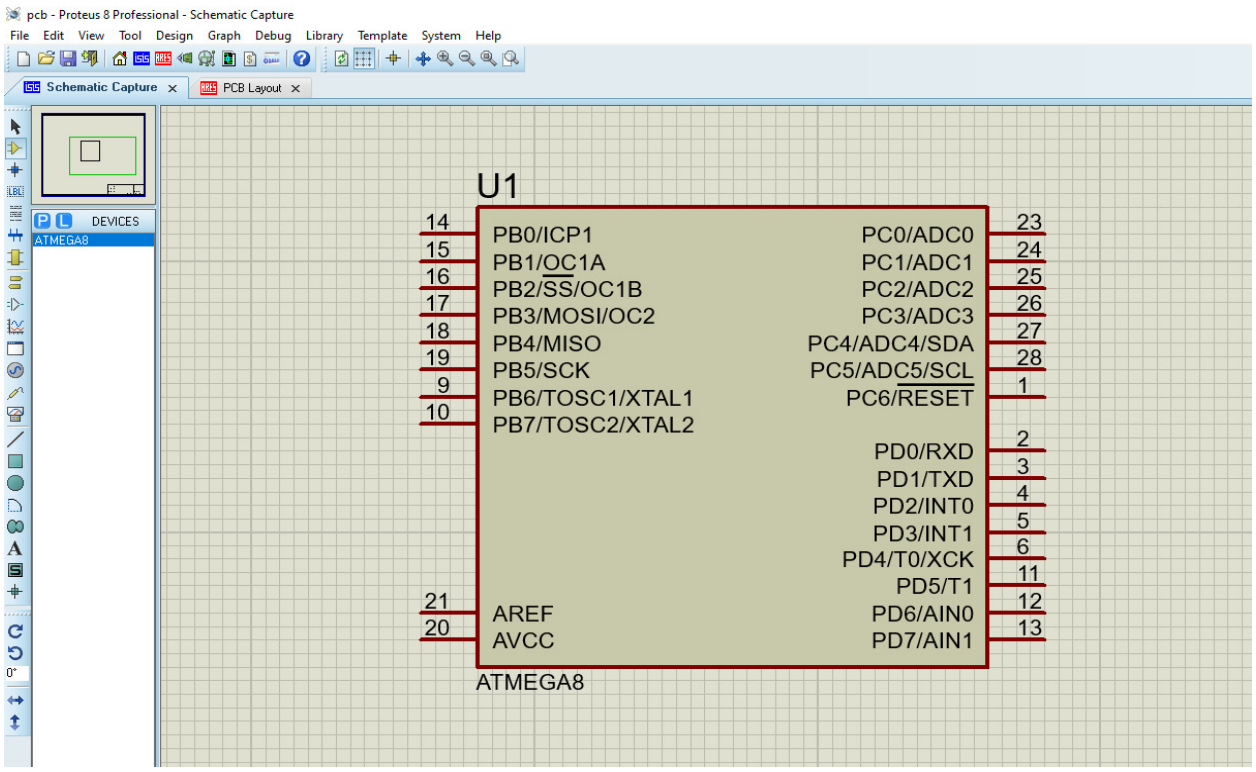
4. **To select a component click on op-amp symbol and click P**



5. **Type the required component on the Keywords and select the component based on the required foot print.**

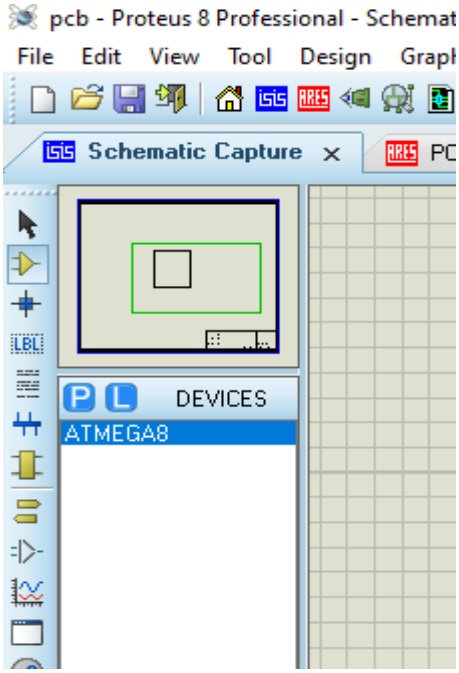


6. **Click OK and click on the schematic capture window where you need to place the component.**

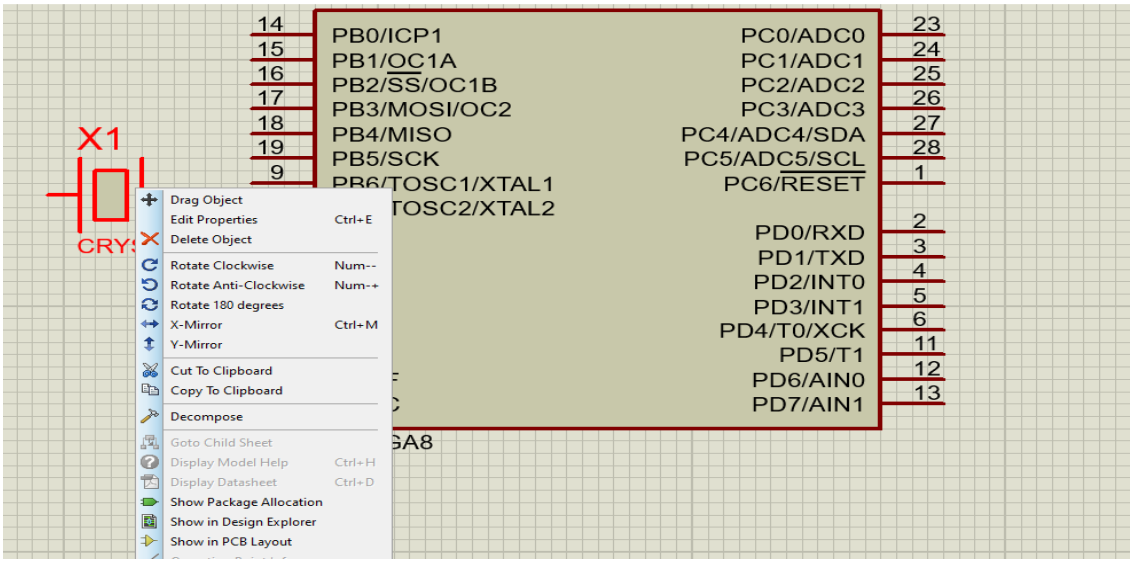


7. **You will find the**

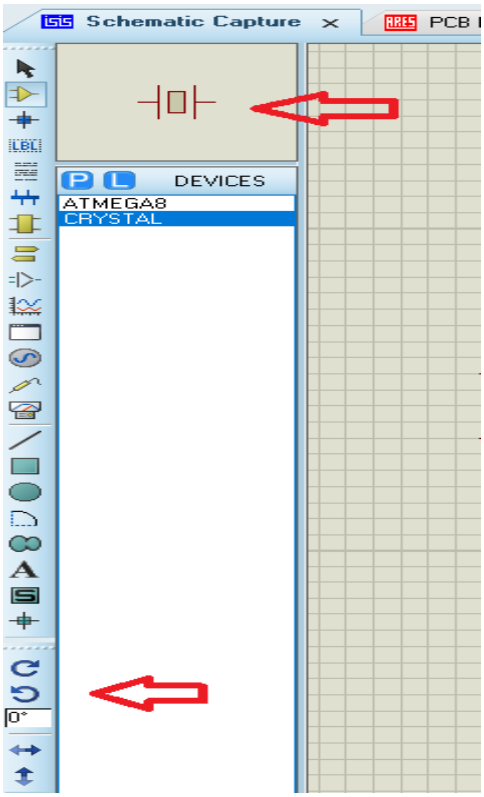
selected component on Devices. For repeated use of the same component, click on the list in devices and place on the capture.



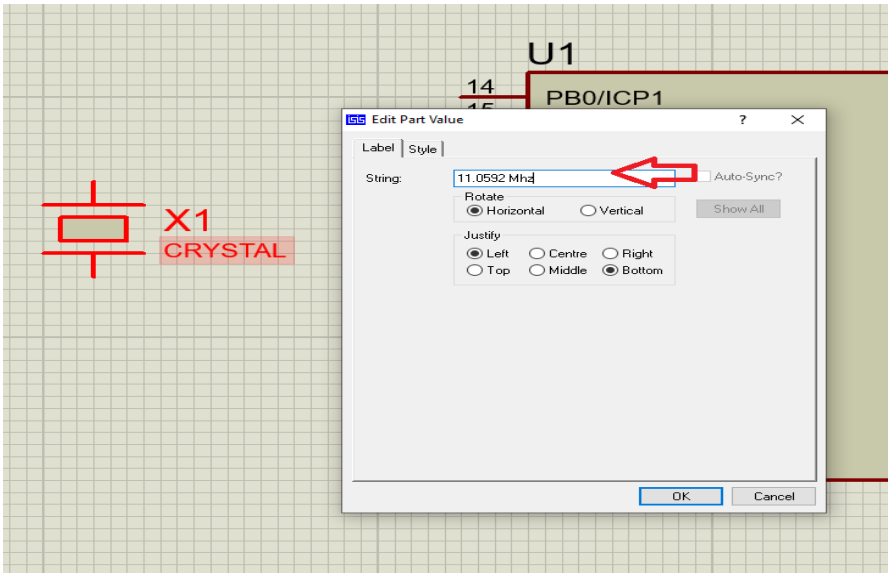
8. **Repeat the procedure for more components. To rotate a component, either place the component on capture, right slick and select rotate**



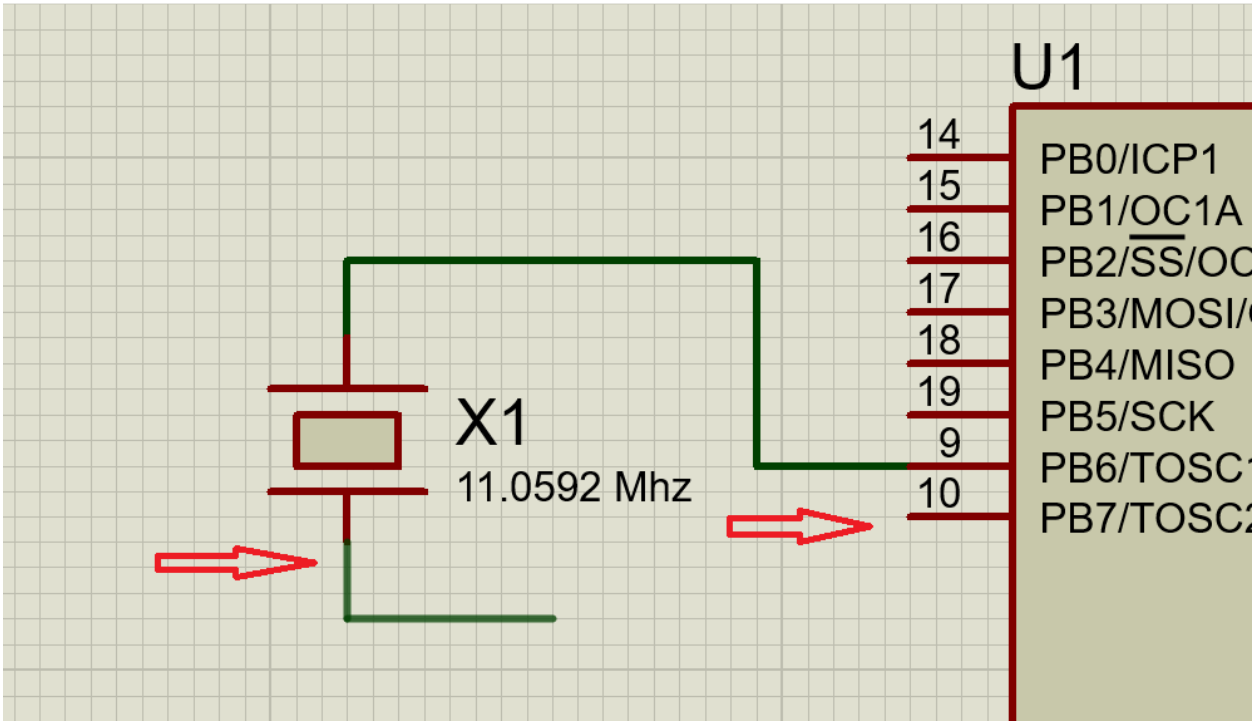
or rotate using the shown tool before placing



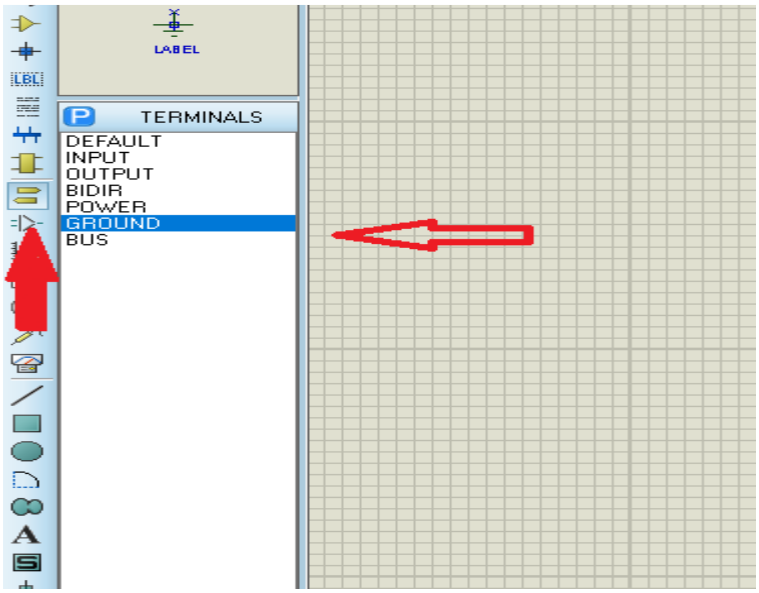
9. **To edit a component value, double click on the component and edit the value**



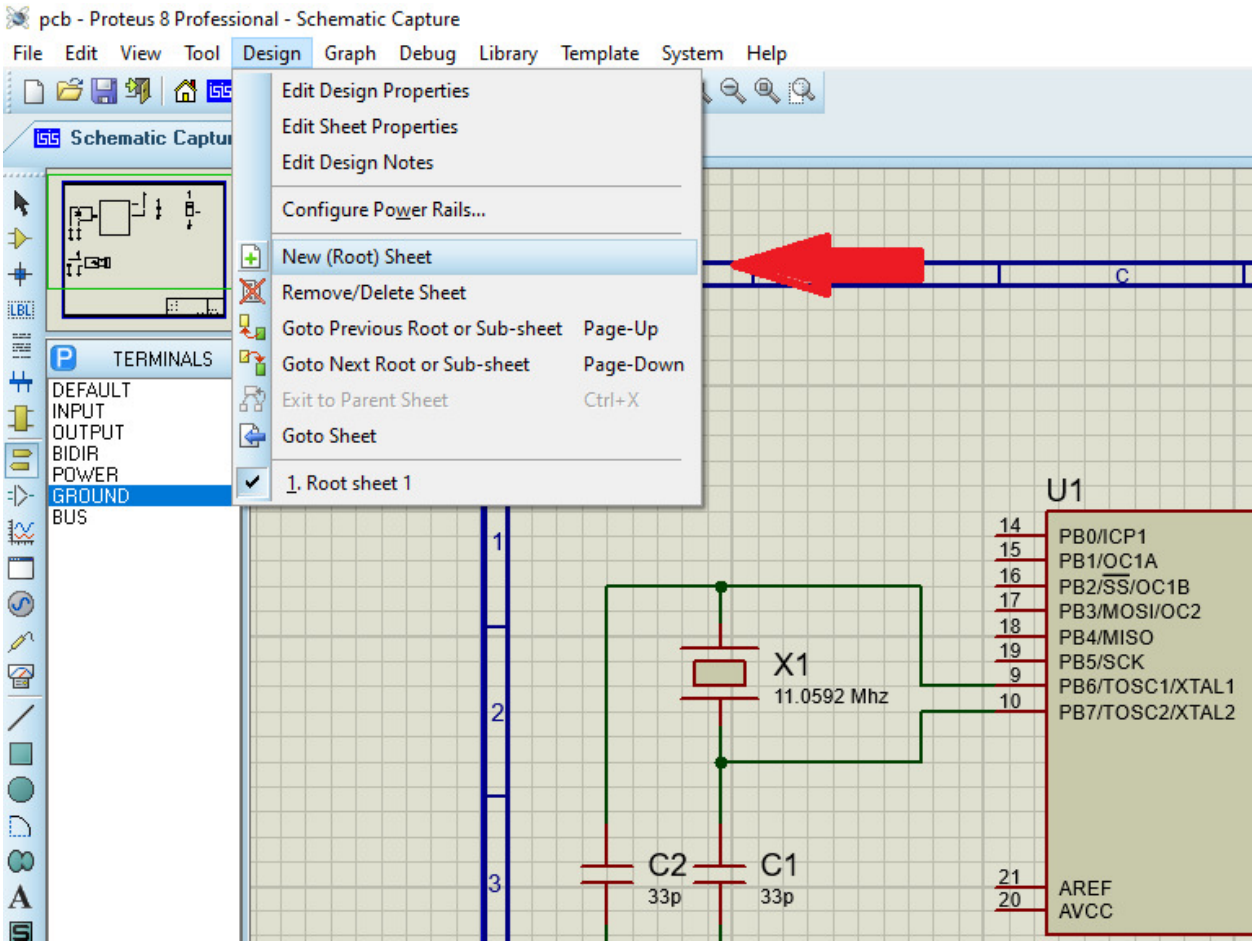
10. **To make a connection, click on the point from where the connection is to be taken and drag to the point to which the connection is to be made.**



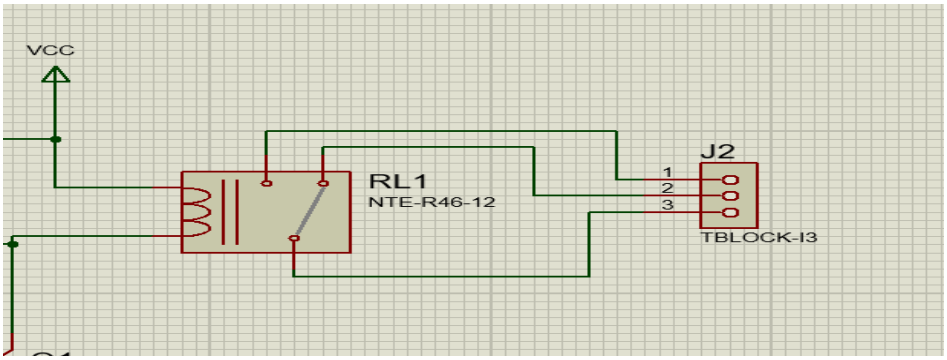
11. **To make a ground or Vcc.**



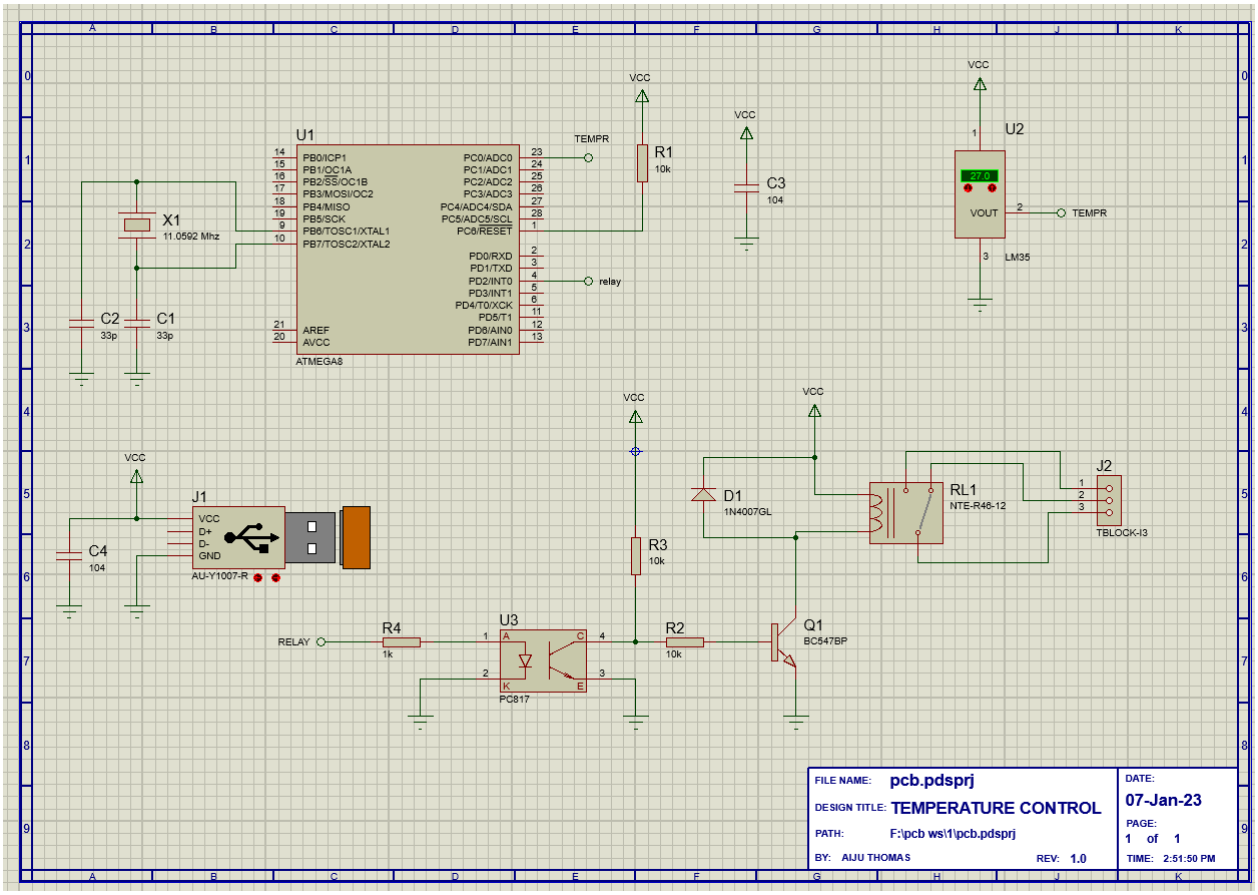
12. **To select a new sheet, do the following procedure. For navigating from sheet to sheet, use page up or page down.**



13. **To delete a component select the component and press delete.**
14. **Use suitable connectors to ensure modularity of design**



15. **Repeat the steps to complete the schematic.**



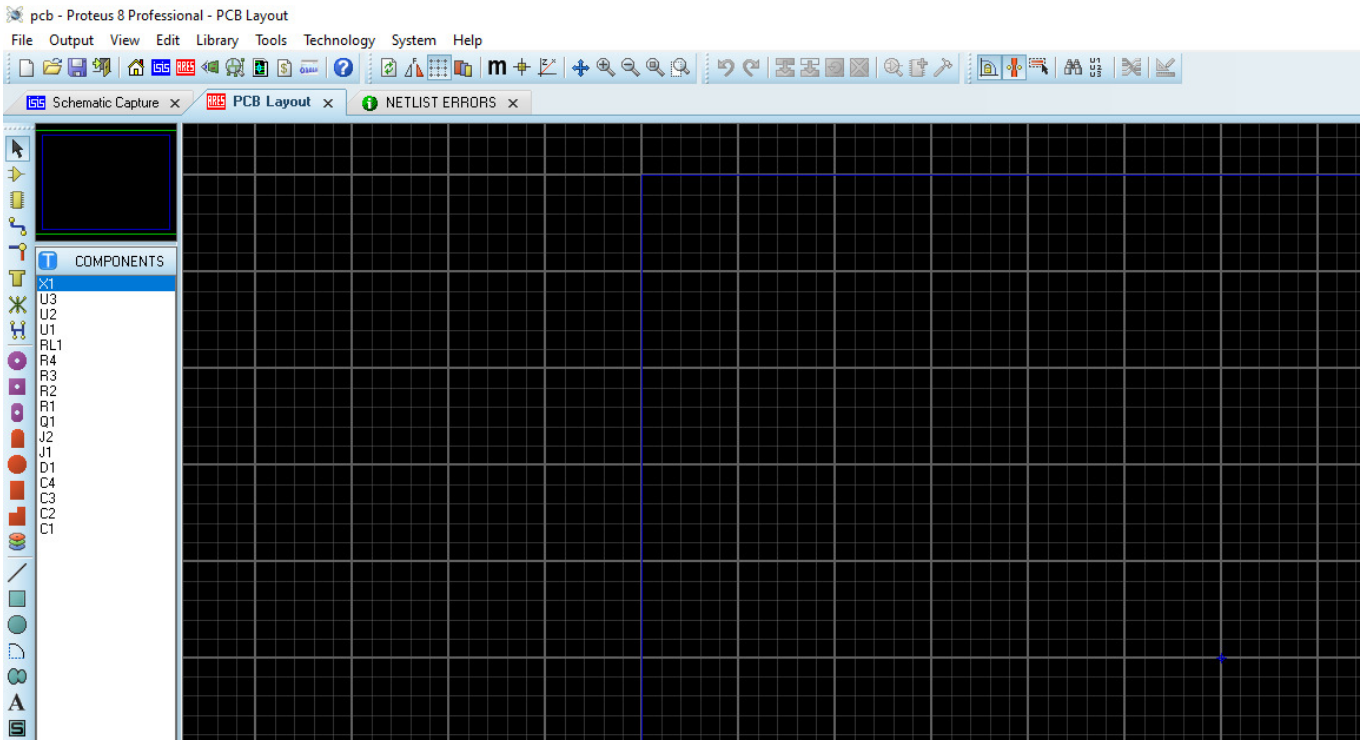
Inference	**The schematic drawing is made using schematic capture**		
Lab in charge		**Date**	

Exp: 6	Preparation of PCB layout	Date :

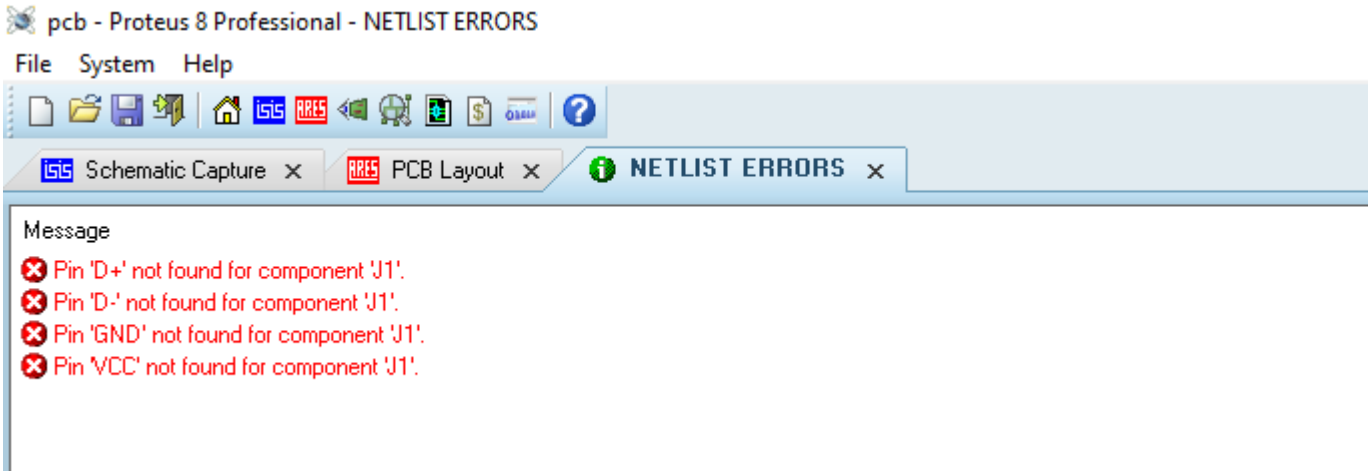
Time : 3 hours

Problem Statement: Prepare PCB layout in double layer for the circuit given in experiment no. 5.

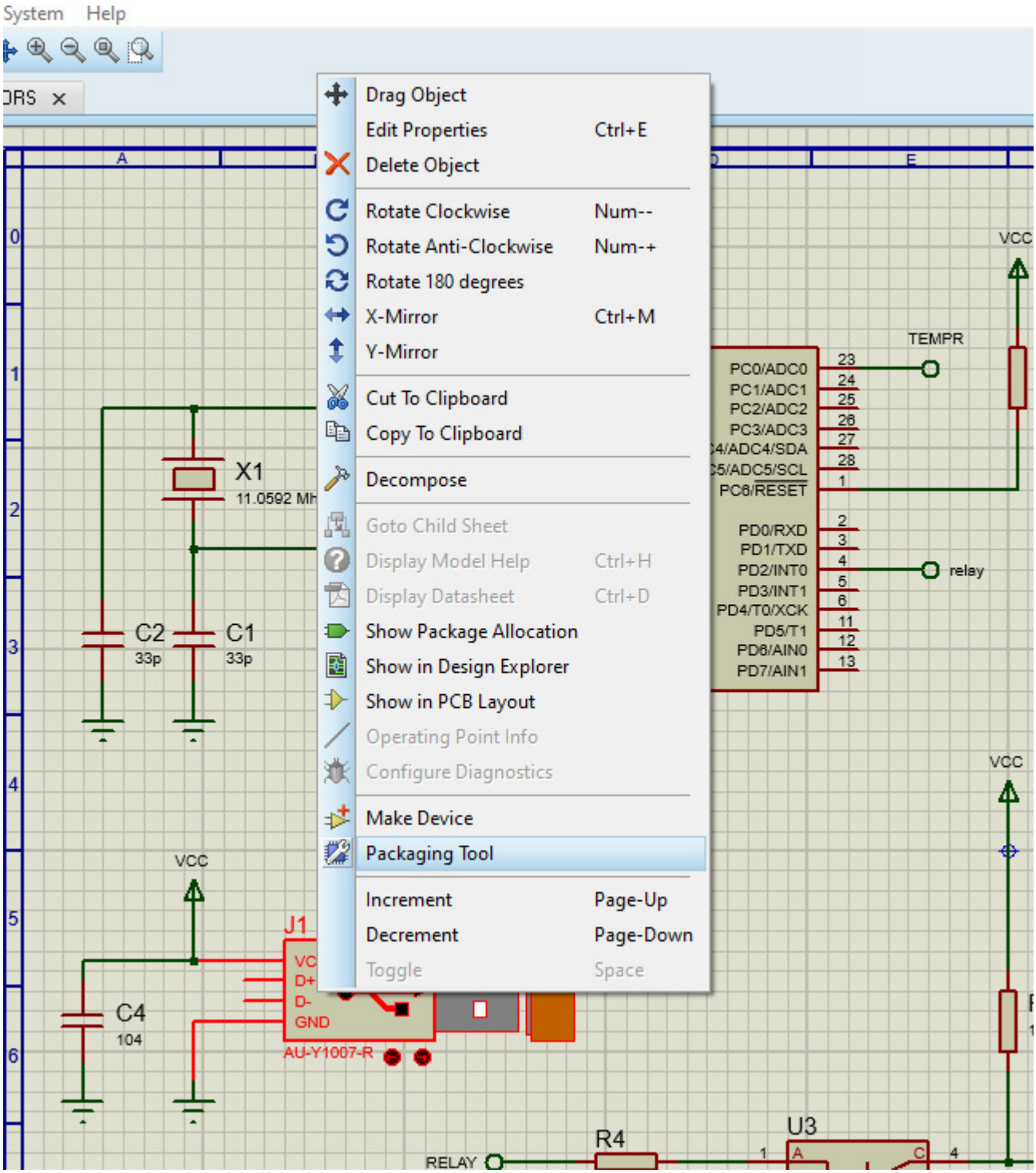
1. **Select PCB layout tab as shown below.**



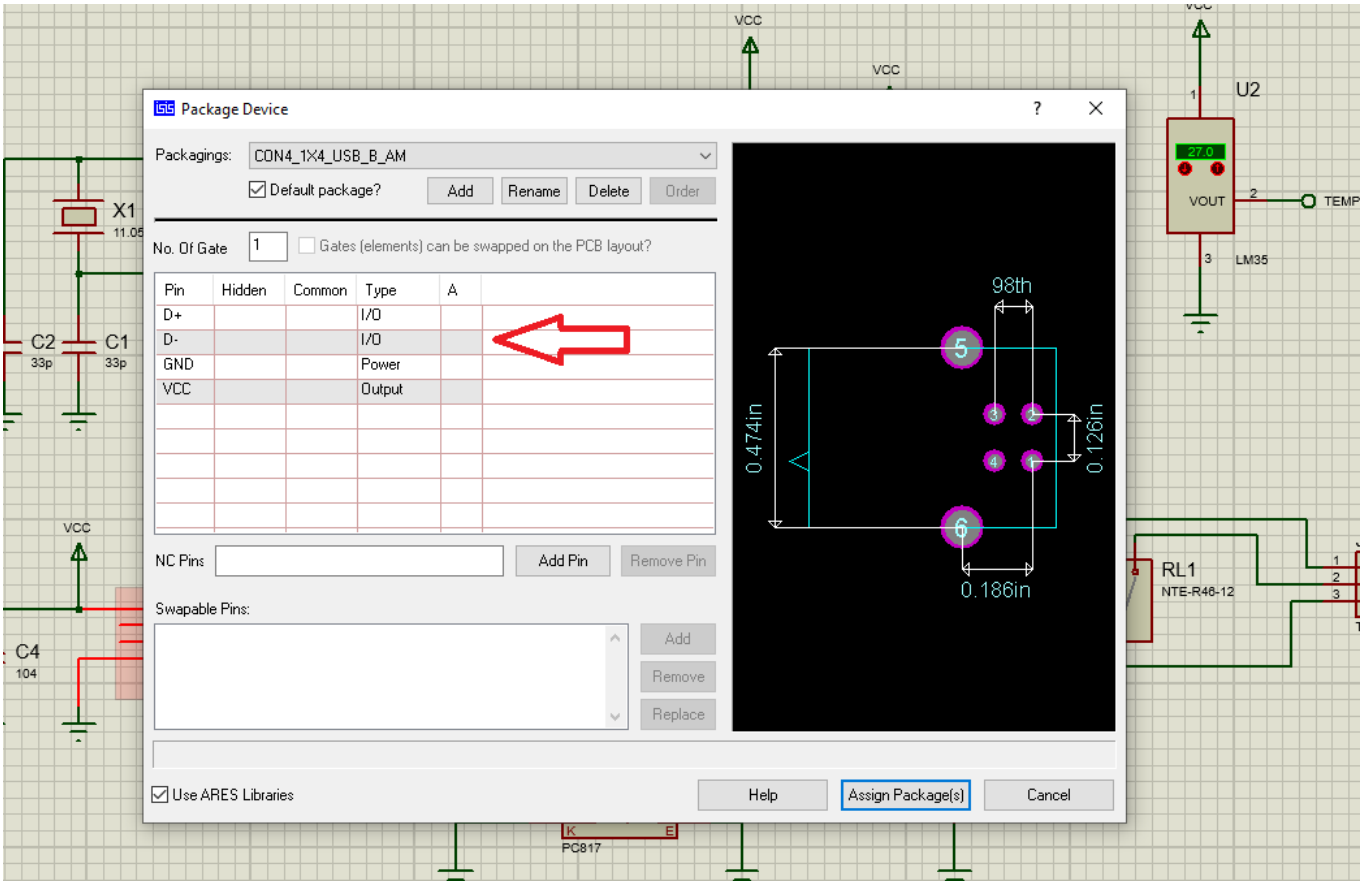
2. **If the lay out shows any net list errors, to rectify such errors click on NETLIST ERRORS tab.**



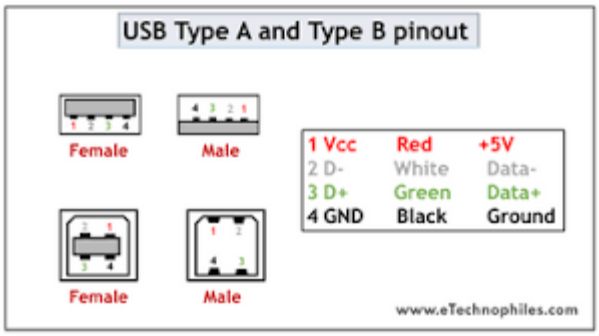
3. **In this specific case, connector J1 is not assigned pin numbers. To assign pin umbers go to schematic capture select the component, right click and select packaging tool.**



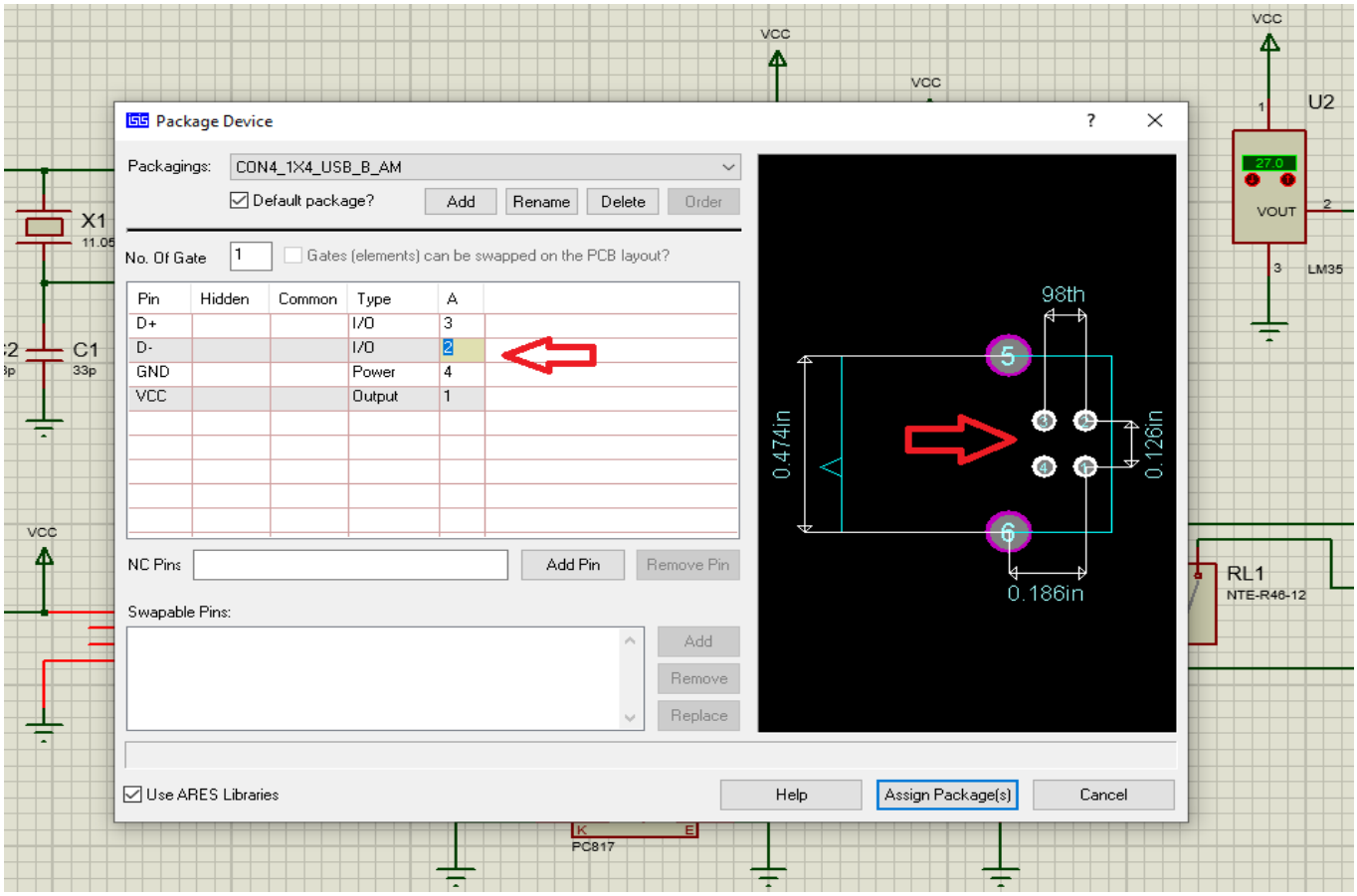
4. You will see that pin numbers for the connector are not assigned.



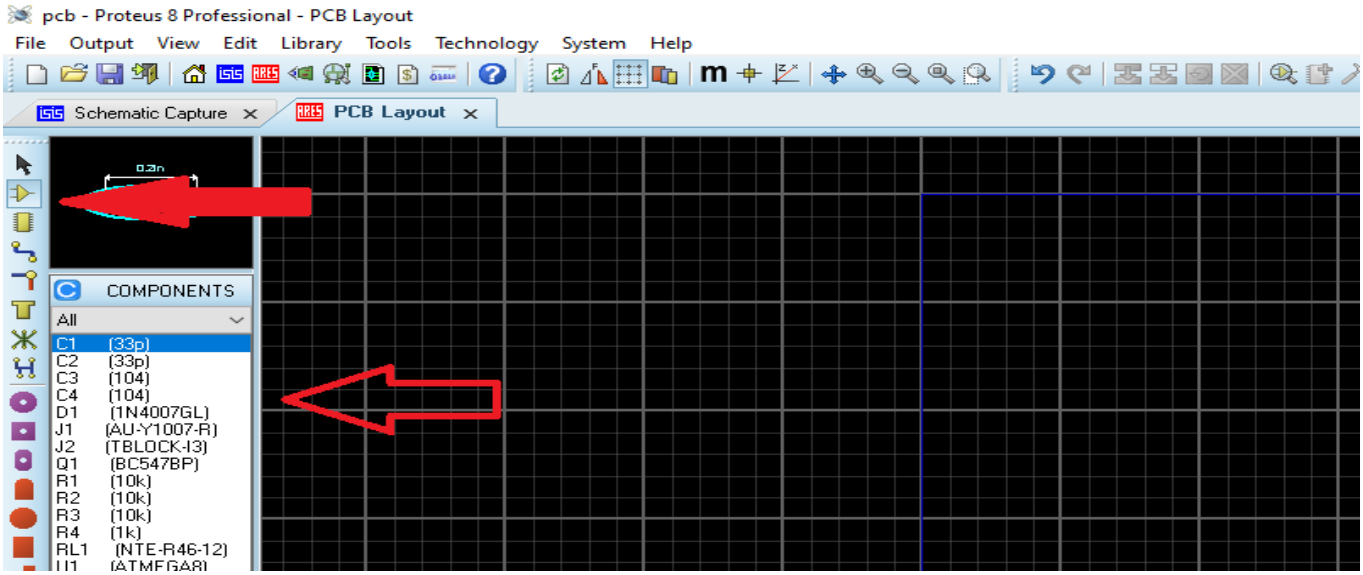
5. Check the internet ofr exact pin configuration of the connector, in this case USB Type B



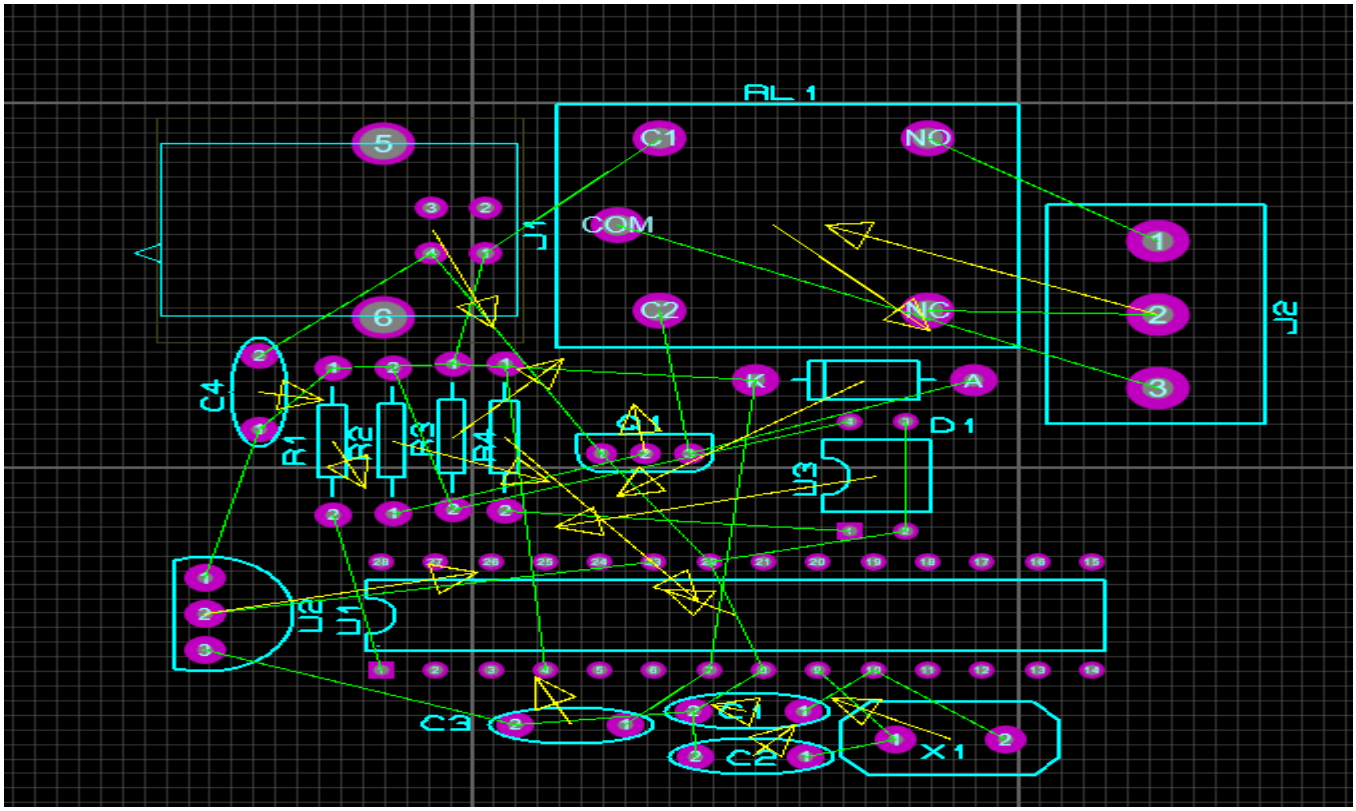
6. **Select the suitable pin and click assign package and proceed as per instructions.**



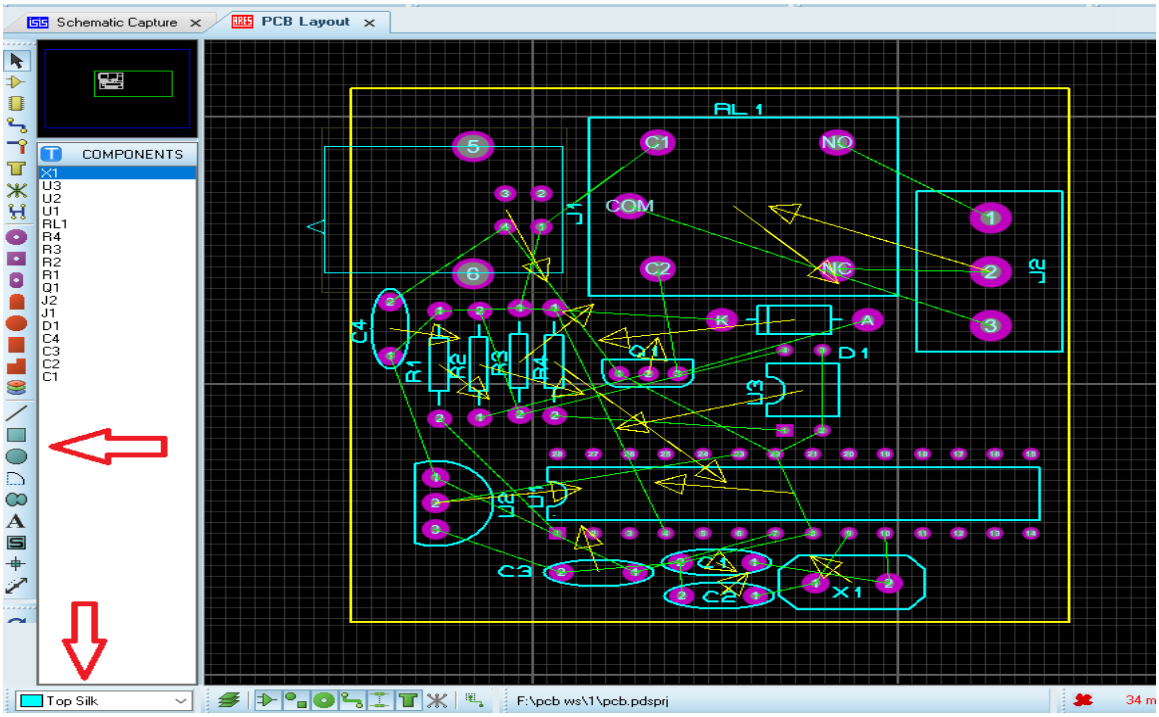
7. **Select and place componenets from compnents tab. Check whetehr all componenets used in the schematic are available in the lay out tab.**



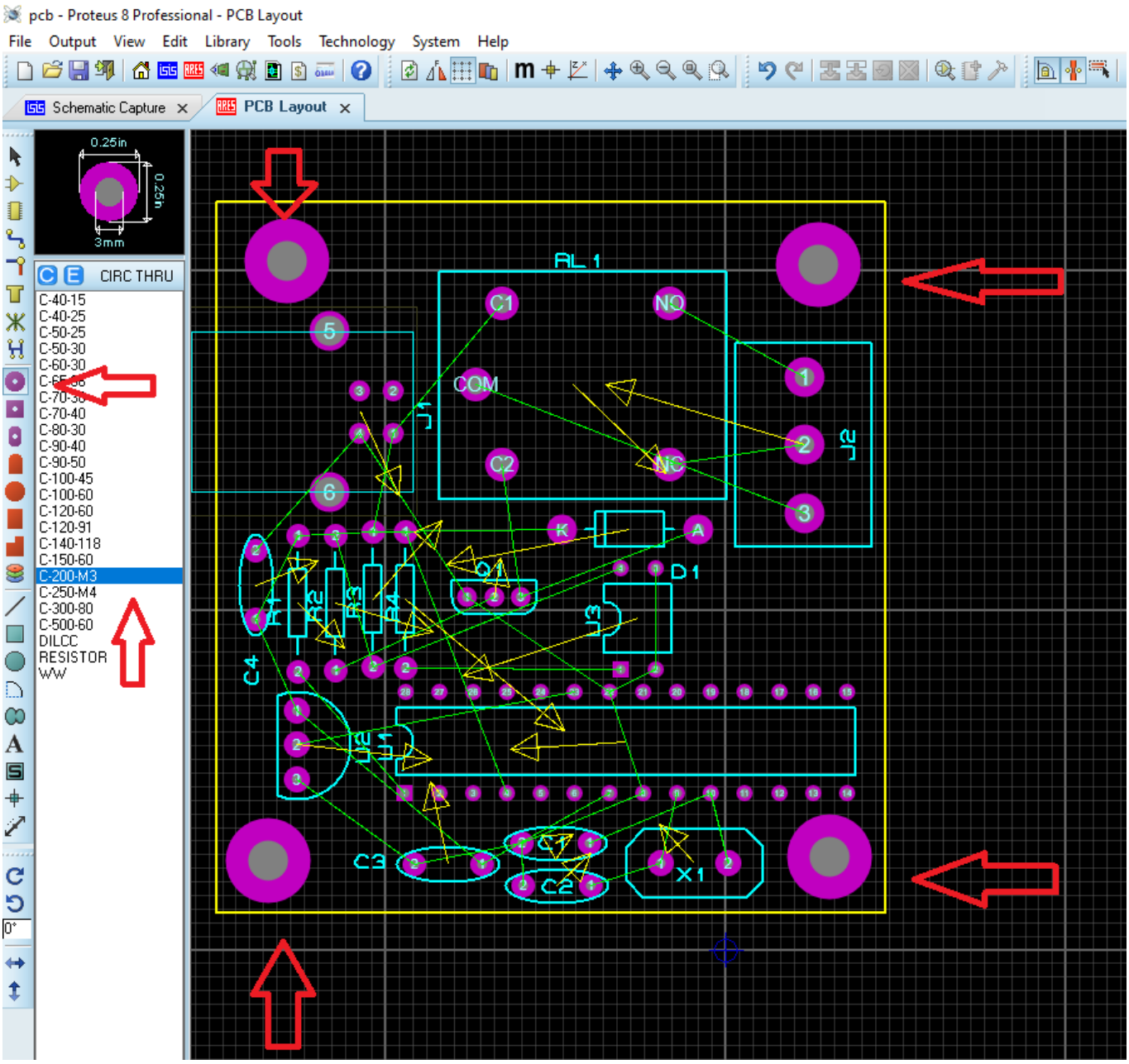
8. Place the components suitably.



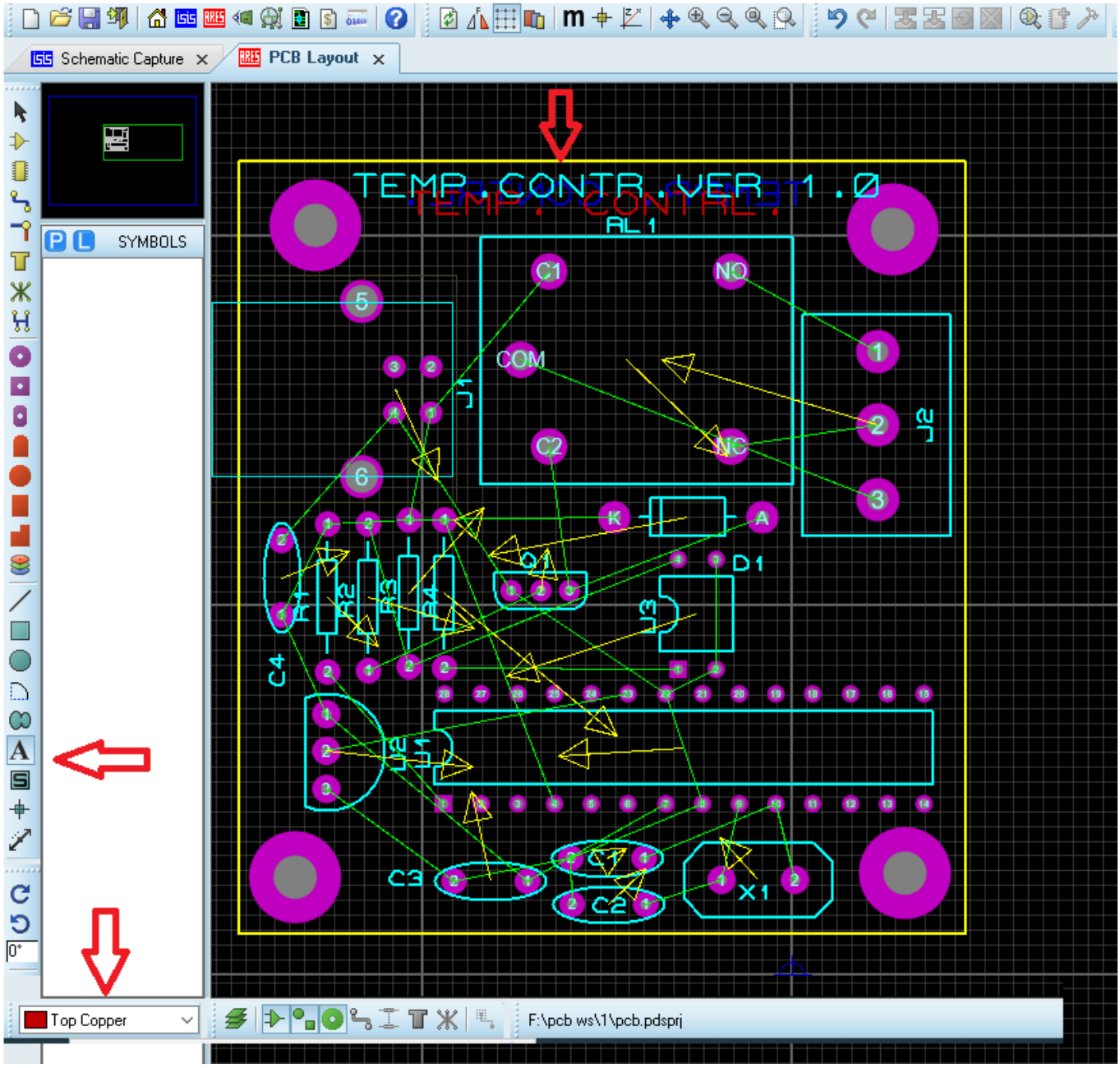
9. Draw board edge.



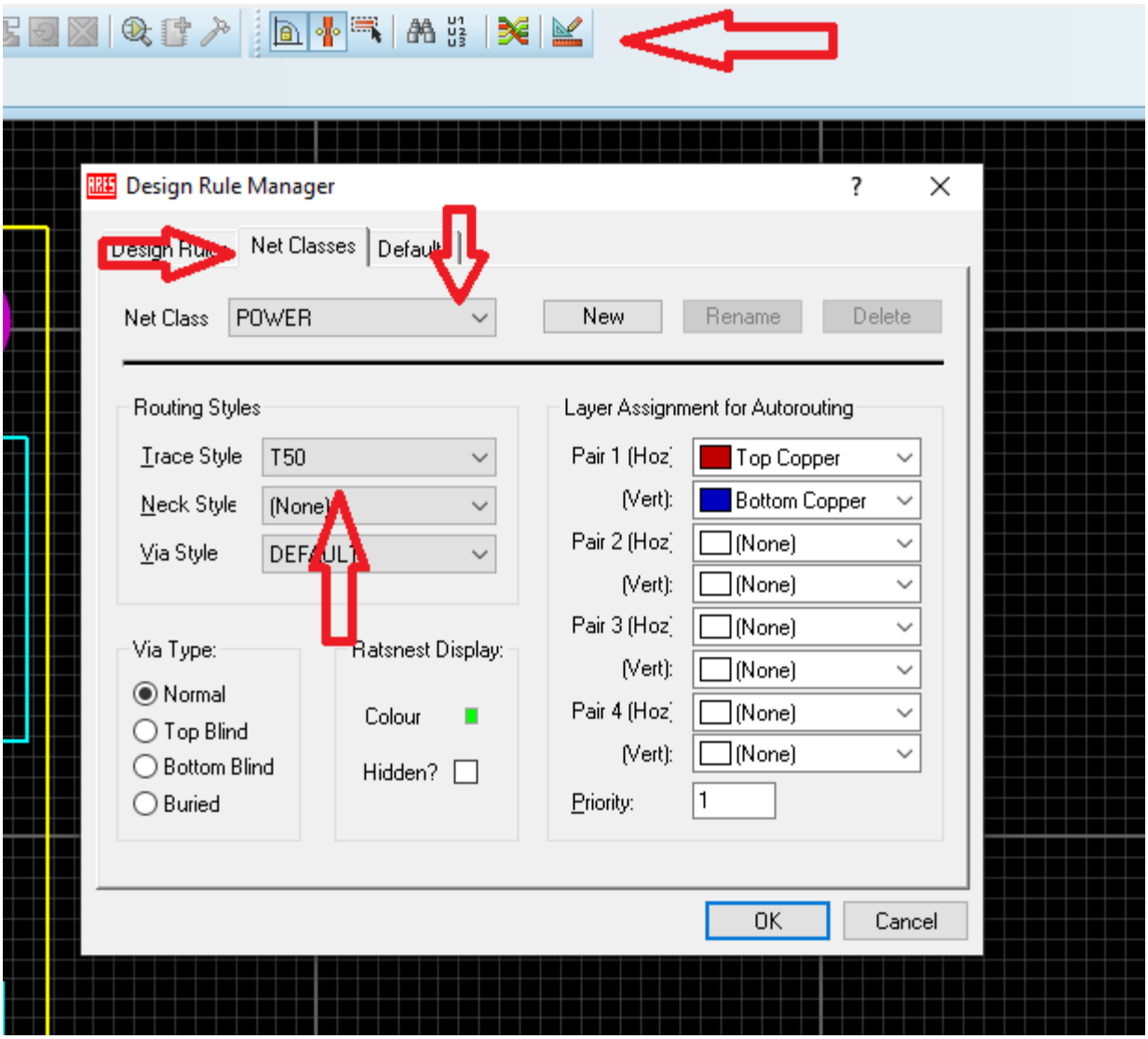
10. Put M3 mounting hole



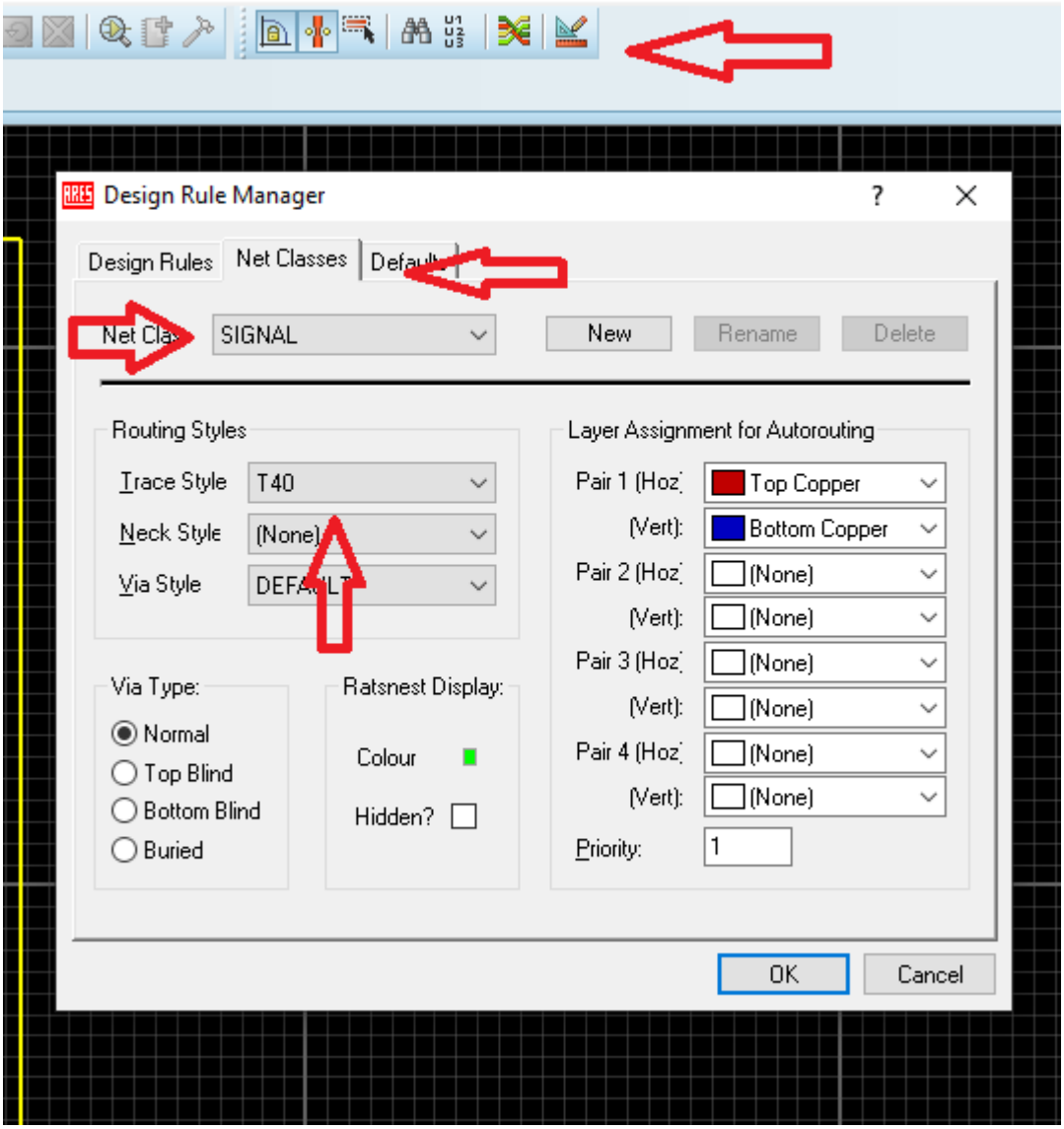
11. Insert suitable label on Silk layer/ top layer or bottom layer



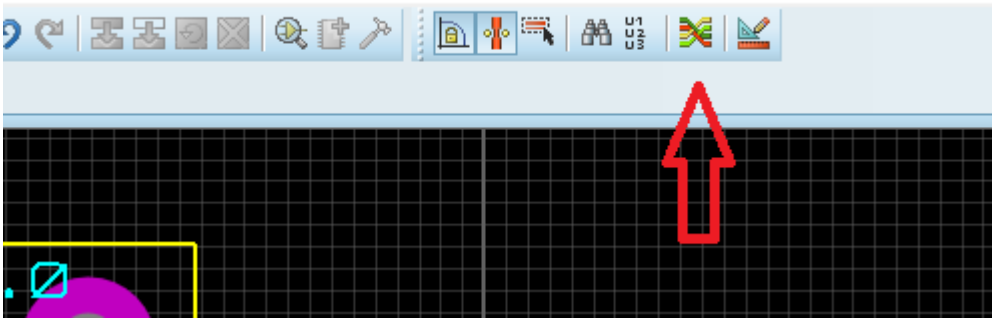
12. Set Design Parameters for power



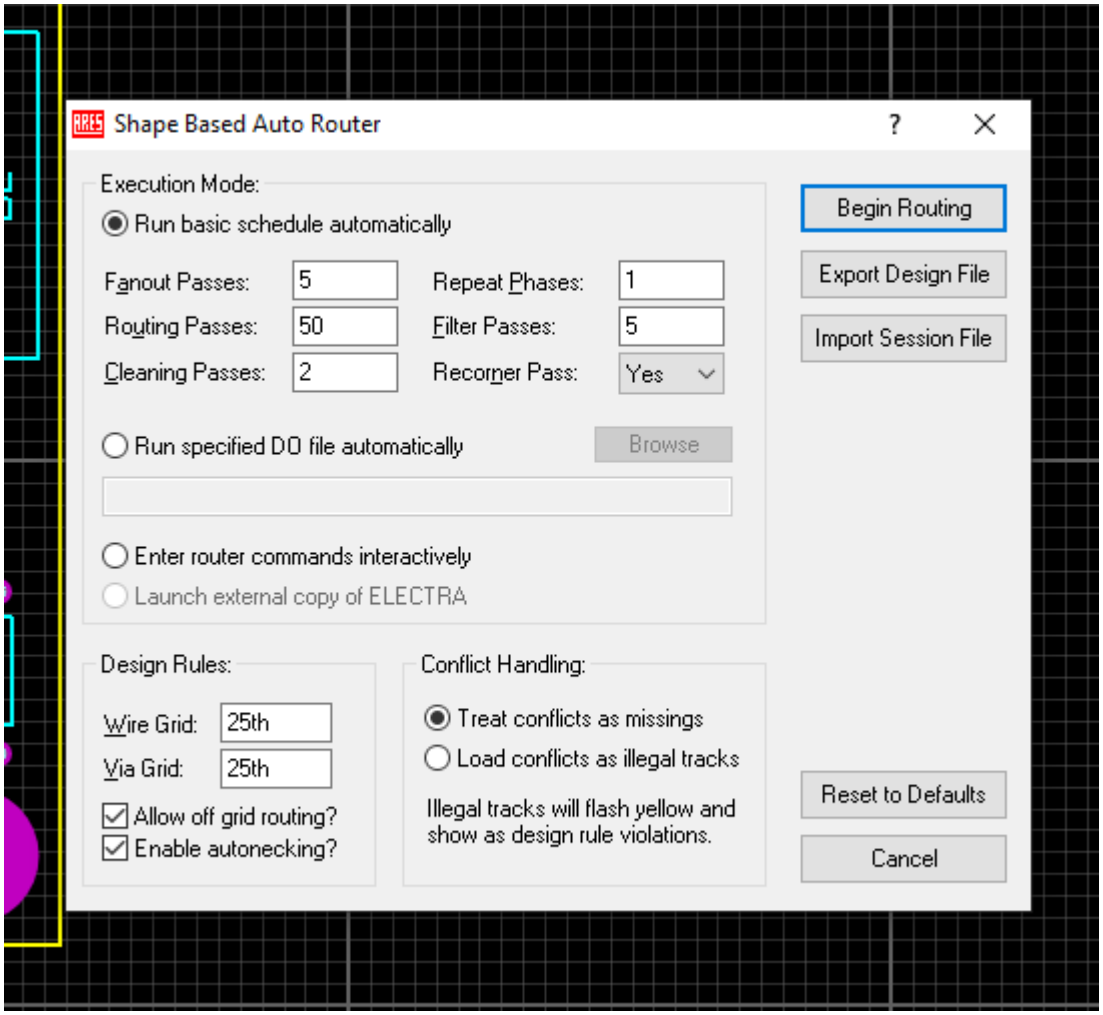
13. Set design parameters for signal



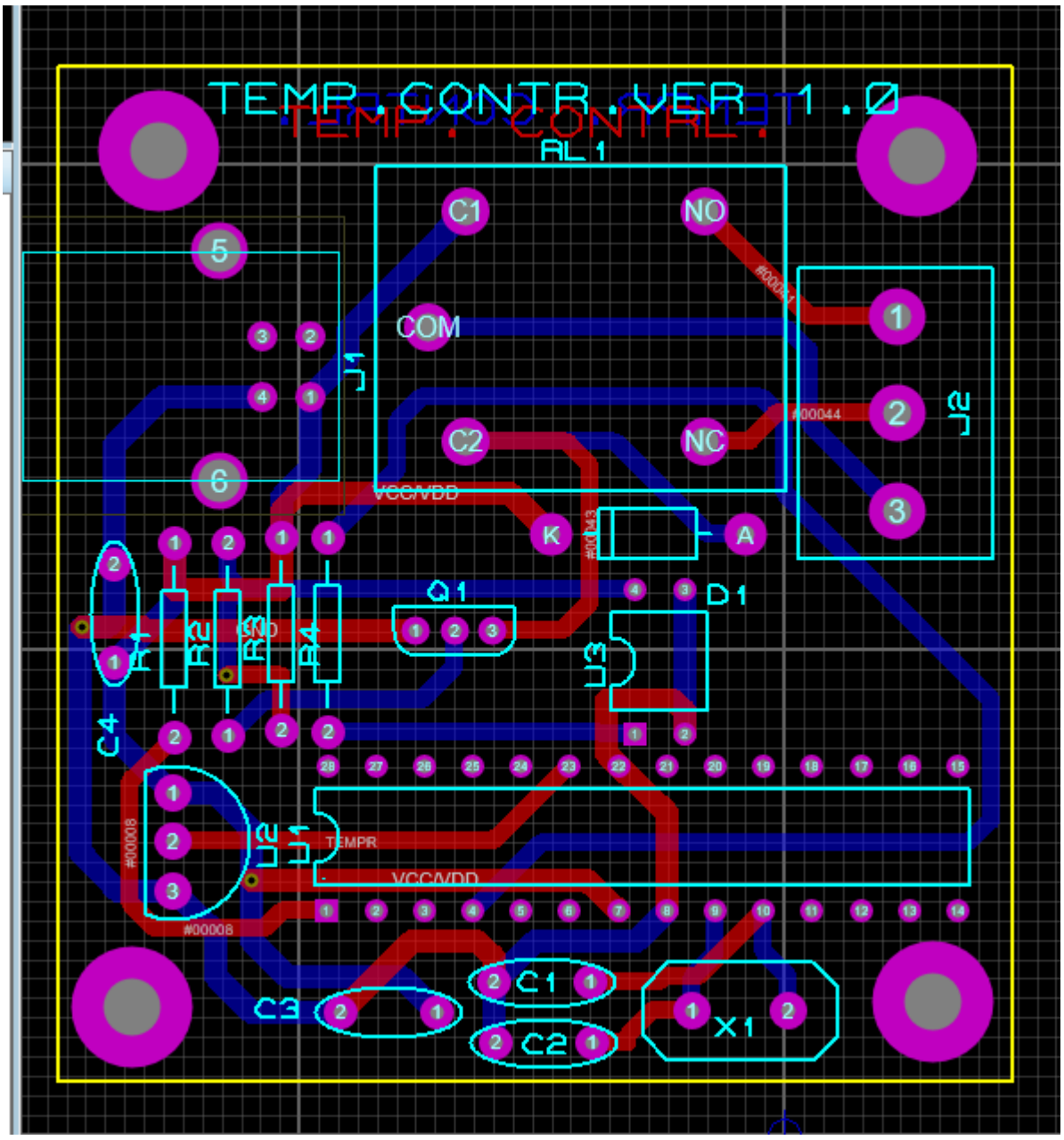
14. Click auto routing and wait for the PBCB to be completed



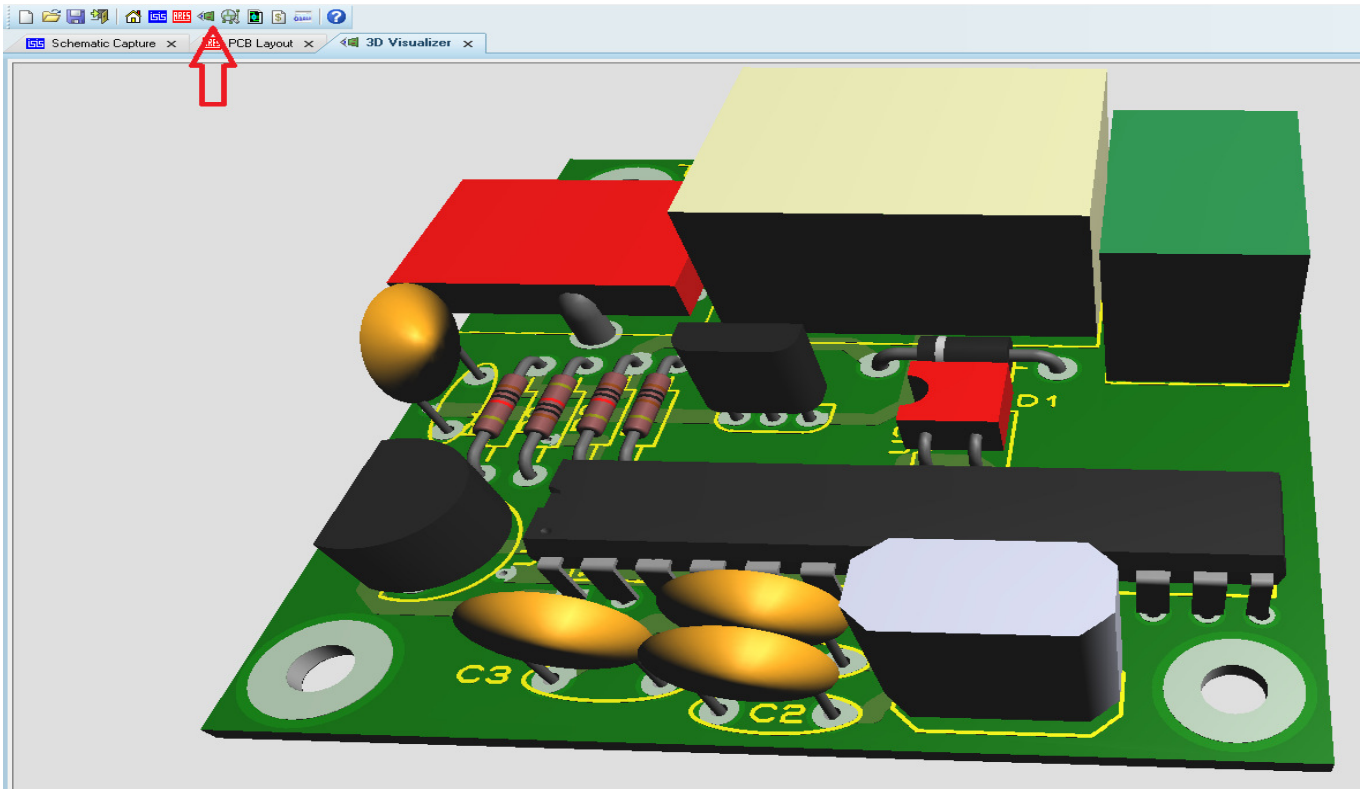
15. Click begin routing

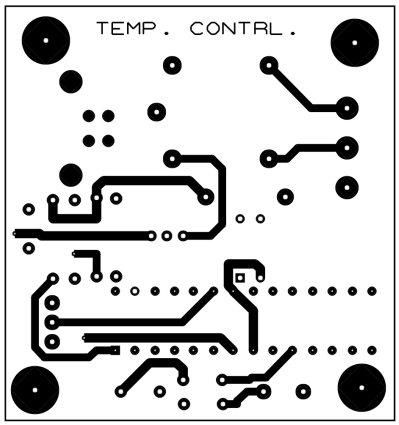


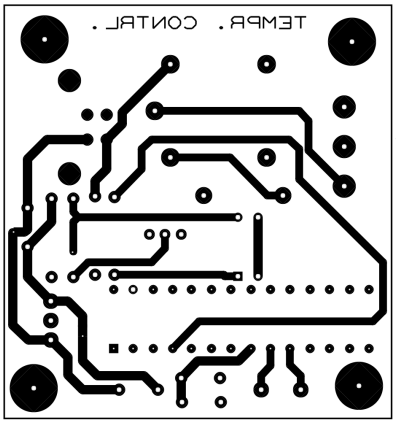
16. The PCB layout is ready

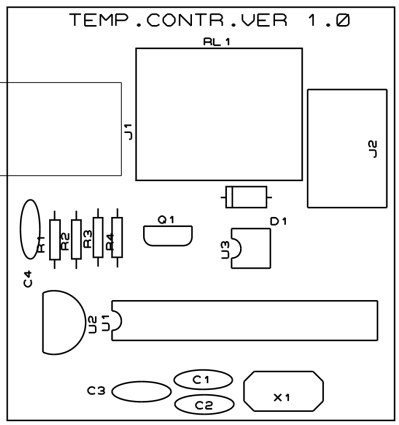


17. For a 3d View









TOP LAYER **BOTTOMN LAYER** **SILK SCREEN**

Inference	**The two layer PCB layout for the given schematic is prepared**		
Lab in charge		**Date**	

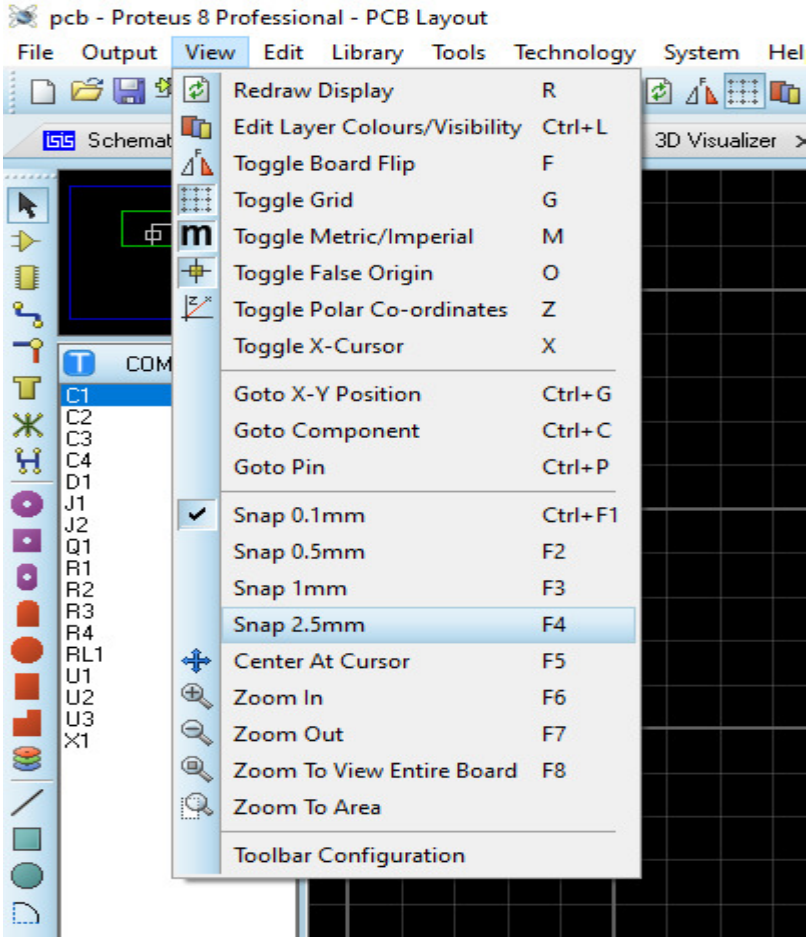
Exp: 7	PCB designing at constrained dimensions	Date :

Time : 120 minutes

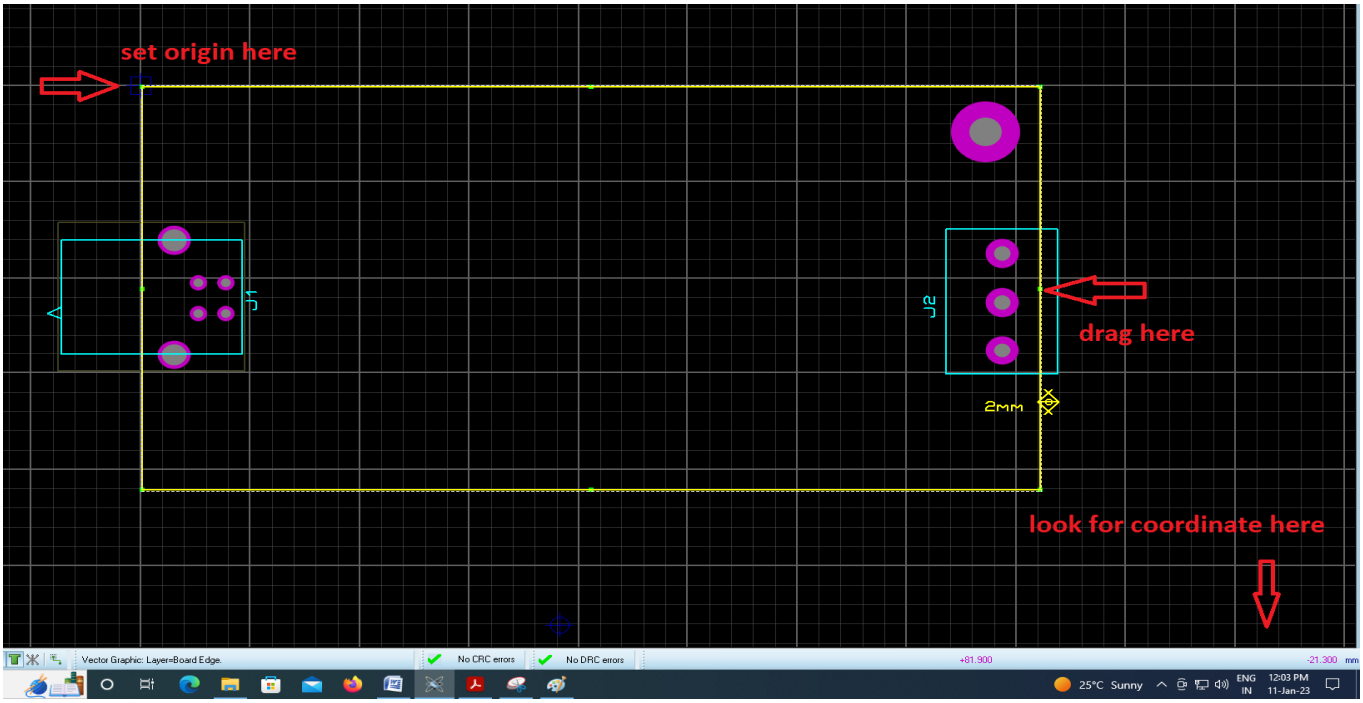
Problem Statement: Prepare double sided PCB of Experiment 5 restricting PCB dimensions as shown below.

Procedure:

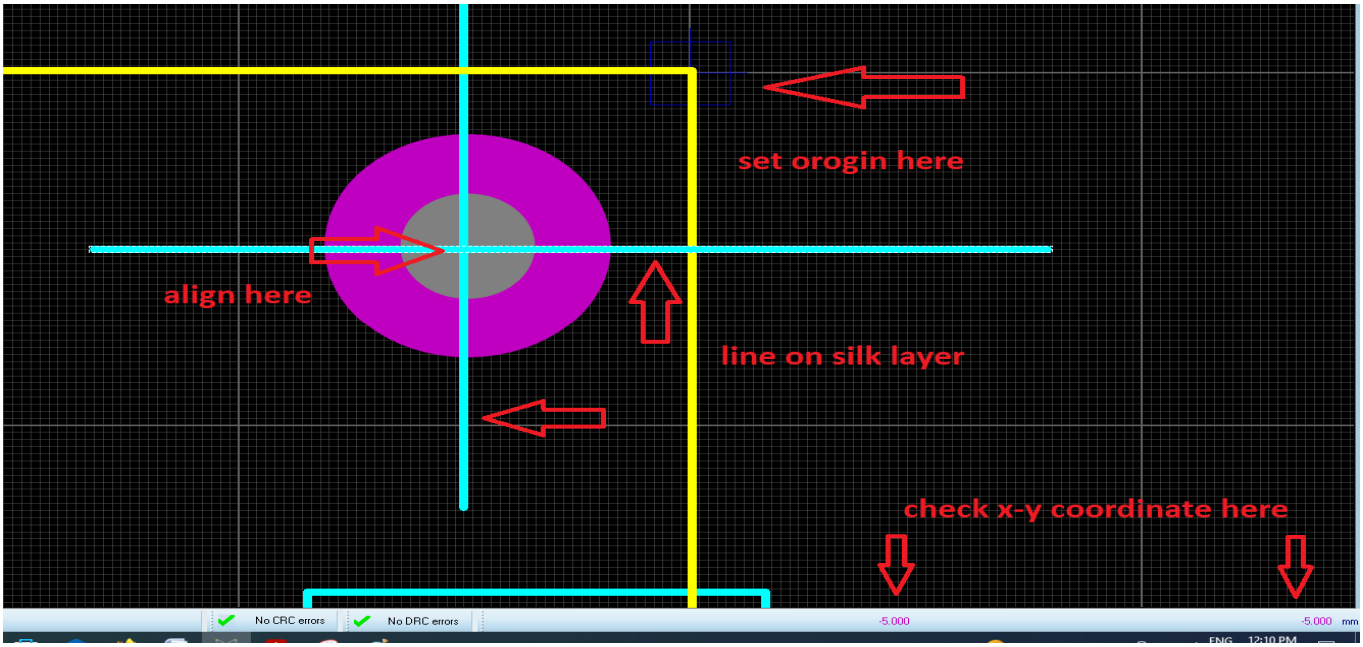
1. **Select convenient snap from the menu**



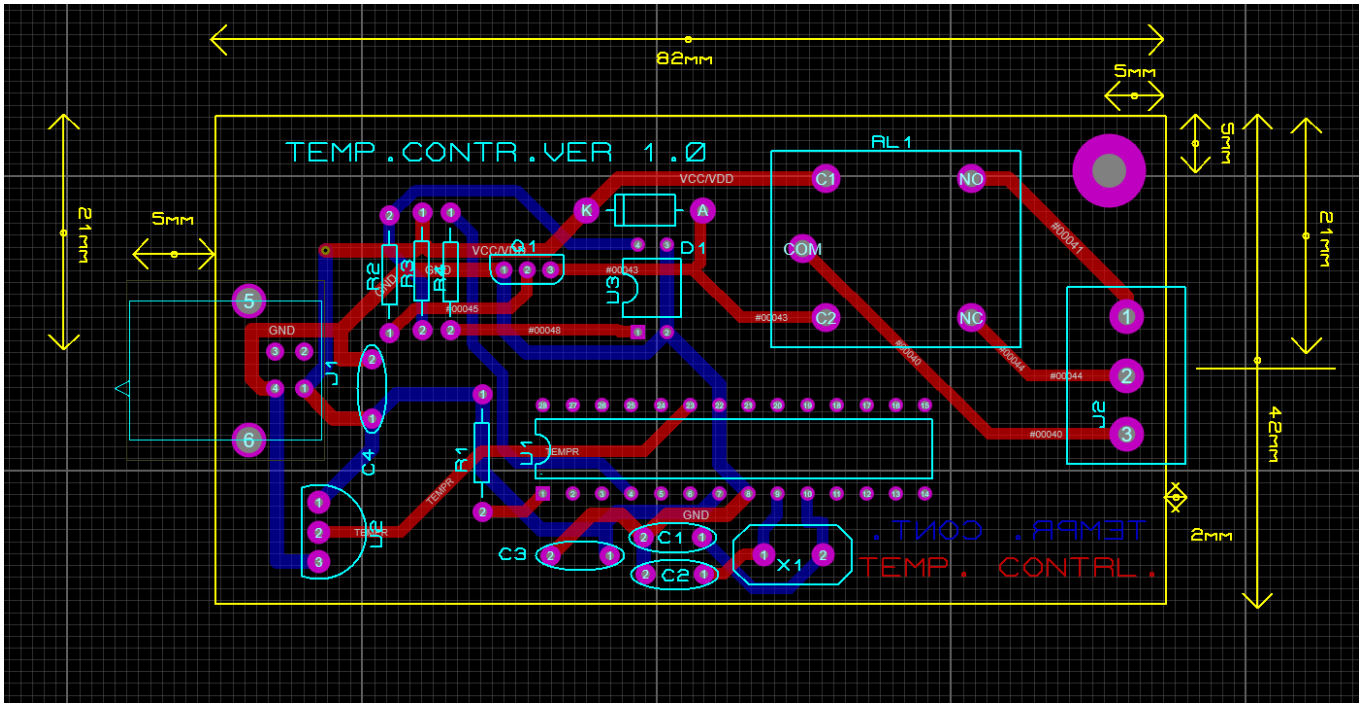
2. **Select one corner of the board edge as origin by pressing "O" key in the keyboard. Press "M" to toggle between inch and mm. Dragg the mouse keeping the pointer at the middle if the board edge to the required dimension looking at the coordinates on the bottom right. Origin**



3. **To position mounting hole use line in silk layer to fix the coordinate**



4. Finish routing the pcb



Result

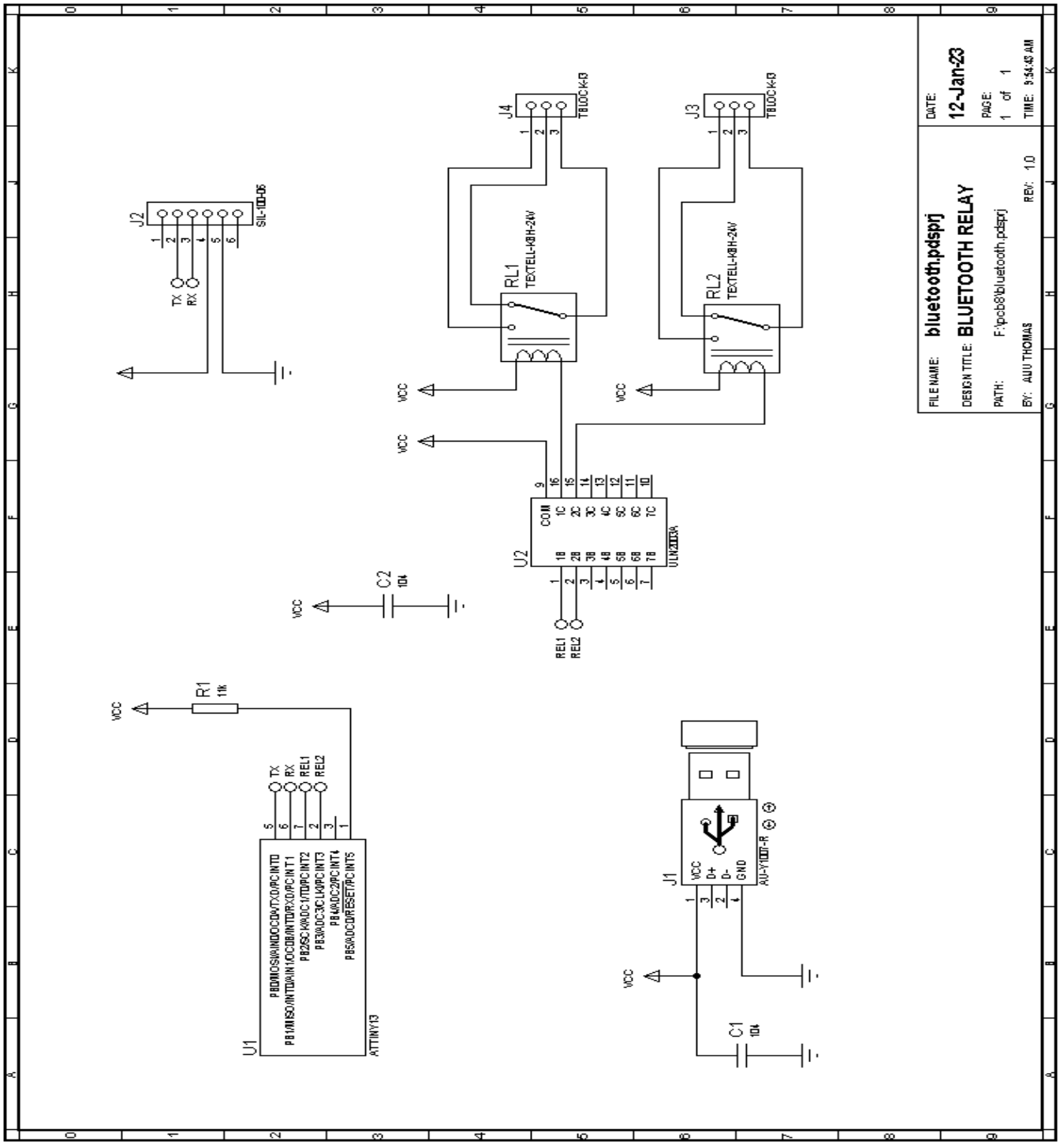
Double sided PCB prepared at constrained environment

Lab in charge	Signature of the lab incharge	Date
Readiness to do the experiment		
Completion of the experiment		

Exp: 8	PCB designing – Single sided	Date :

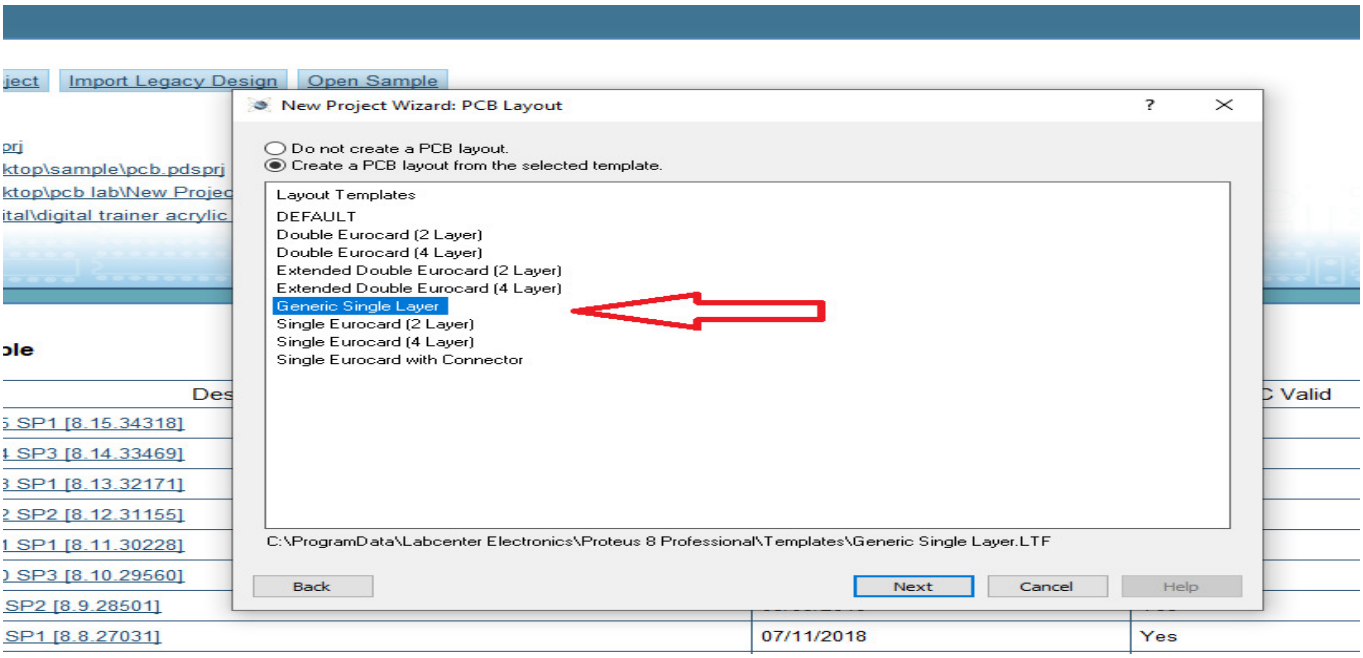
Time : 120 minutes

Problem Statement: Develop single sided PCB for the given circuit.

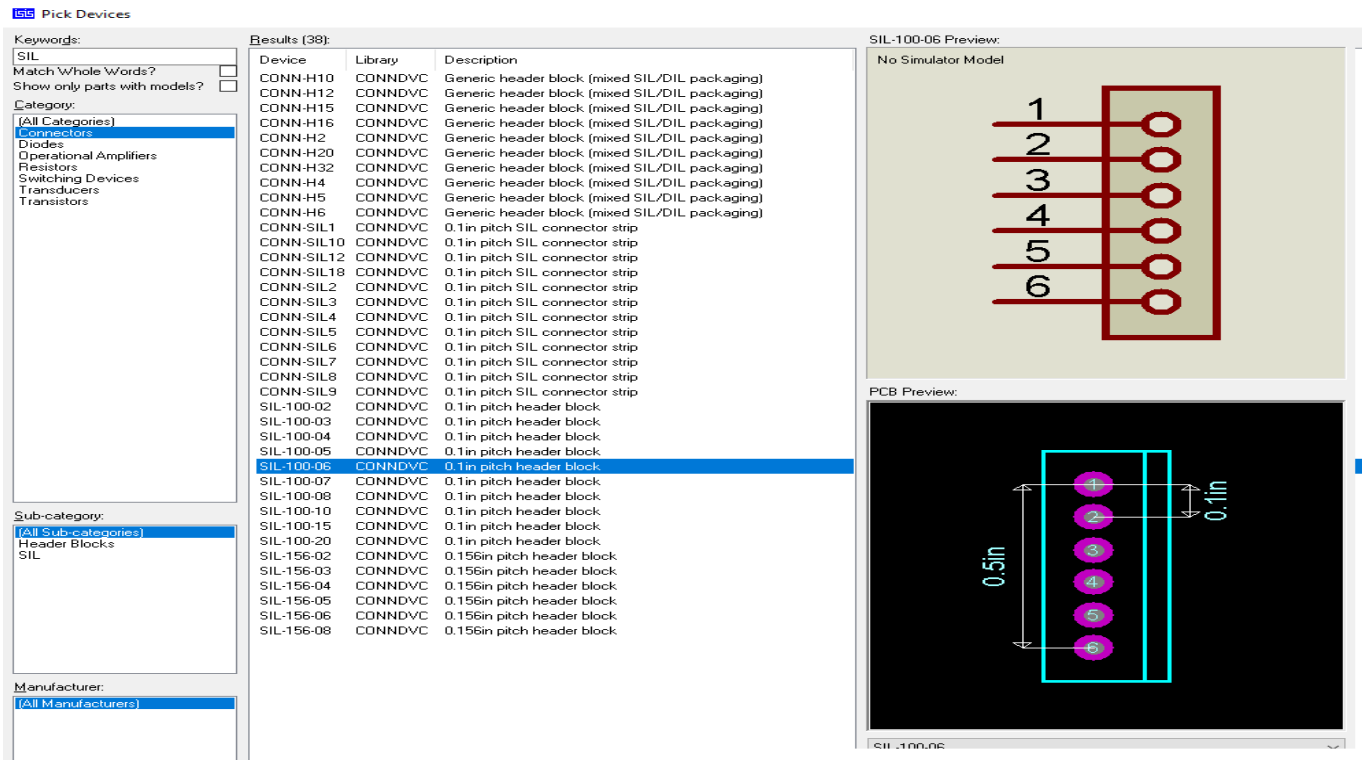


Procedure:

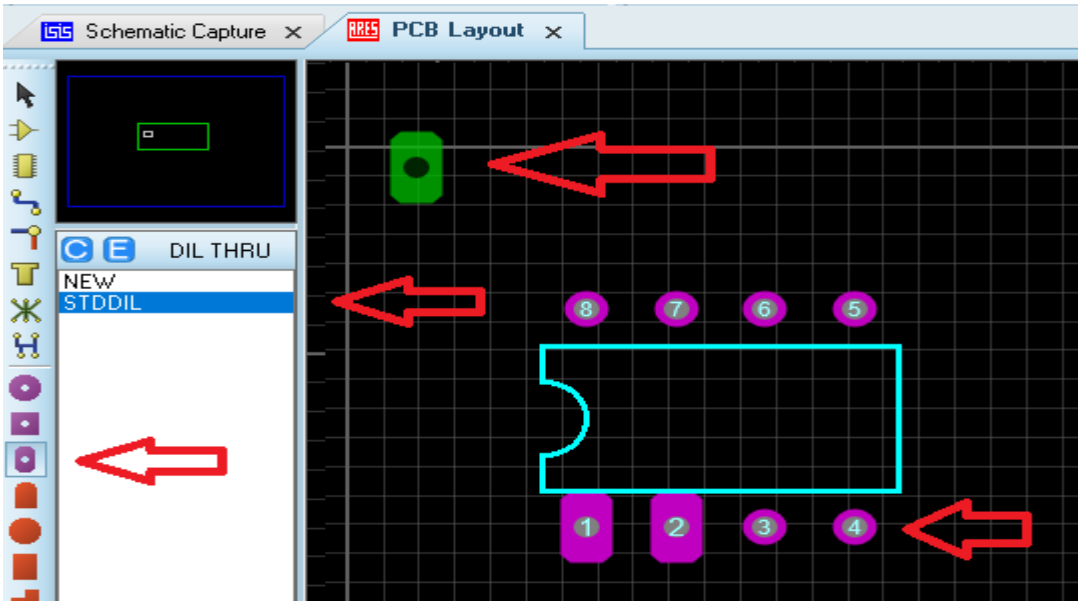
1. **Open new project and select Generic Single Layer PCB.**



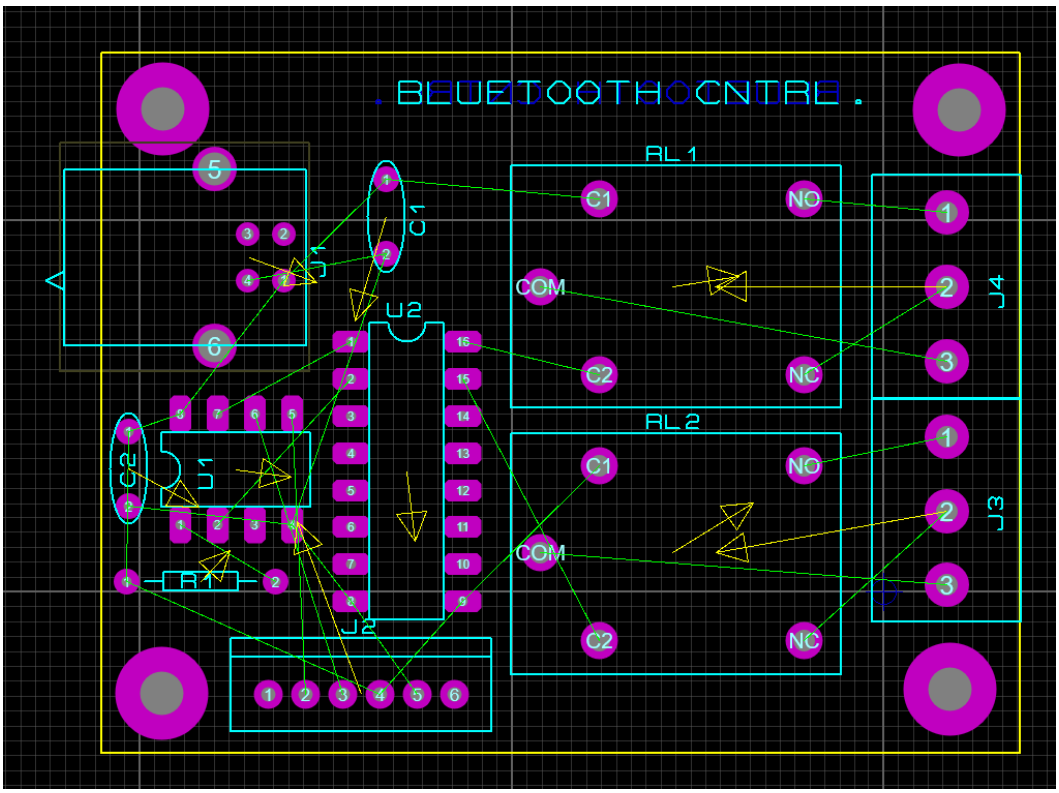
2. **Complete schematic use 6 pin SIL connector for HC-05 (Bluetooth)**



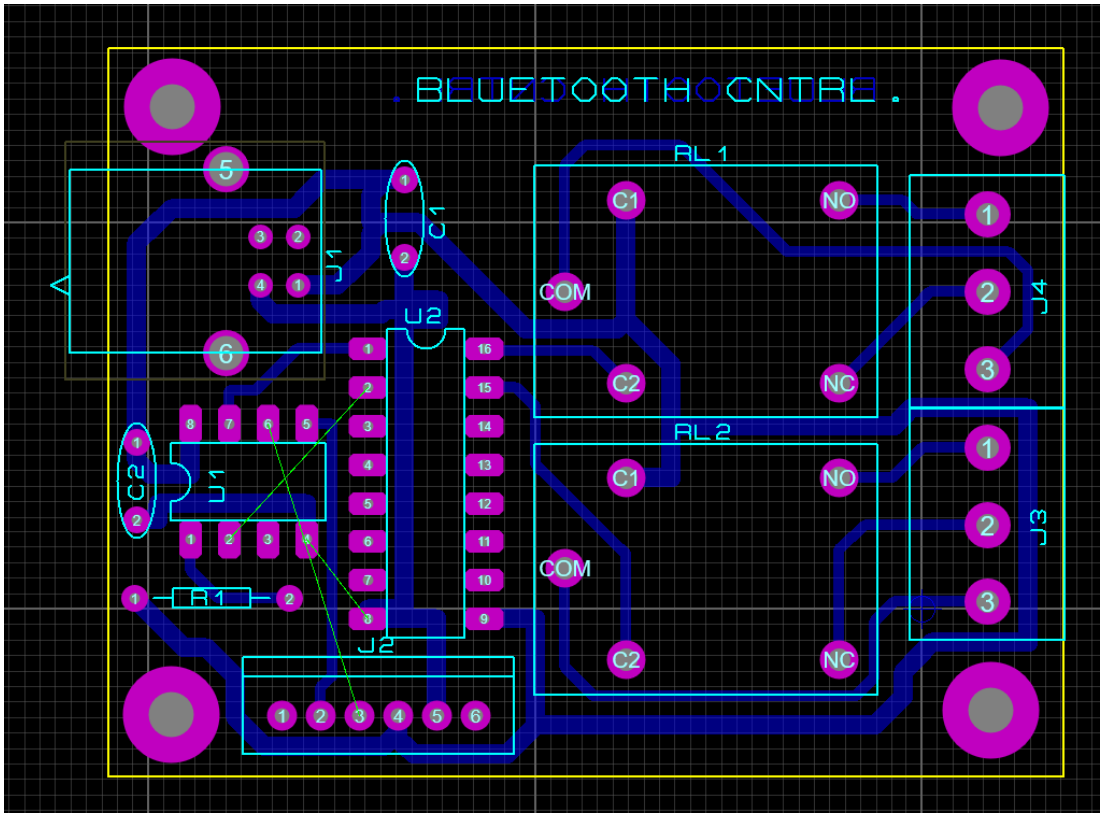
3. **Place components as done before. Please note that for DIP package the pad size is too small for soldering. Insert STDDIL from DIL pad mode.**



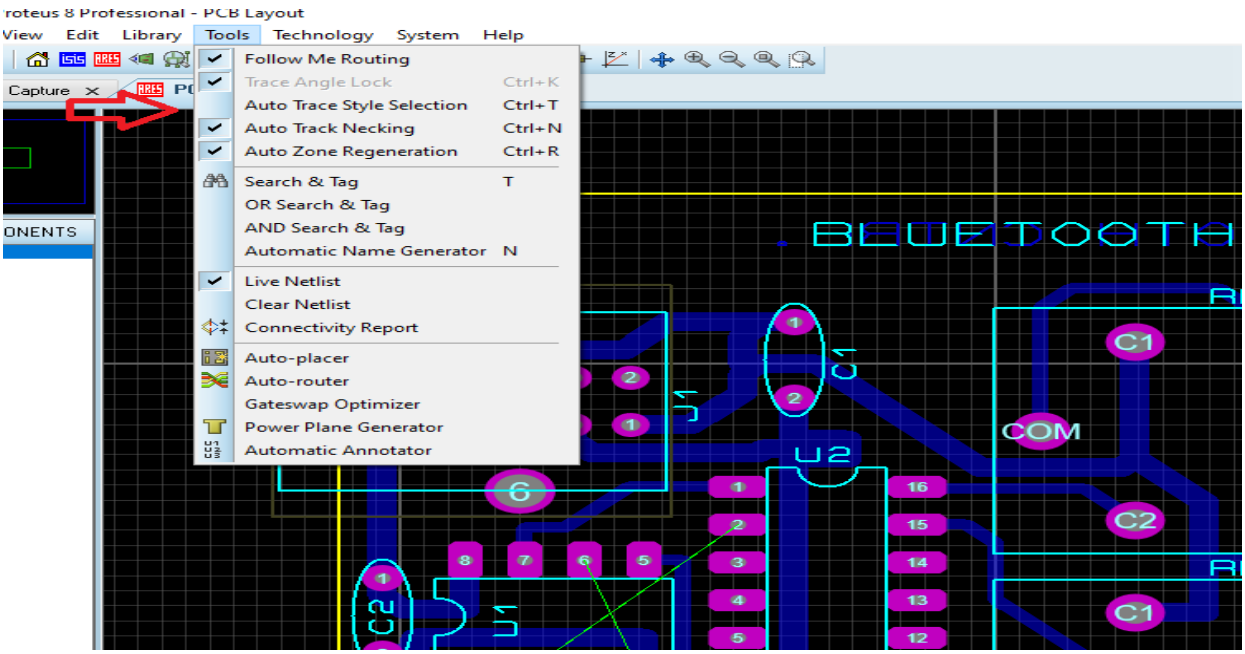
4. **Complete component placing**



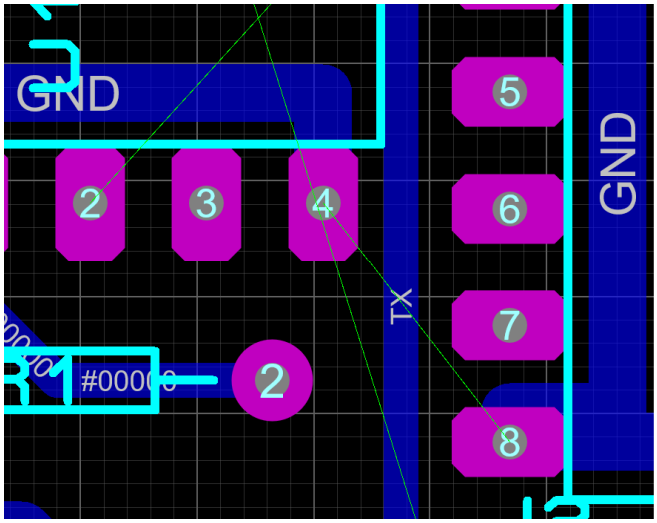
5. **Set rules and finish auto routing the PCB. You will find missing connections in green.**

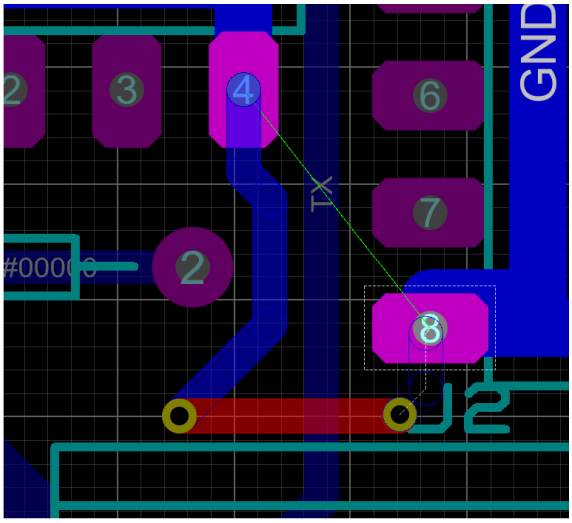


6. **Unfinished connections have to be routed manually. For that disable auto track selection.**

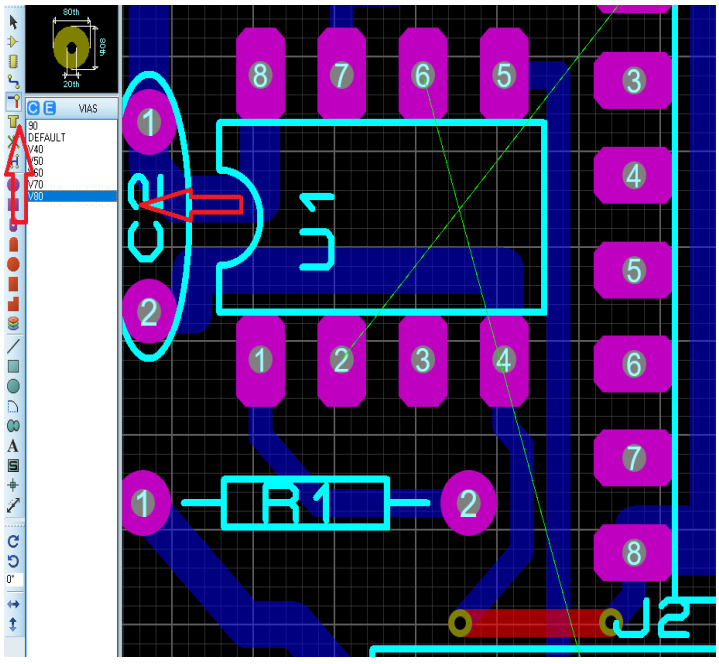


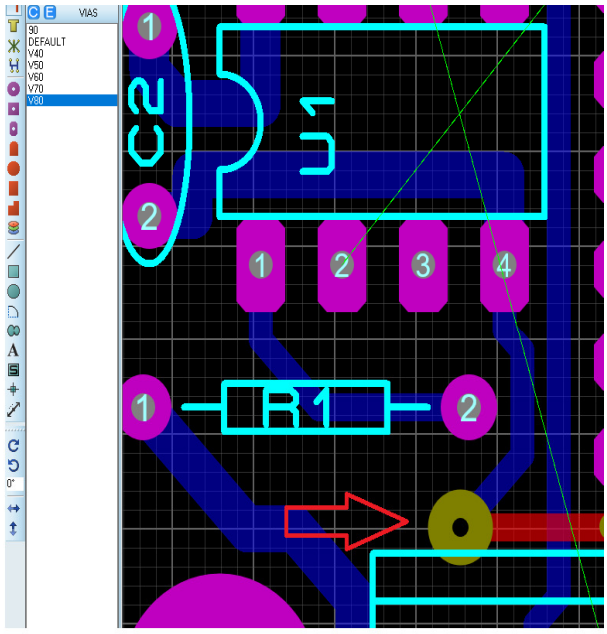
7. **Select trace from the menu and do manual routing of unfinished traces. Any traces that need to be modified due to current handling capability or possibility of interfere.**



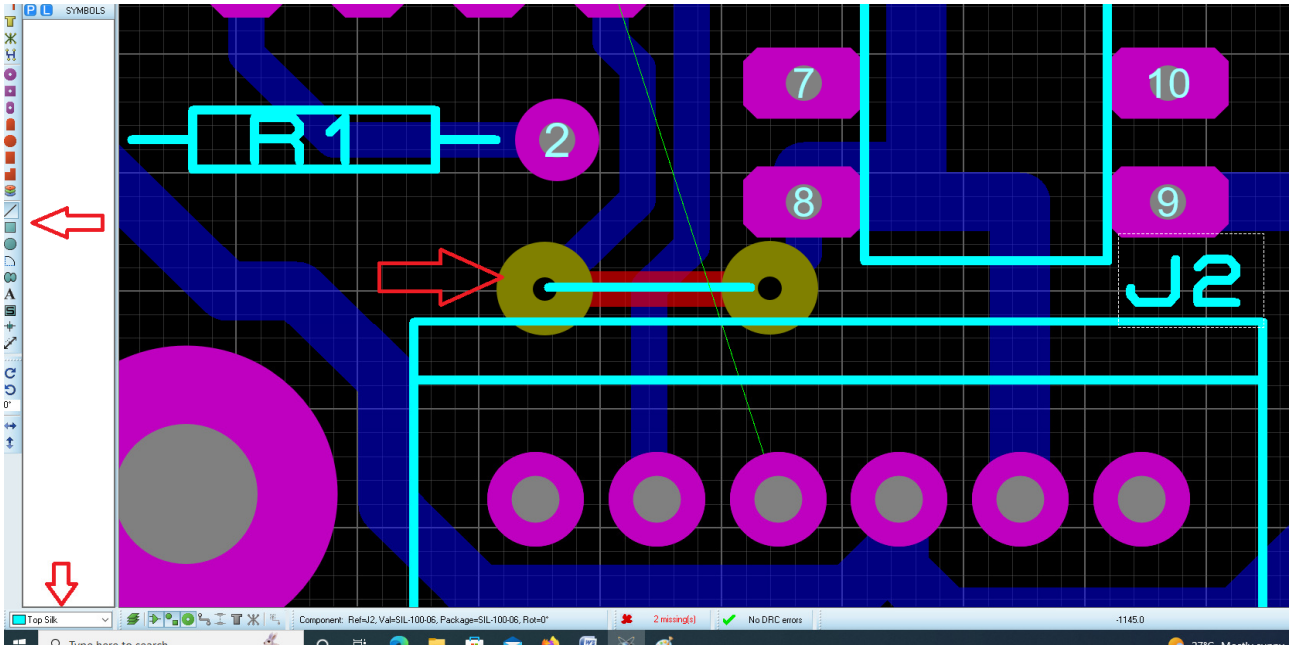


8. **Increase via size to do soldering properly**

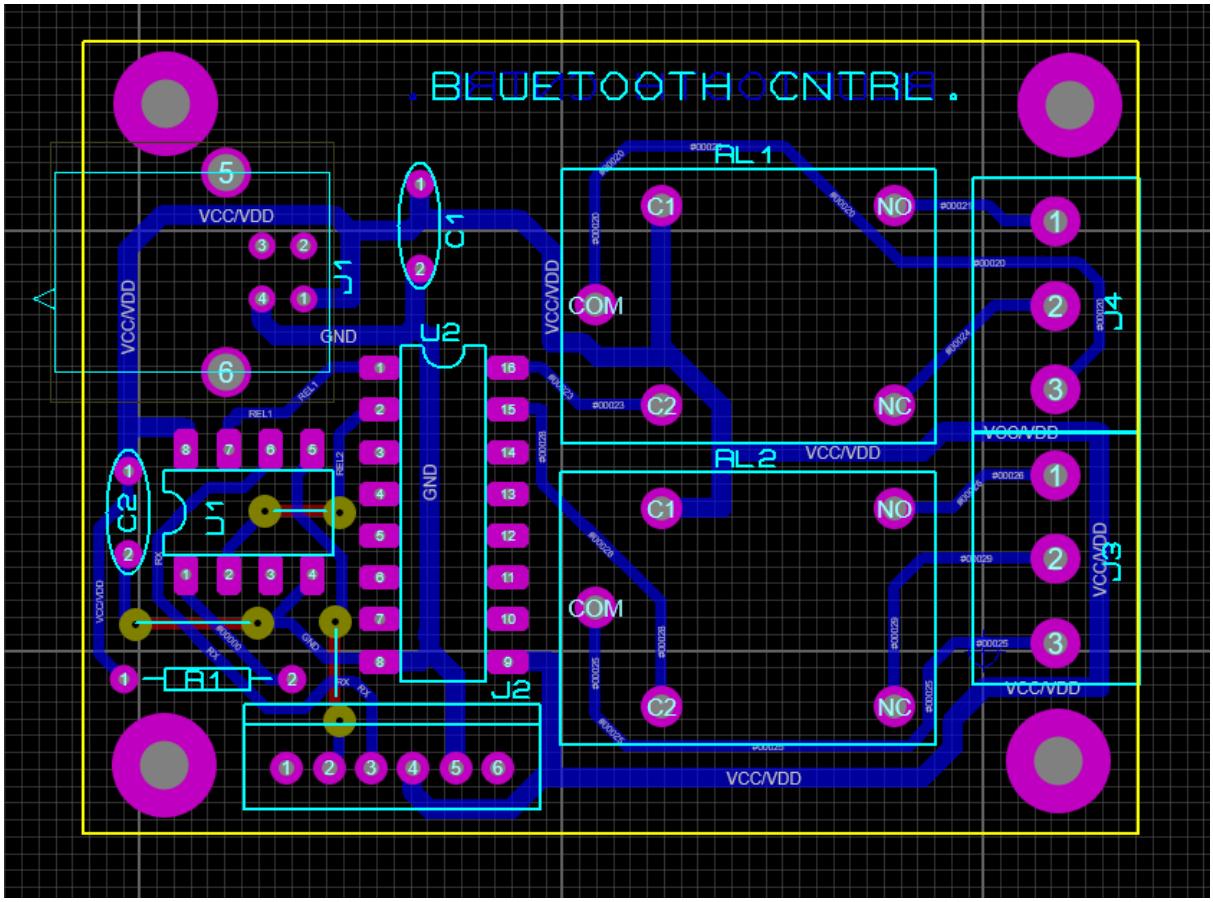


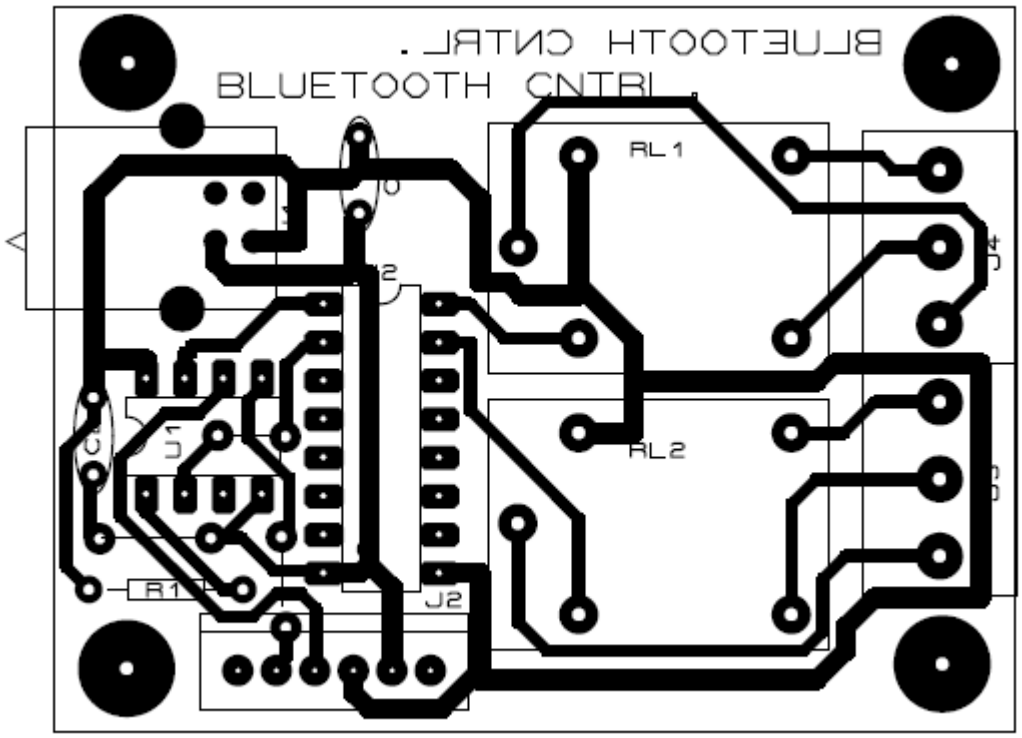


9. Mark jumper on the silk screen.



10. Finish PCB layout





Result

Single sided PCB for the given schematic is prepared.

Lab in charge	**Signature of the lab incharge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

Exp: 9	Custom component Design	Date :

Time : 60 minutes

Problem Statement: Develop custom component for TDA2003a referring to datasheet.

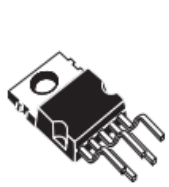
TDA2003A

10 W car radio audio amplifier

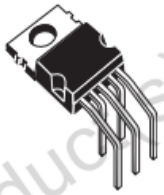
Datasheet – production data

Features

- Improved performance over the TDA2002 (pin-to-pin compatible)
- Very low number of external components
- Ease of assembly
- Cost and space savings



Pentawatt (vertical)



Pentawatt (horizontal)

Description

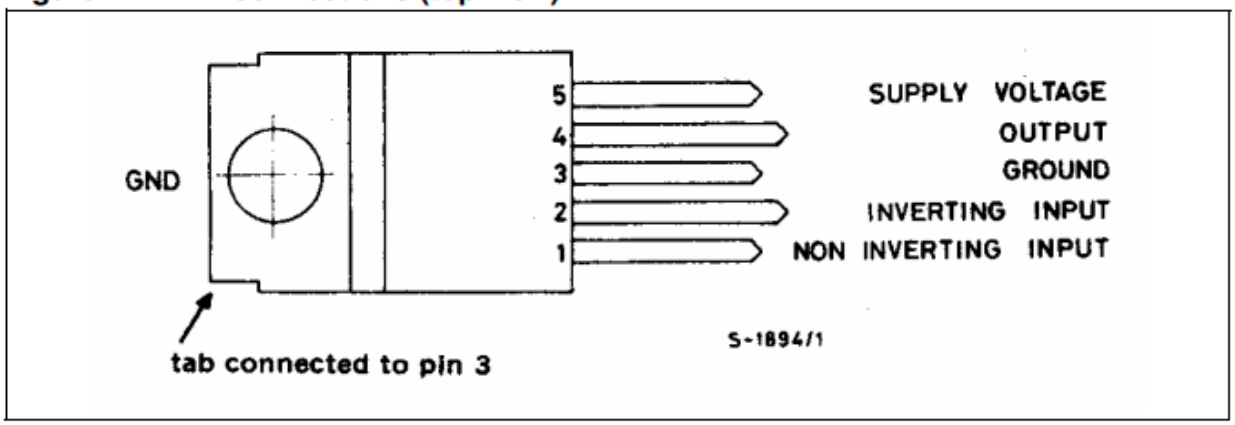
The TDA2003A is capable of providing a high output current (up to 3.5 A) with very low harmonic and crossover distortion.

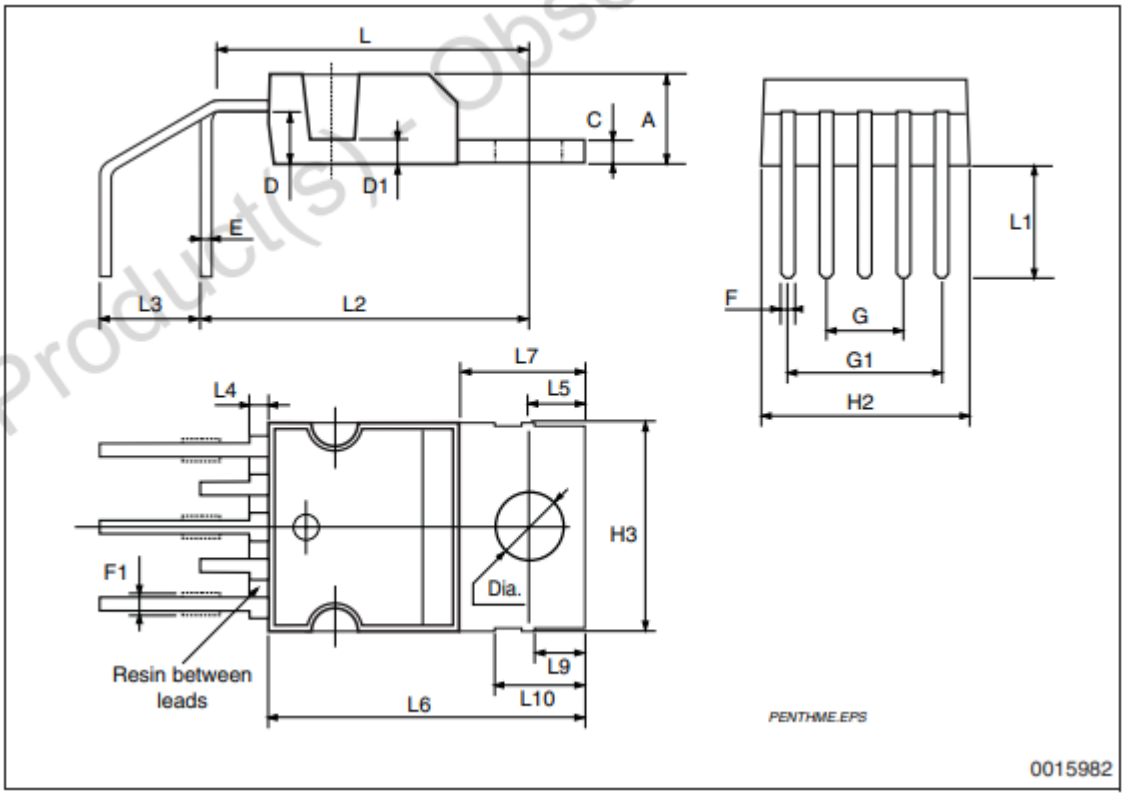
Completely safe operation is guaranteed due to DC and AC short-circuit protection between all pins and ground, a thermal limiting circuit, load dump voltage surge protection up to 40 V and protection diodes in case of accidental open ground.

Table 1. Device summary

Order code	Package	Packing
TDA2003AV	Pentawatt (vertical)	Tube
TDA2003AH	Pentawatt (horizontal)	Tube

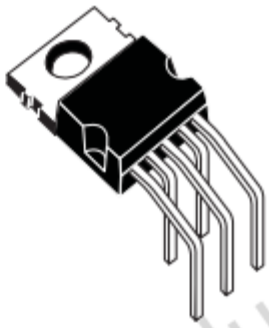
Figure 4. Pin connections (top view)





DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.80			0.188
C			1.37			0.054
D	2.40		2.80	0.094		0.11
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.80		1.05	0.031		0.041
F1	1.00		1.40	0.039		0.055
G	3.20	3.40	3.60	0.126	0.134	0.142
G1	6.60	6.80	7.00	0.260	0.267	0.275
H2			10.40			0.41
H3	10.05		10.40	0.395		0.409
L	14.20		15.00	0.56		0.59
L1	5.70		6.20	0.224		0.244
L2	14.60		15.20	0.574		0.598
L3	3.50		4.10	0.137		.161
L4			1.29			0.05
L5	2.60		3.00	0.102		0.118
L6	15.10		15.80	0.594		0.622
L7	6.00		6.60	0.236		0.260
L9	2.10		2.70	0.083		0.106
L10	4.30		4.80	0.170		0.189
DIA	3.65		3.85	0.143		0.151

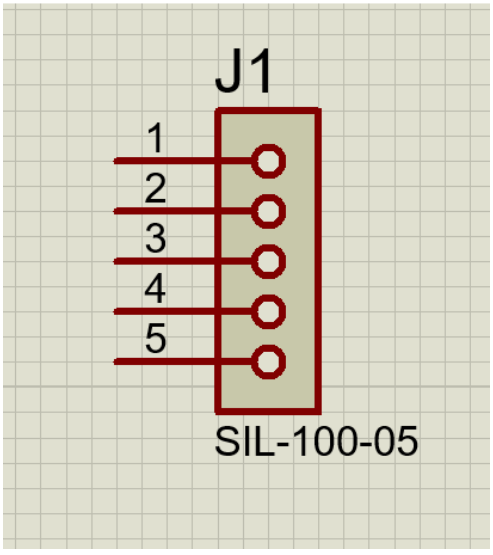
OUTLINE AND MECHANICAL DATA



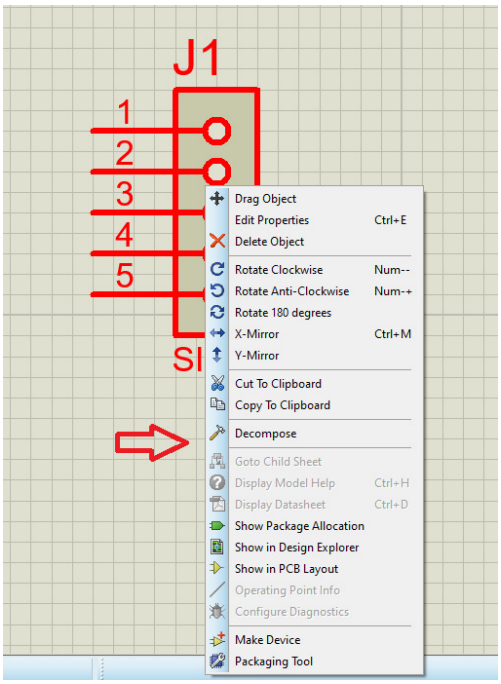
Pentawatt H

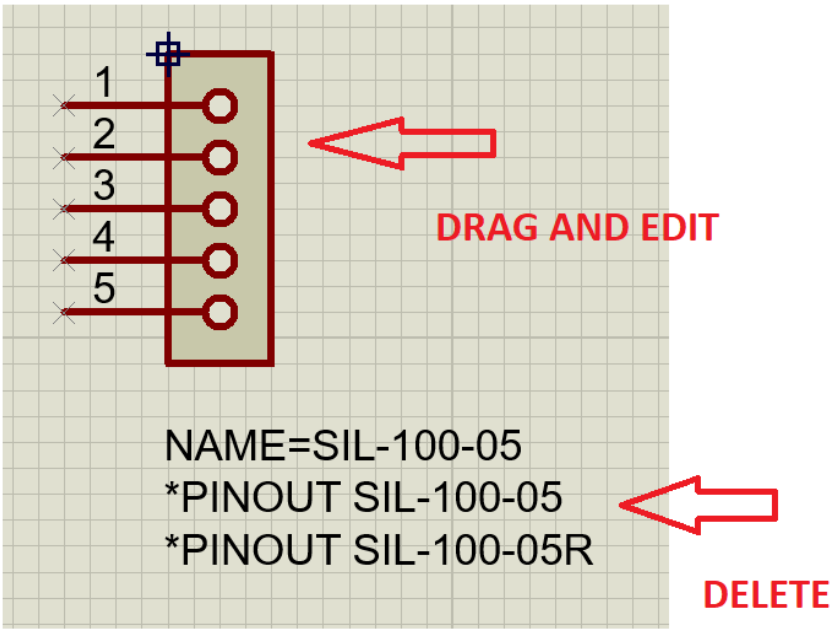
Procedure:

1. **Open Schematic tab and select a component which is in close match with the required component.**

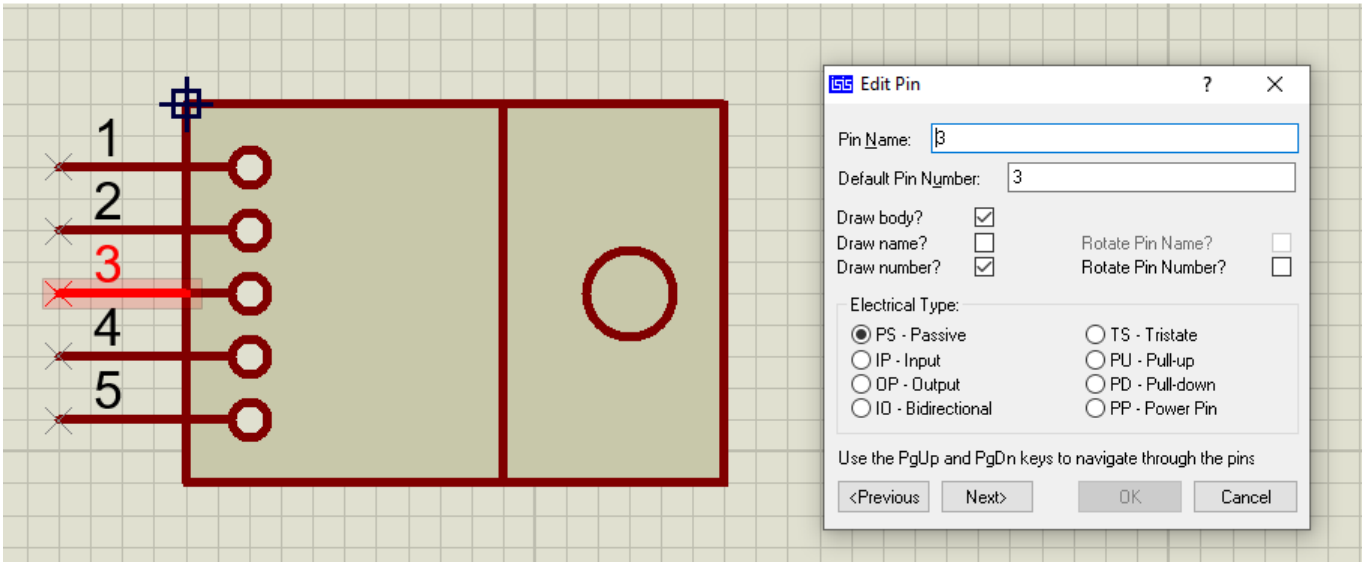


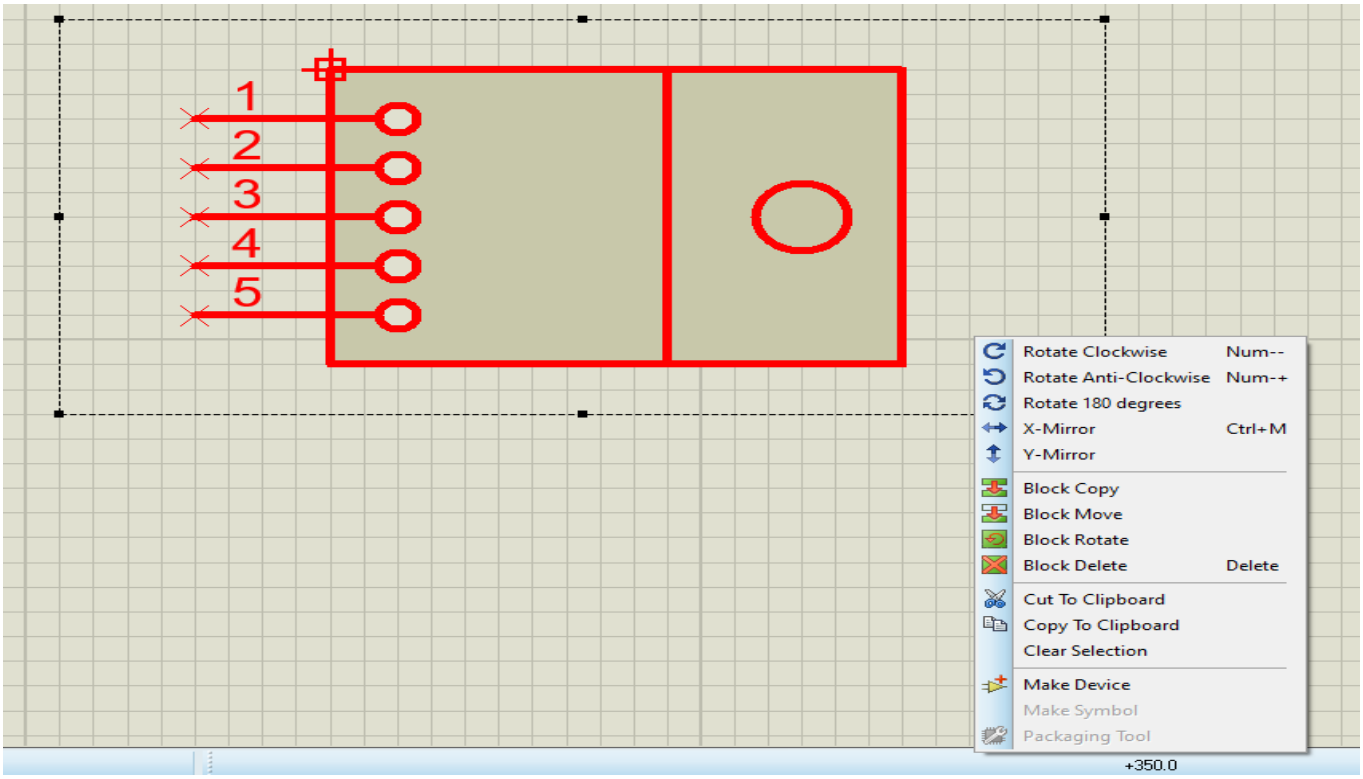
2. Right click and select decompose

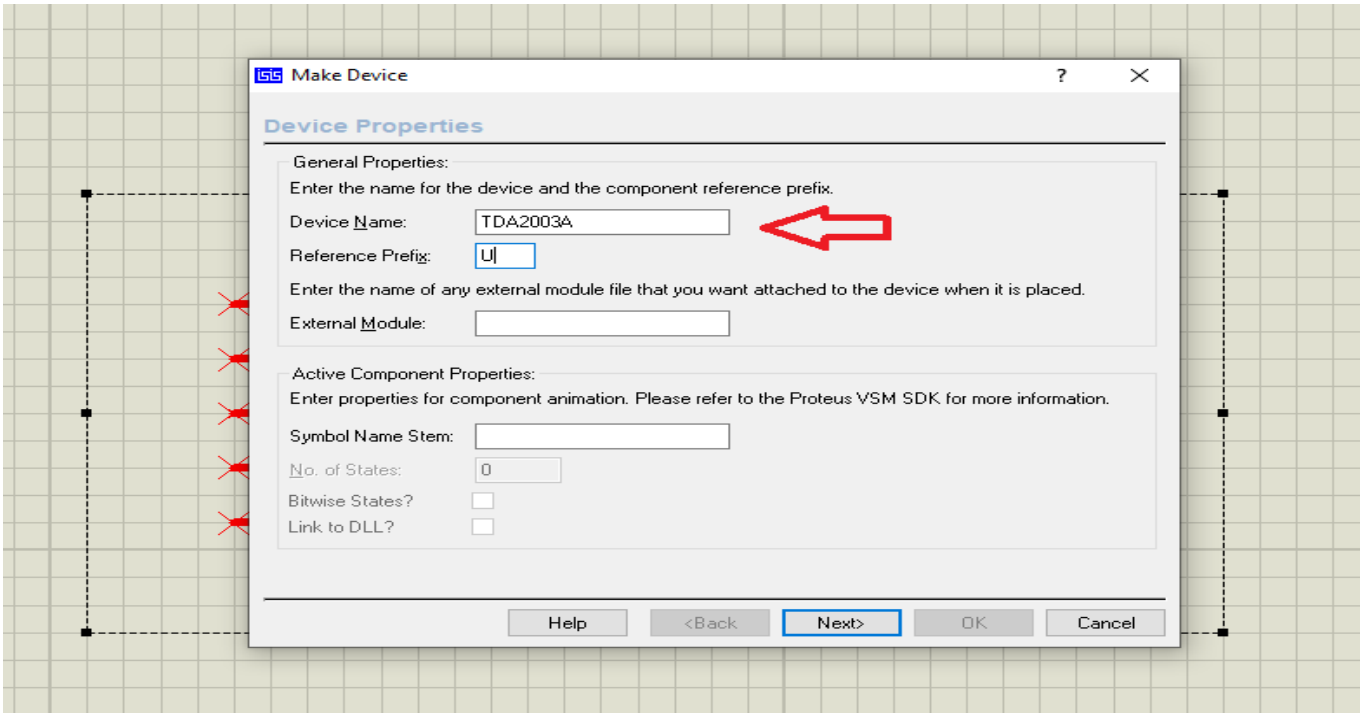


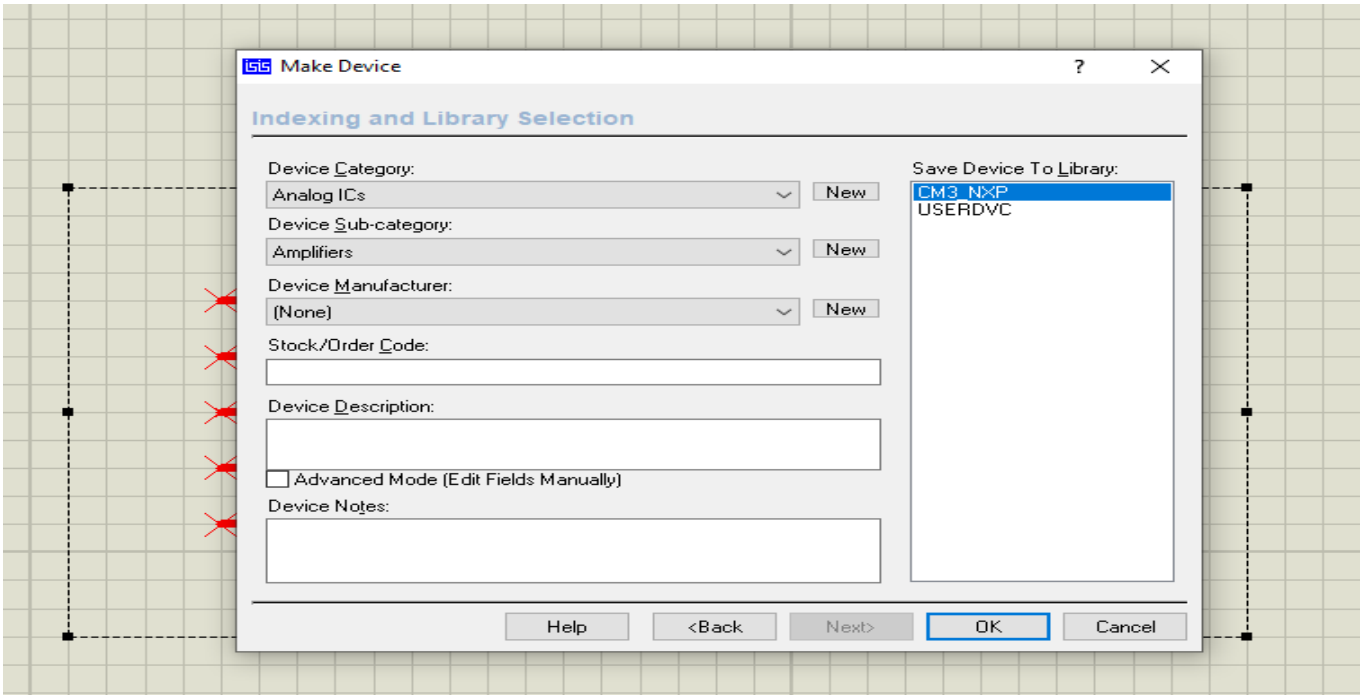


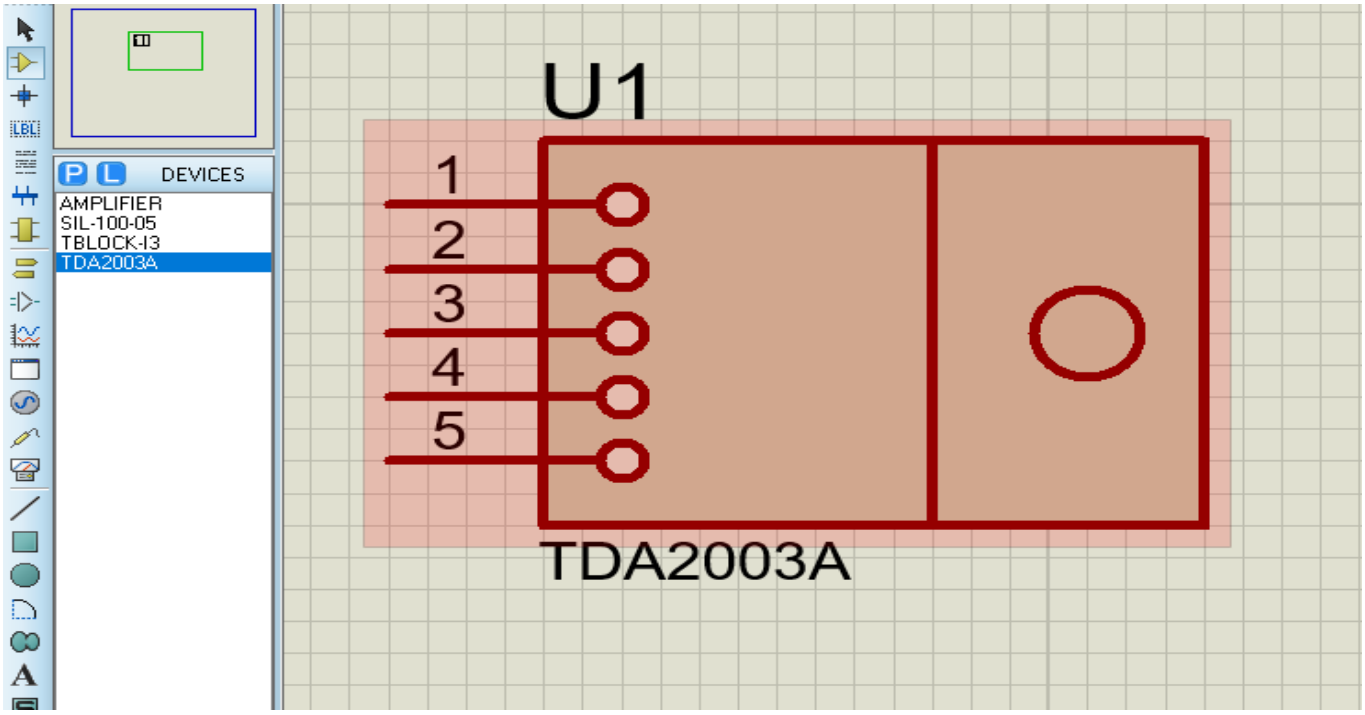
3. Edit component as below




1
2
3
4
5
Rotate Clockwise Num--
Rotate Anti-Clockwise Num-+
Rotate 180 degrees
X-Mirror Ctrl+M
Y-Mirror
Block Copy
Block Move
Block Rotate
Block Delete Delete
Cut To Clipboard
Copy To Clipboard
Clear Selection
Make Device
Make Symbol
Packaging Tool
+350.0


Make Device
Device Properties
General Properties:
Enter the name for the device and the component reference prefix.
Device Name: TDA2003A
Reference Prefix: U
Enter the name of any external module file that you want attached to the device when it is placed.
External Module:
Active Component Properties:
Enter properties for component animation. Please refer to the Proteus VSM SDK for more information.
Symbol Name Stem:
No. of States: 0
Bitwise States?
Link to DLL?
Help
<Back
Next>
OK
Cancel


Make Device
Indexing and Library Selection
Device Category:
Analog ICs
New
Device Sub-category:
Amplifiers
New
Device Manufacturer:
(None)
New
Stock/Order Code:
Device Description:
Advanced Mode (Edit Fields Manually)
Device Notes:
Save Device To Library:
CM3_NXP
USERDVC
Help
<Back
Next>
OK
Cancel


DEVICES
AMPLIFIER
SIL-100-05
TBLOCK-I3
TDA2003A
U1
1
2
3
4
5
TDA2003A

4. **You will find the custom component in the library**

Custom component for TDA2003A prepared.

Lab in charge	**Signature of the lab incharge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

Exp: 10	Custom Footprint Design	Date :

Time : 60 minutes

Problem Statement: Develop custom footprint for TDA2003a referring to datasheet.

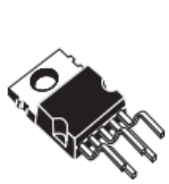
TDA2003A

10 W car radio audio amplifier

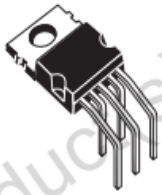
Datasheet – production data

Features

- Improved performance over the TDA2002 (pin-to-pin compatible)
- Very low number of external components
- Ease of assembly
- Cost and space savings



Pentawatt (vertical)



Pentawatt (horizontal)

Description

The TDA2003A is capable of providing a high output current (up to 3.5 A) with very low harmonic and crossover distortion.

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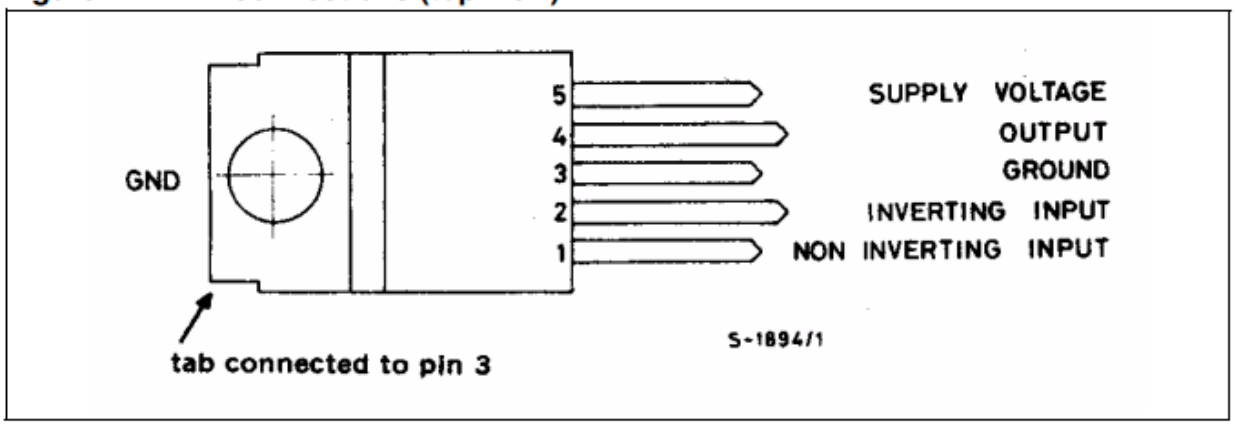
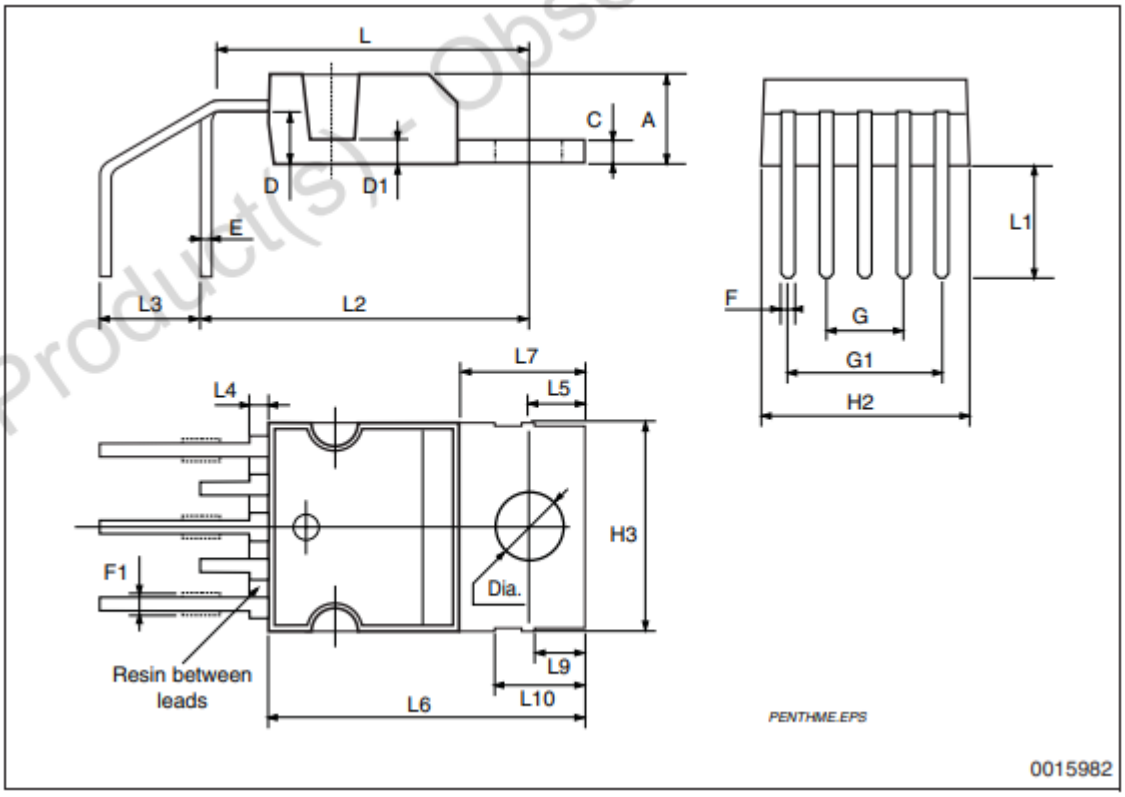
Table 1. Device summary

Order code	Package	Packing
TDA2003AV	Pentawatt (vertical)	Tube
TDA2003AH	Pentawatt (horizontal)	Tube

Figure 4. Pin connections (top view)





DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.80			0.188
C			1.37			0.054
D	2.40		2.80	0.094		0.11
D1	1.20		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.80		1.05	0.031		0.041
F1	1.00		1.40	0.039		0.055
G	3.20	3.40	3.60	0.126	0.134	0.142
G1	6.60	6.80	7.00	0.260	0.267	0.275
H2			10.40			0.41
H3	10.05		10.40	0.395		0.409
L	14.20		15.00	0.56		0.59
L1	5.70		6.20	0.224		0.244
L2	14.60		15.20	0.574		0.598
L3	3.50		4.10	0.137		.161
L4			1.29			0.05
L5	2.60		3.00	0.102		0.118
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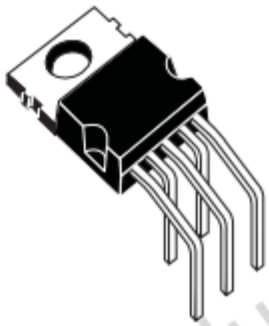
L7	6.00		6.60	0.236		0.260
L9	2.10		2.70	0.083		0.106
L10	4.30		4.80	0.170		0.189
DIA	3.65		3.85	0.143		0.151

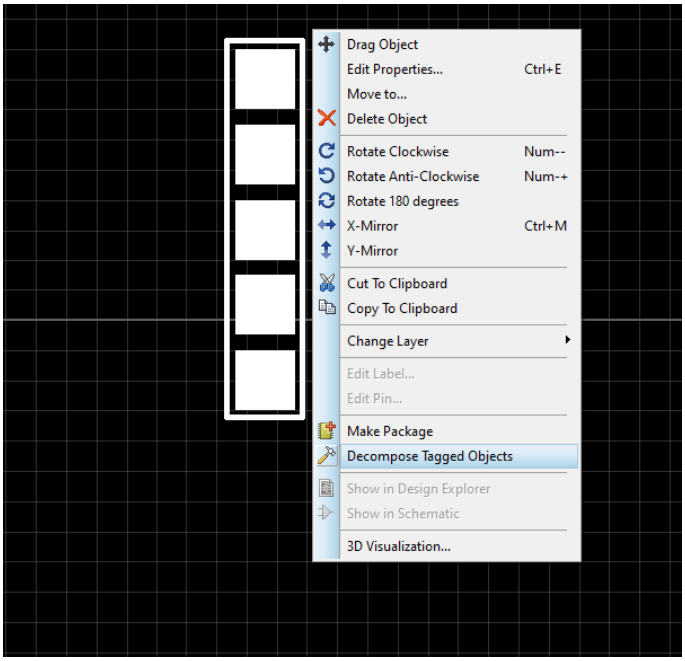
OUTLINE AND MECHANICAL DATA



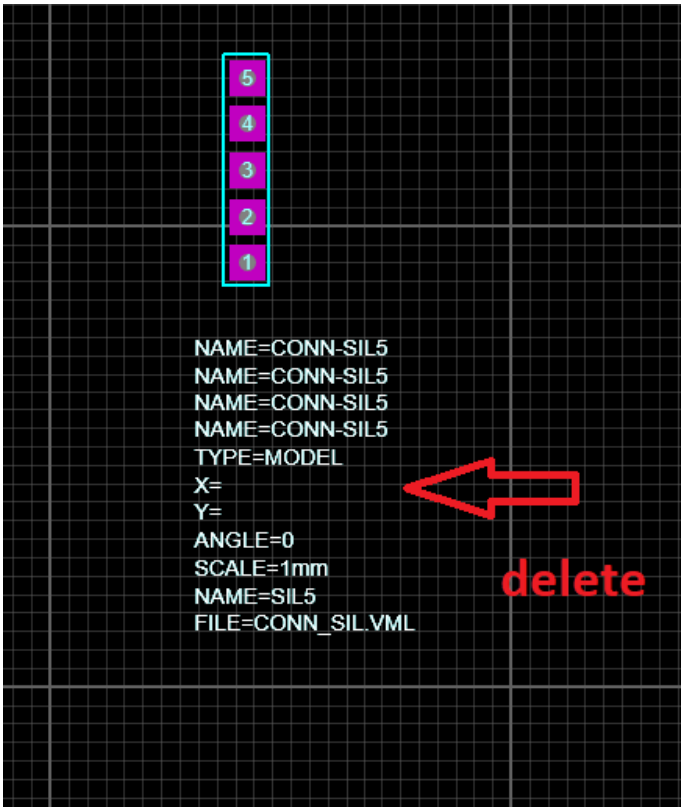
Pentawatt H

Procedure:

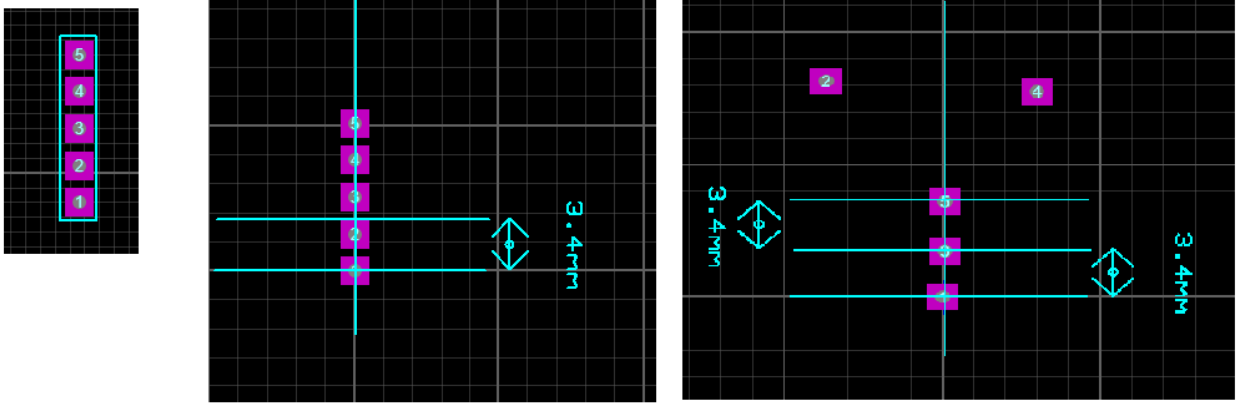
1. **Open PCB lay out tab and select a component which is in close match with the required component.**

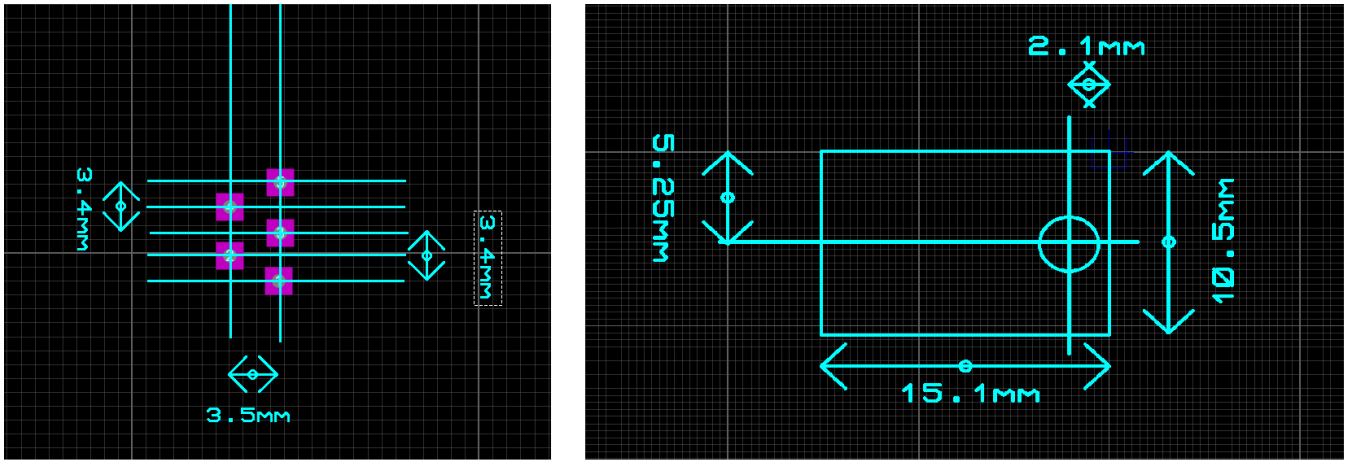


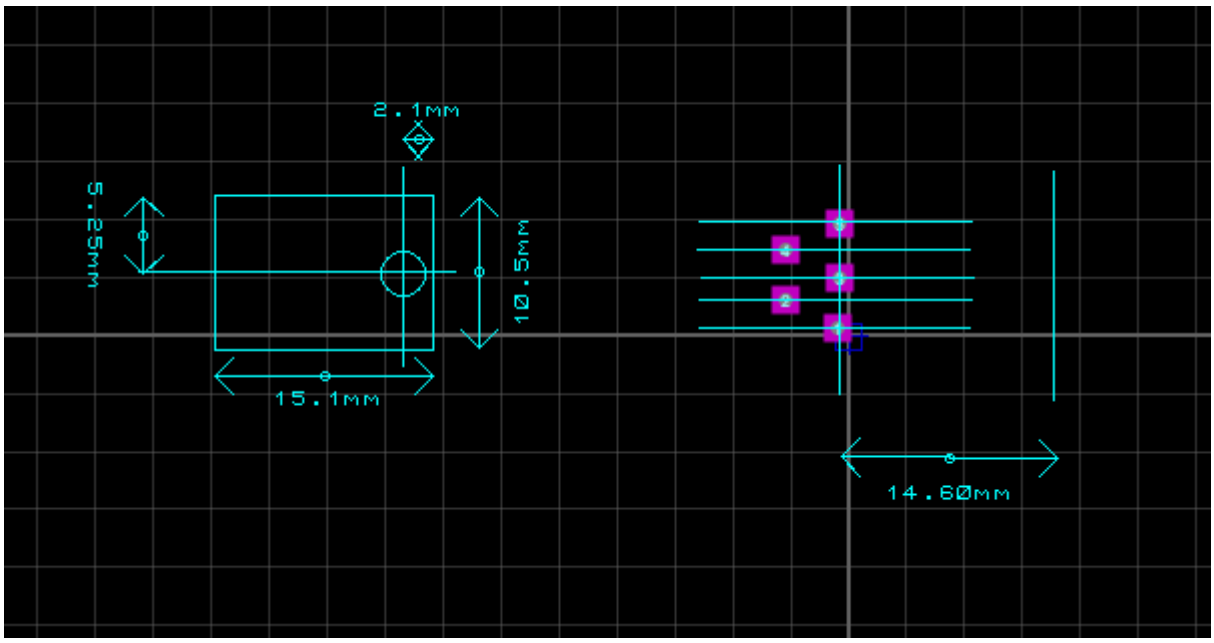
2. **Right click and select decompose**

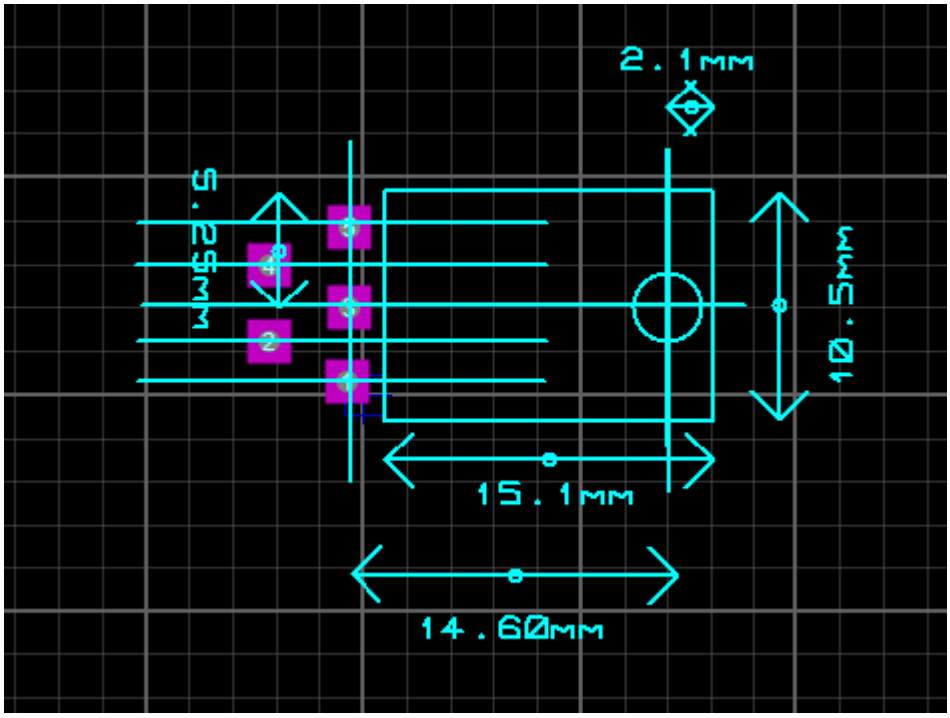


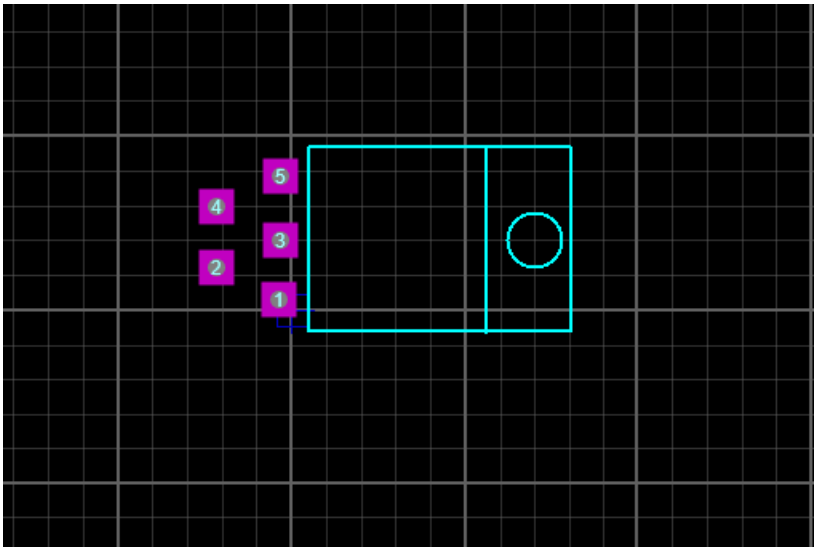
3. Edit component as below



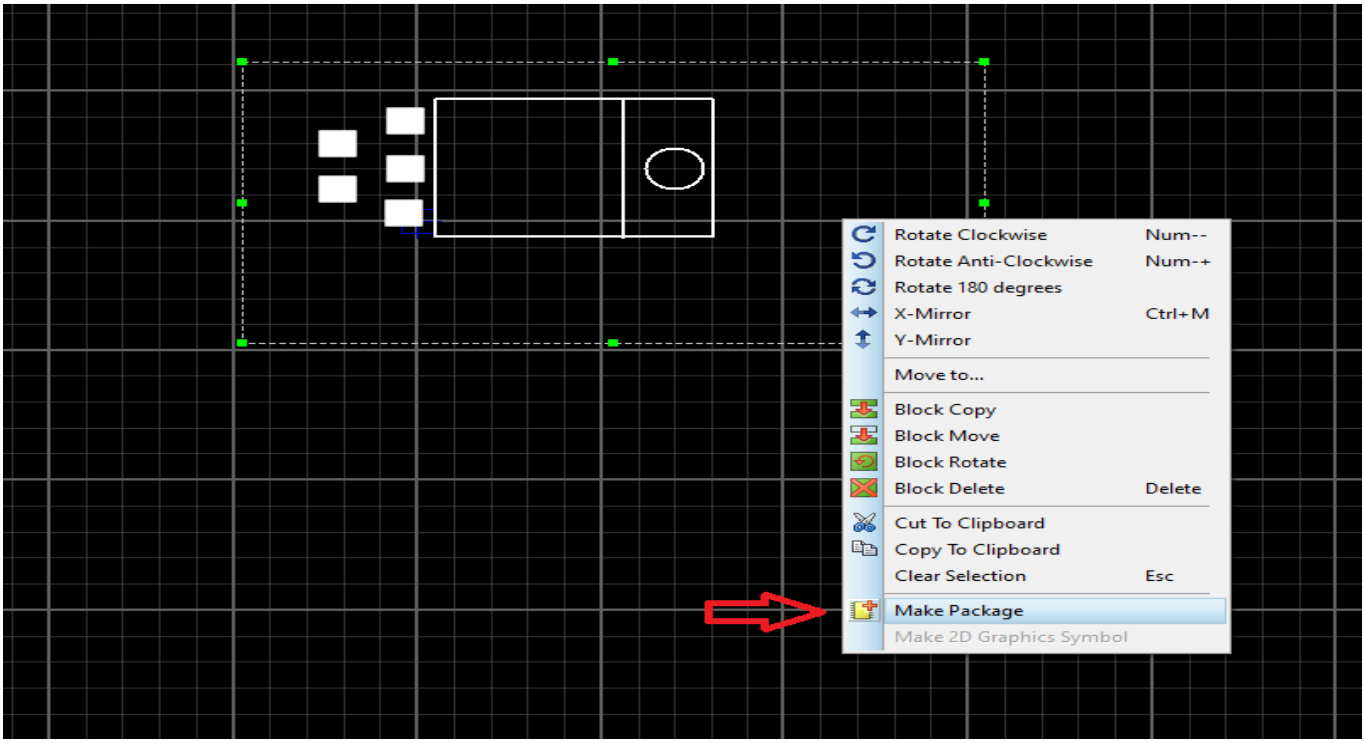


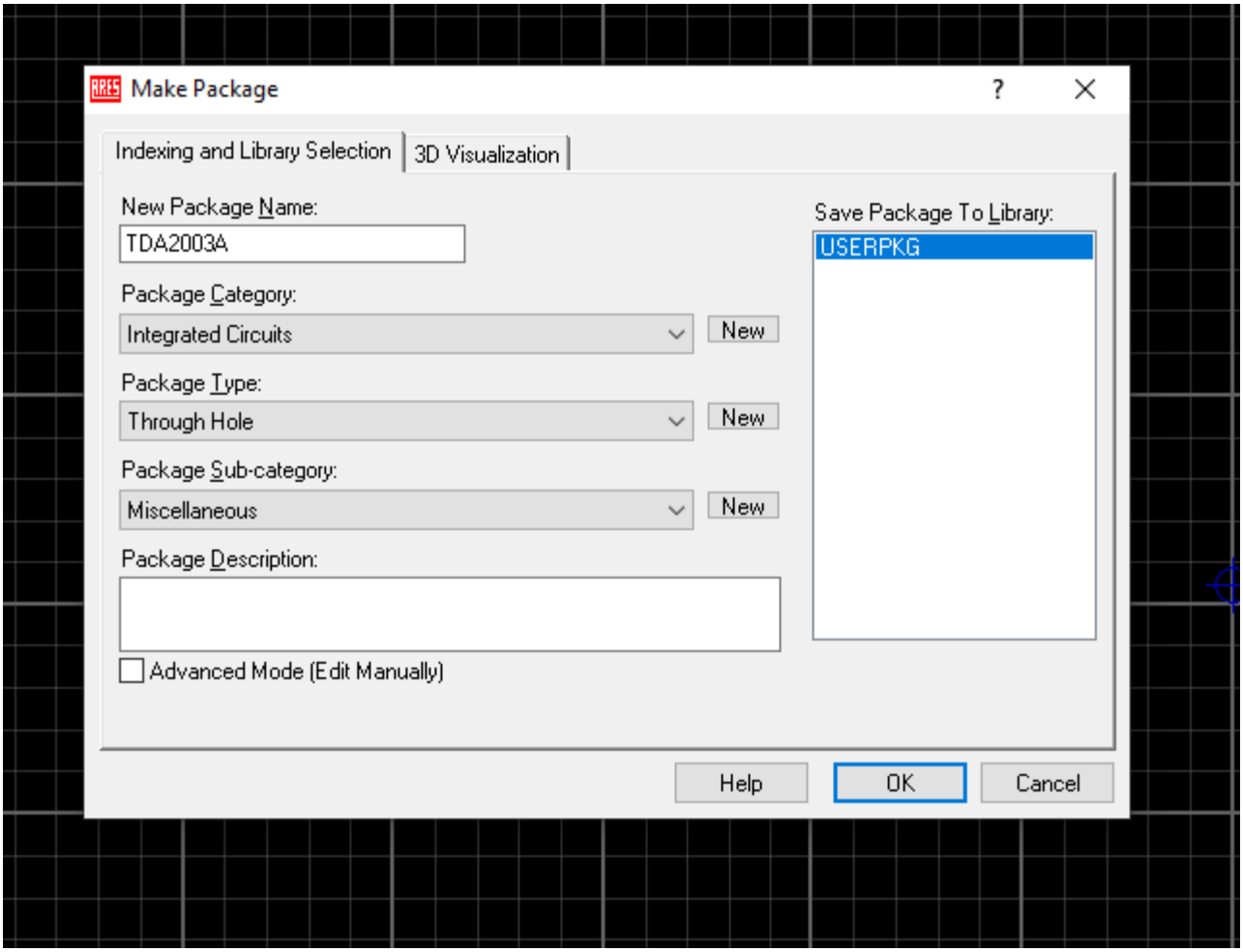

2.1MM
5.25MM
10.5MM
15.1MM
14.60MM


2.1MM
5.25MM
10.5MM
15.1MM
14.60MM

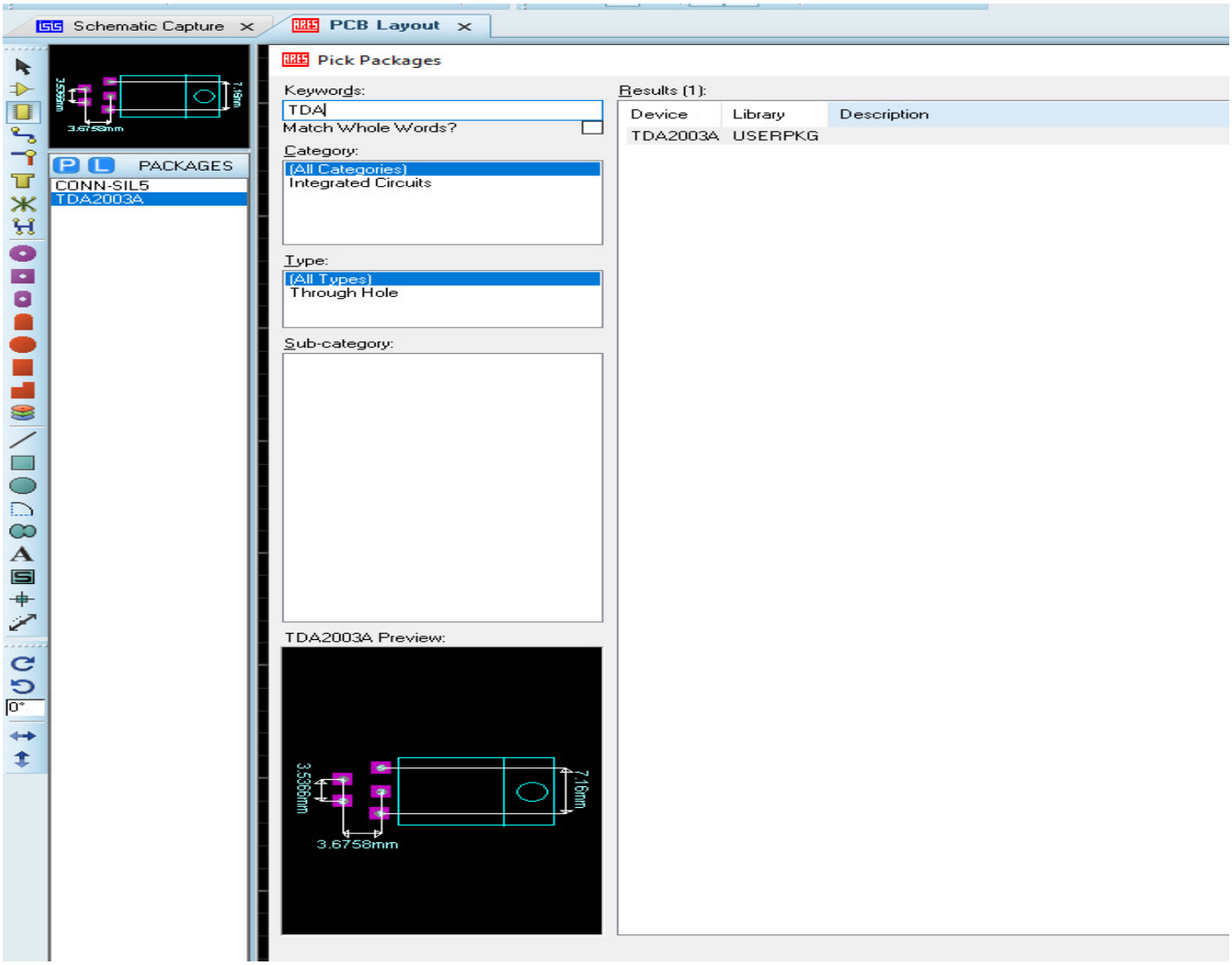


4. Select the whole drawing, right click and select make package




Make Package
Indexing and Library Selection
3D Visualization
New Package Name:
TDA2003A
Package Category:
Integrated Circuits
New
Package Type:
Through Hole
New
Package Sub-category:
Miscellaneous
New
Package Description:
Advanced Mode (Edit Manually)
Save Package To Library:
USERPKG
Help
OK
Cancel

5. The component is ready and available in the library



Custom foot print for TDA2003A prepared.

Lab in charge	Signature of the lab in charge	Date
Readiness to do the experiment		
Completion of the experiment		

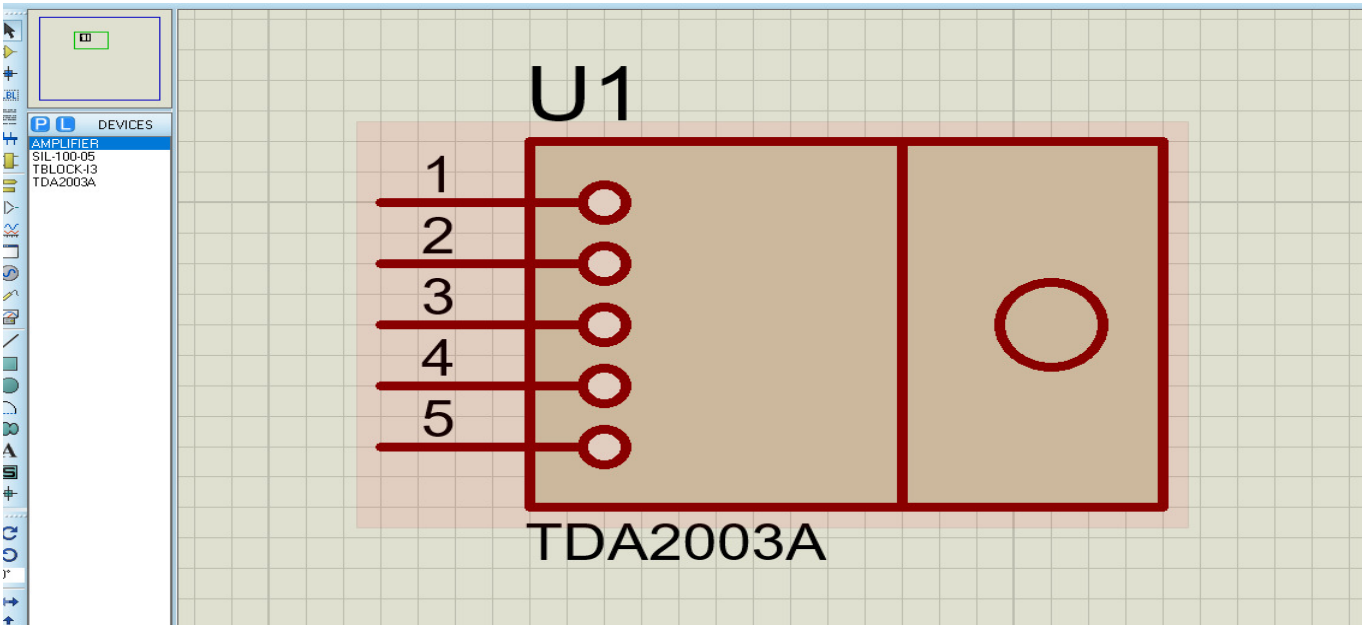
Exp: 11	Linking custom foot print to schematic	Date :

Time : 30 minutes

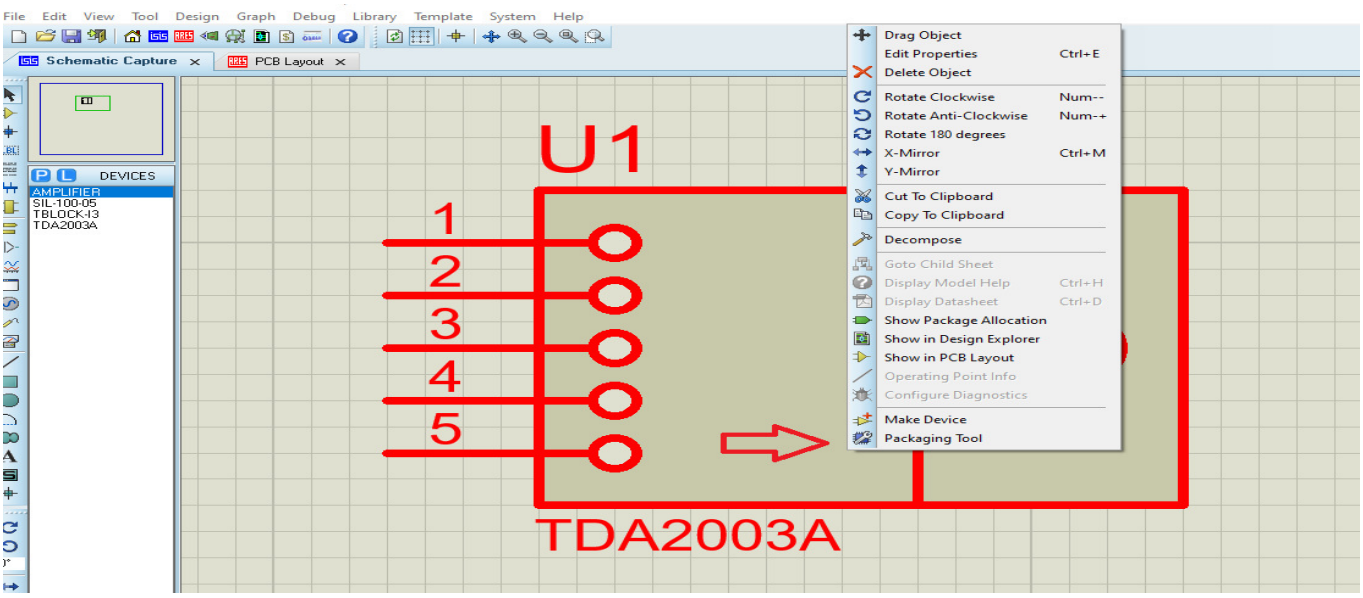
Problem Statement: Link custom foot print designed for experiment 10 to custom component of experiment 8.

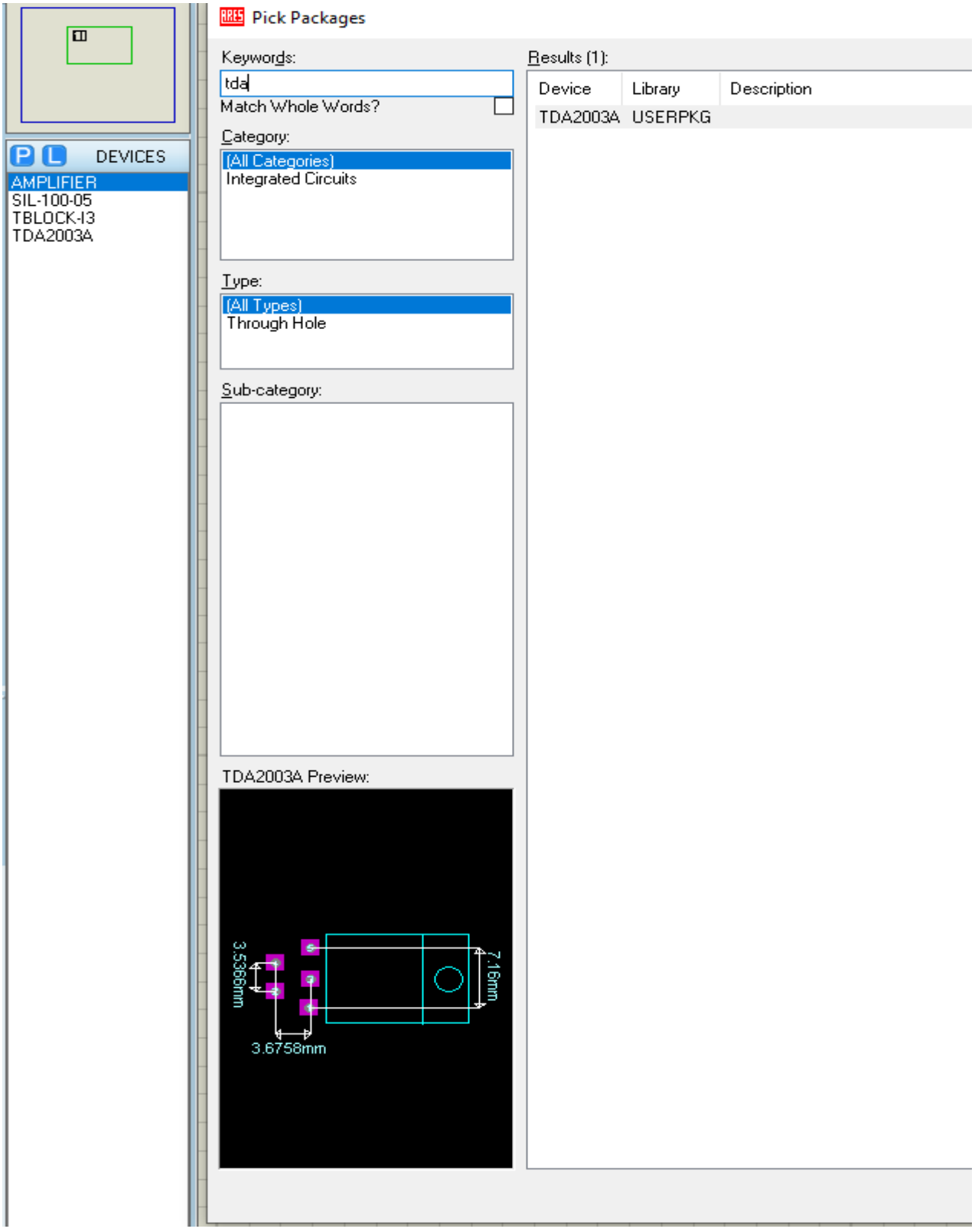
Procedure:

1. **Open schematic tab and select component designed through experiment 8 from the library.**

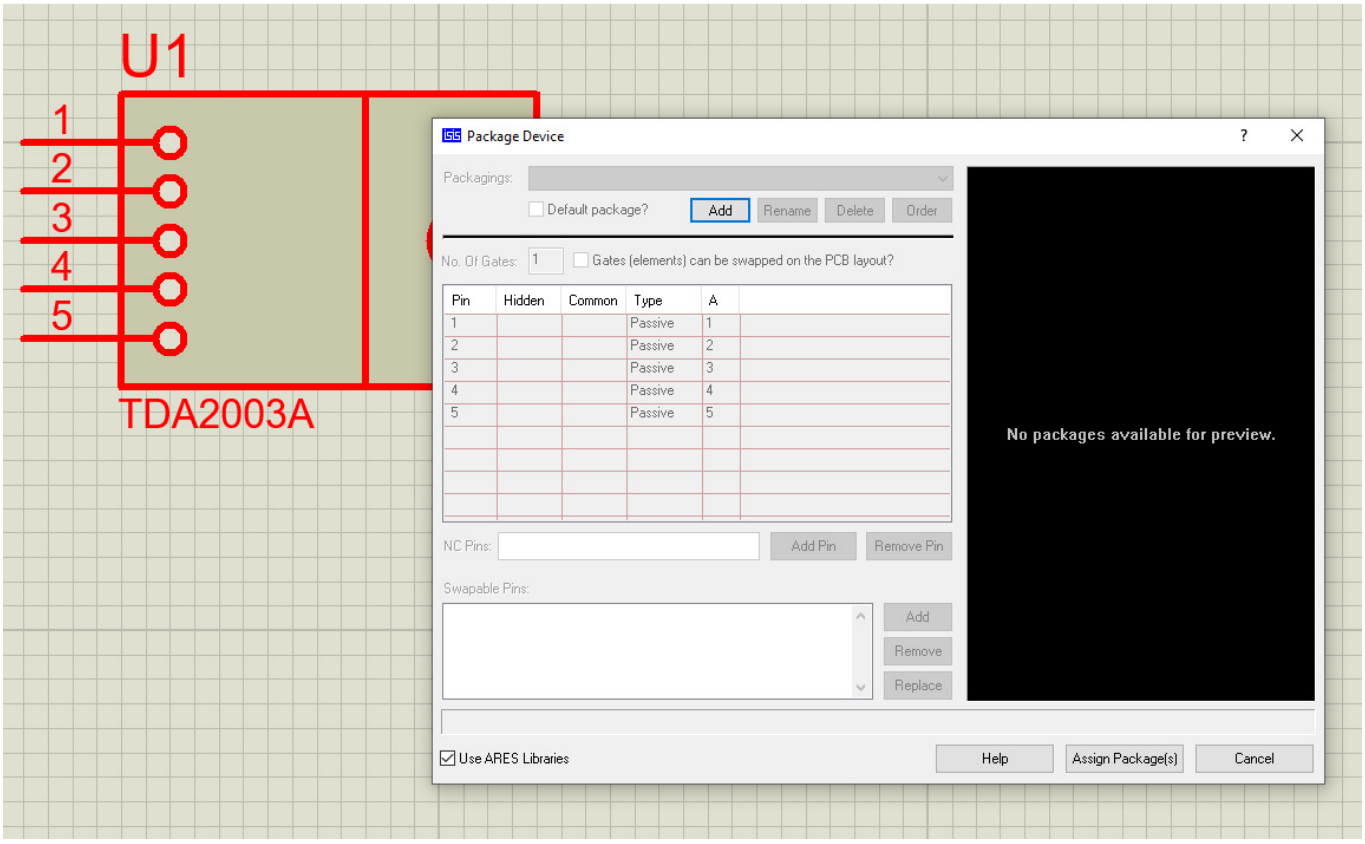


2. **Right click and select Packaging tool.**

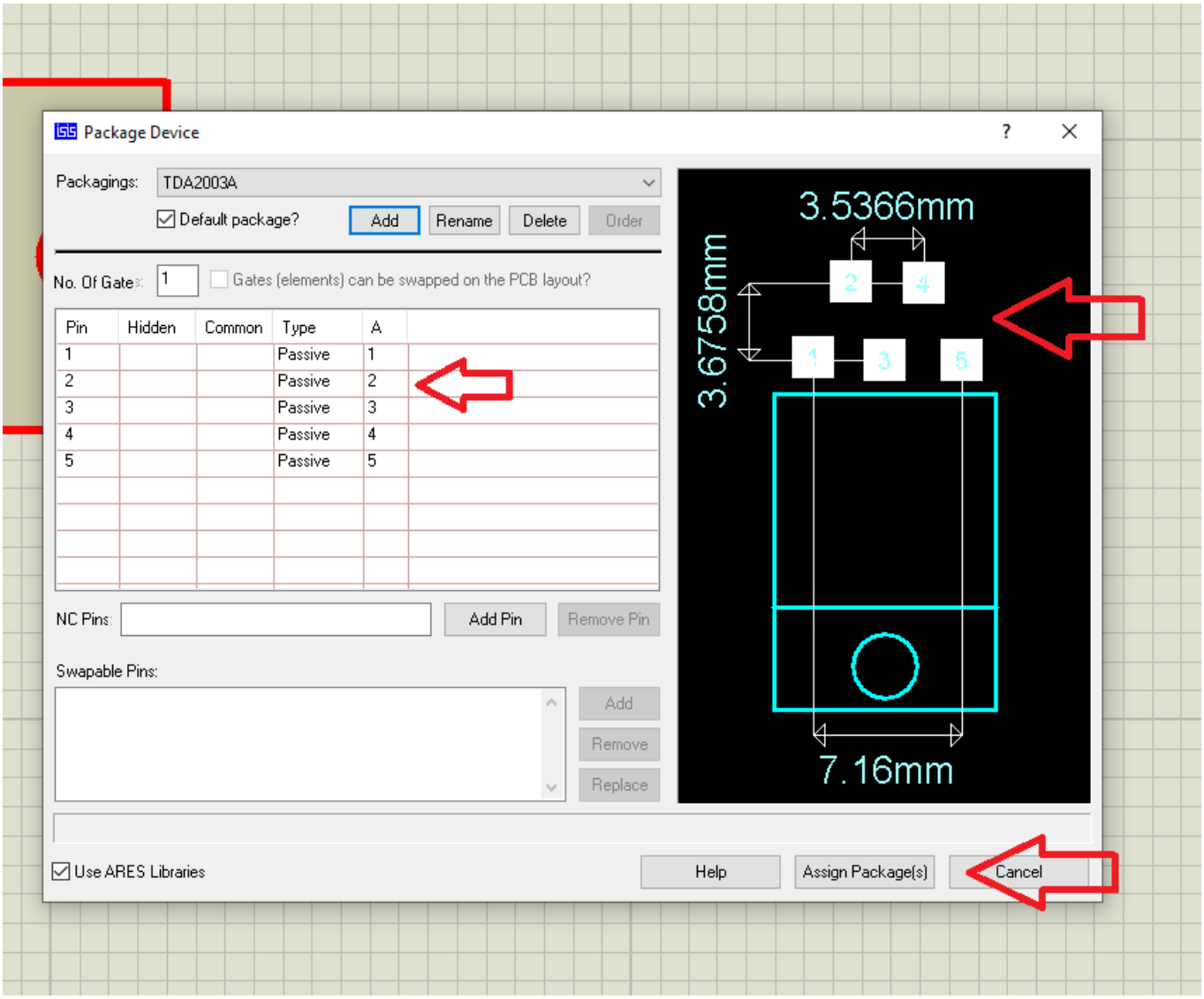



Pick Packages
DEVICES
AMPLIFIER
SIL-100-05
TBLOCK-I3
TDA2003A
Keywords:
tda
Match Whole Words?
Category:
[All Categories]
Integrated Circuits
Type:
[All Types]
Through Hole
Sub-category:
Results (1):
Device
Library
Description
TDA2003A
USERPKG
TDA2003A Preview:
3.5386mm
7.16mm
3.6758mm

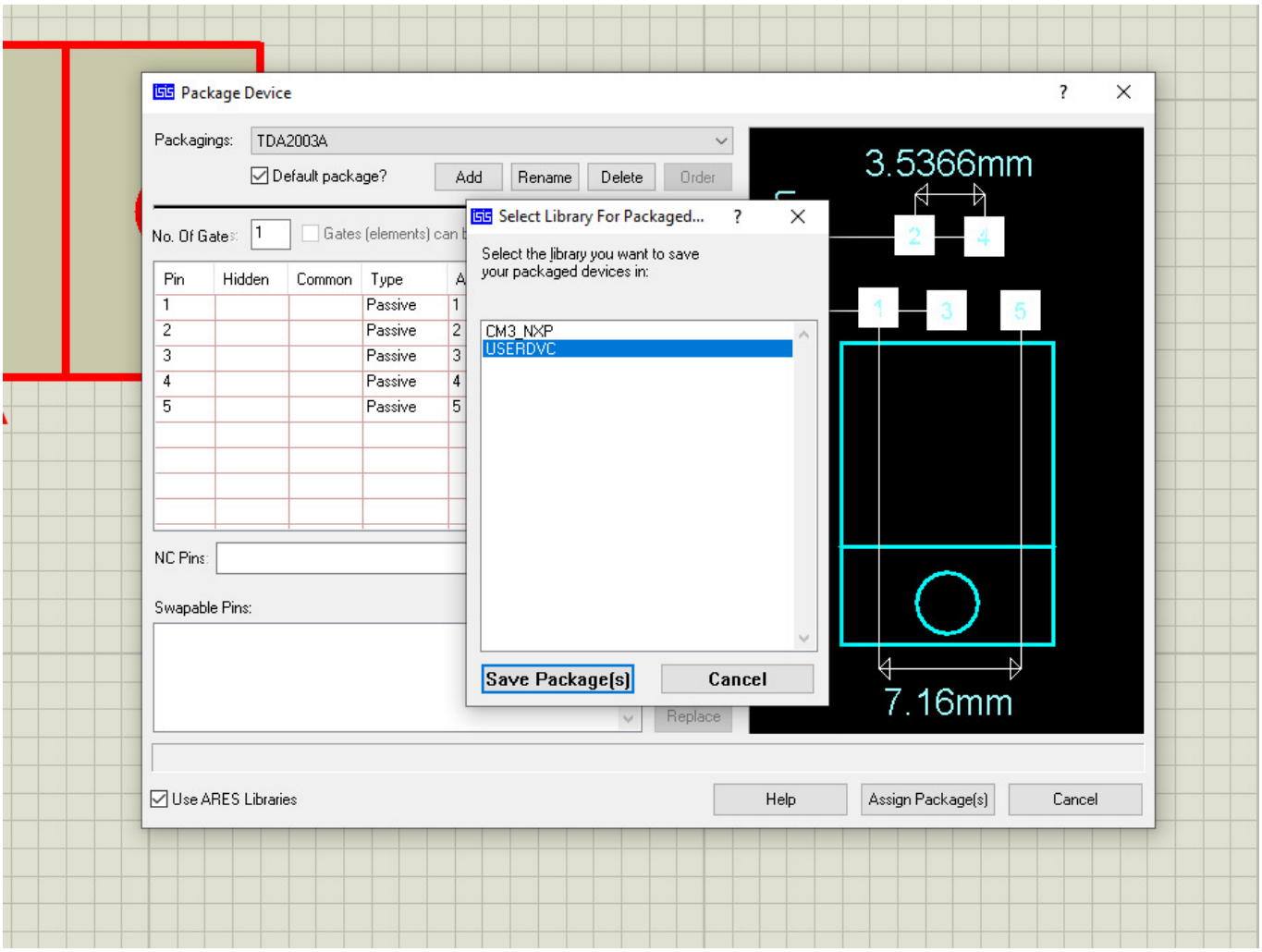
3. Proceed as shown below – click add



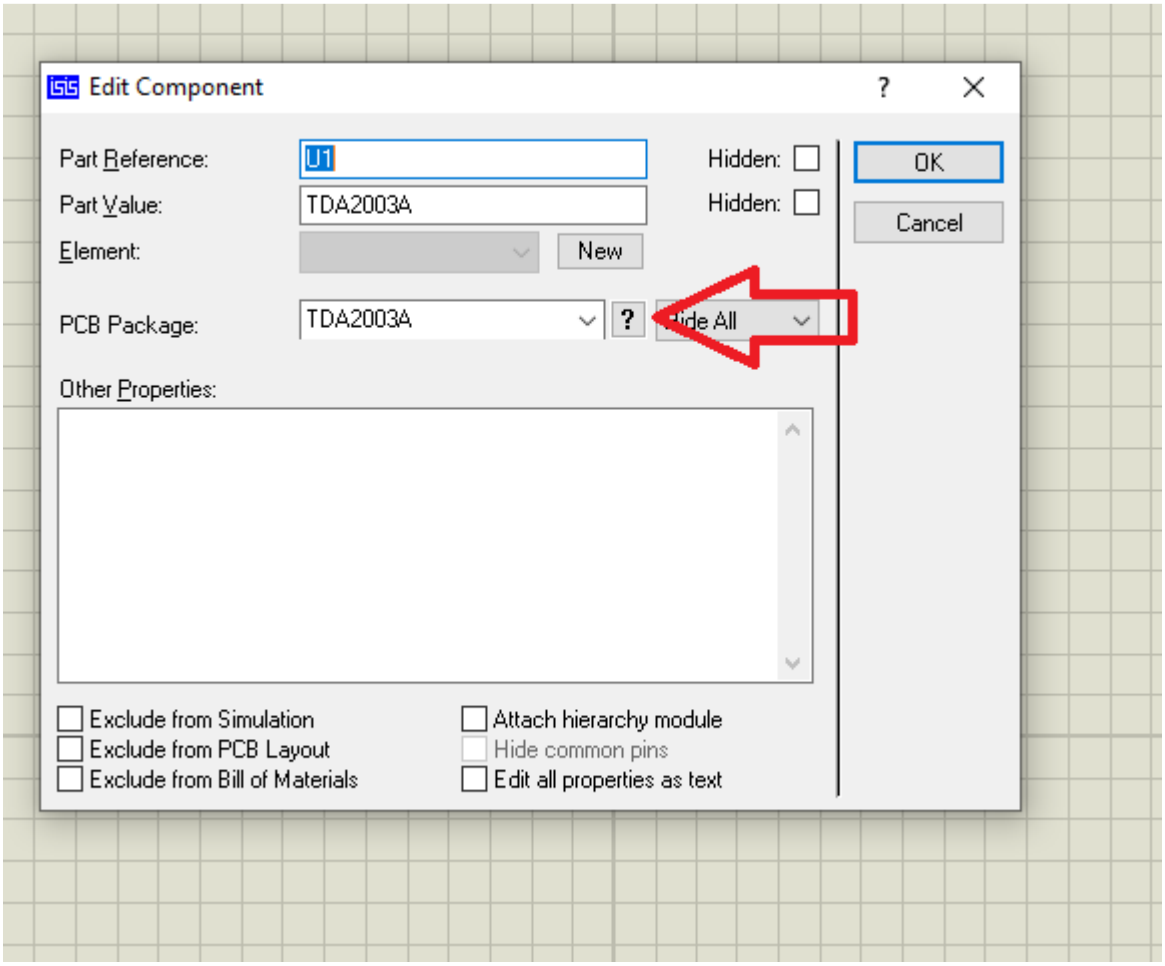
4. Assign Pin numbers by clicking on corresponding pins and click assign package



5. Save package



6. **Double click on the component to select edit component and check whether the component is assigned or browse for the component.**



Now the custom foot print is assigned to the component

Custom foot print is linked to the schematic.

Lab in charge	**Signature of the lab in charge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

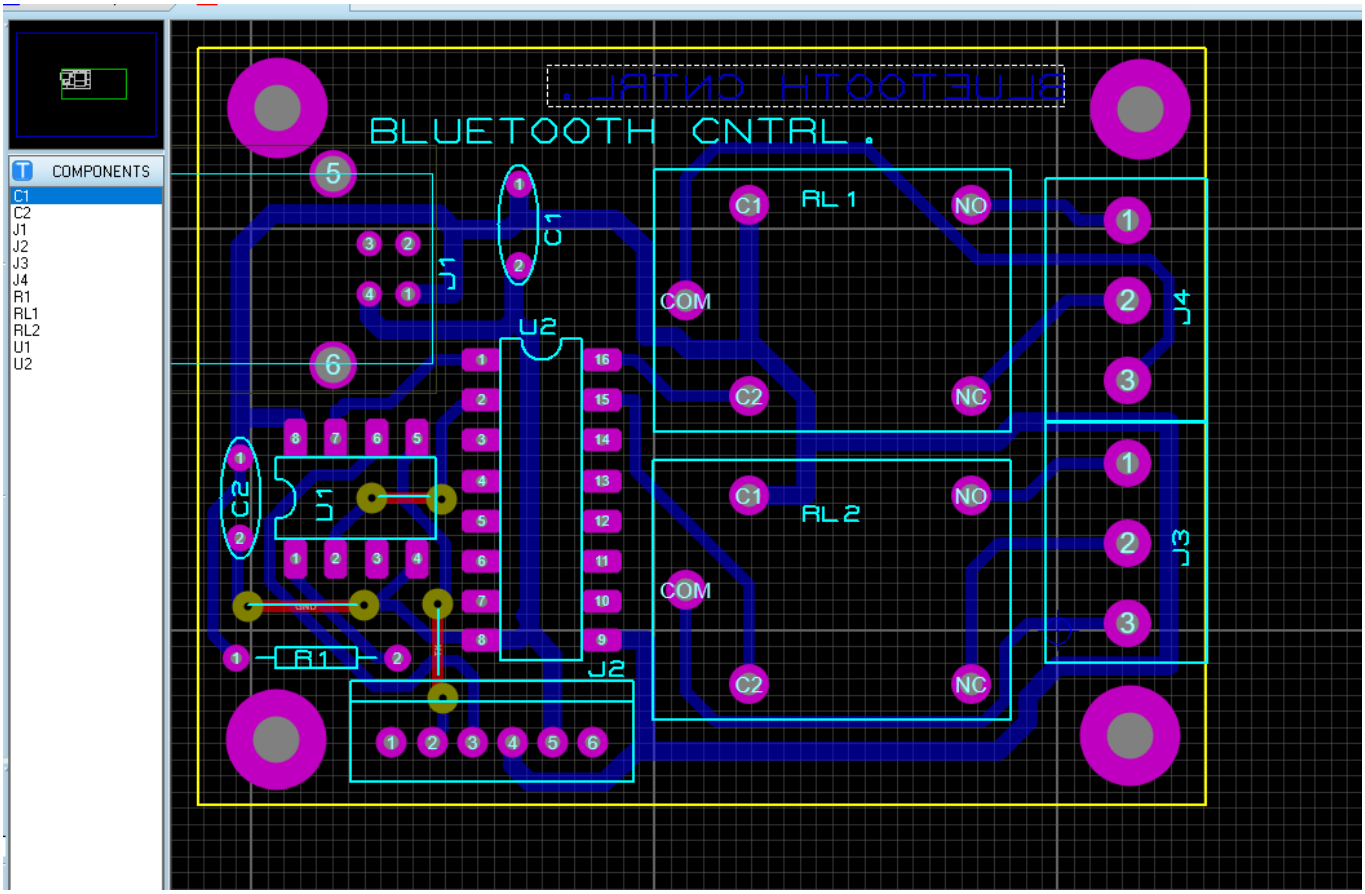
Exp: 12	Gerber file generation	Date :

Time : 30 minutes

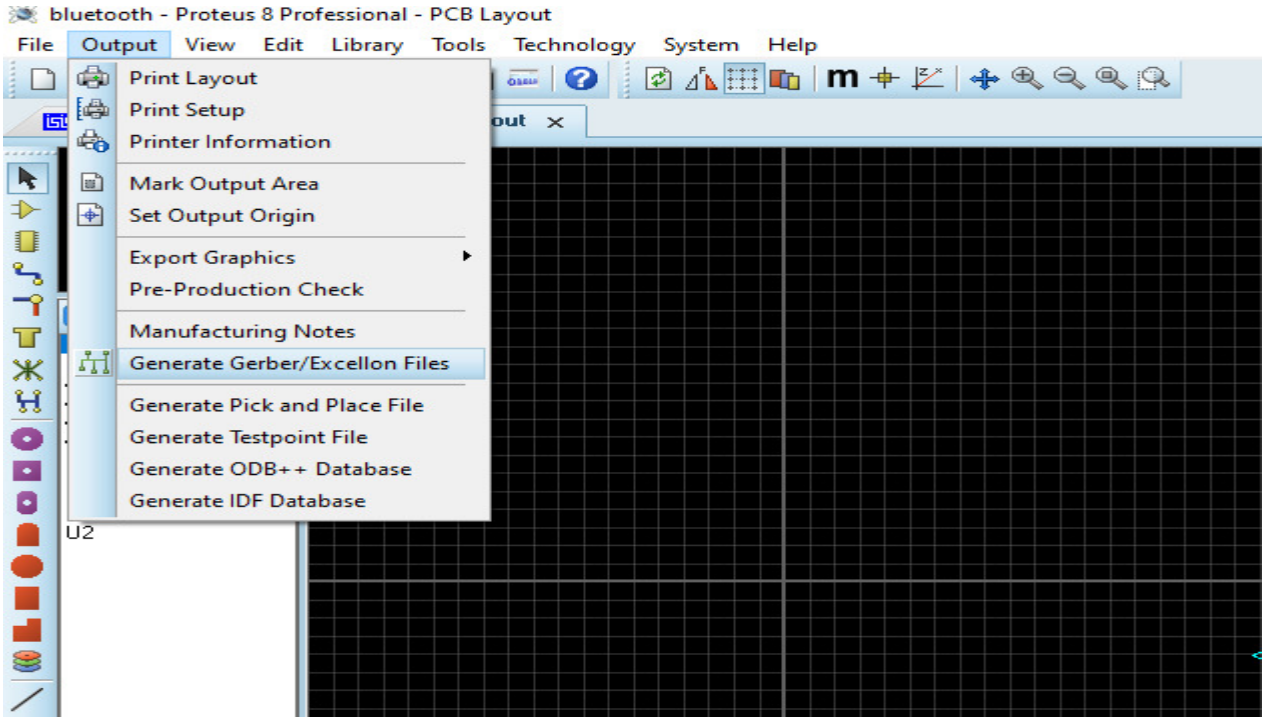
Problem Statement: Perform pre production check and generate Gerber file for a schematic.

Procedure:

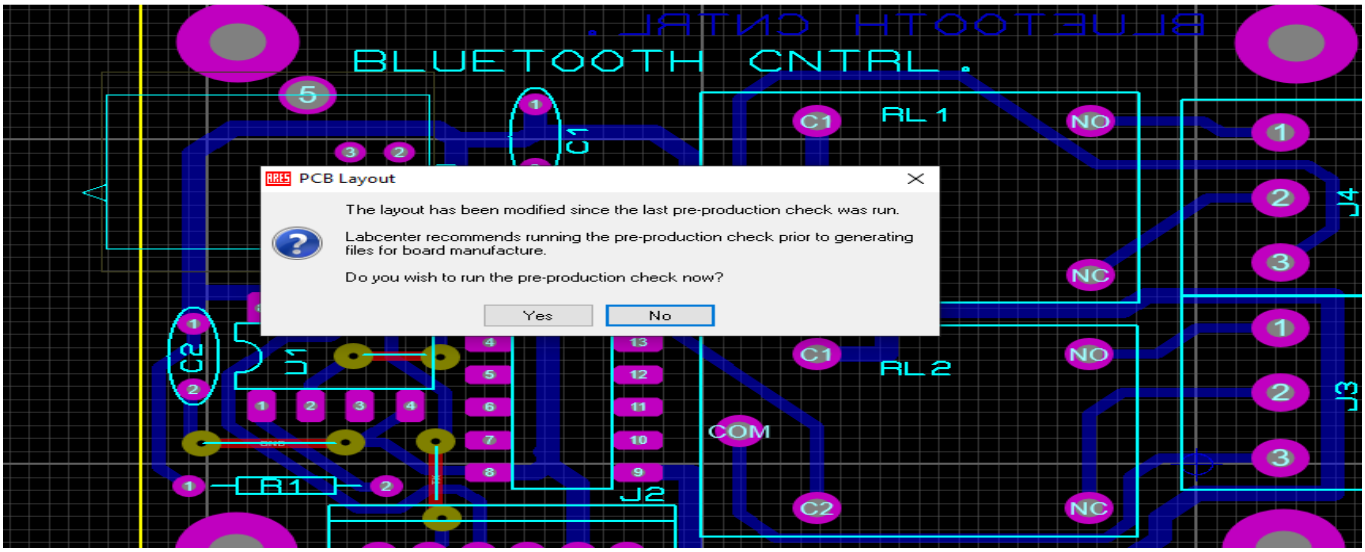
1. **Open the required PCB lay out**



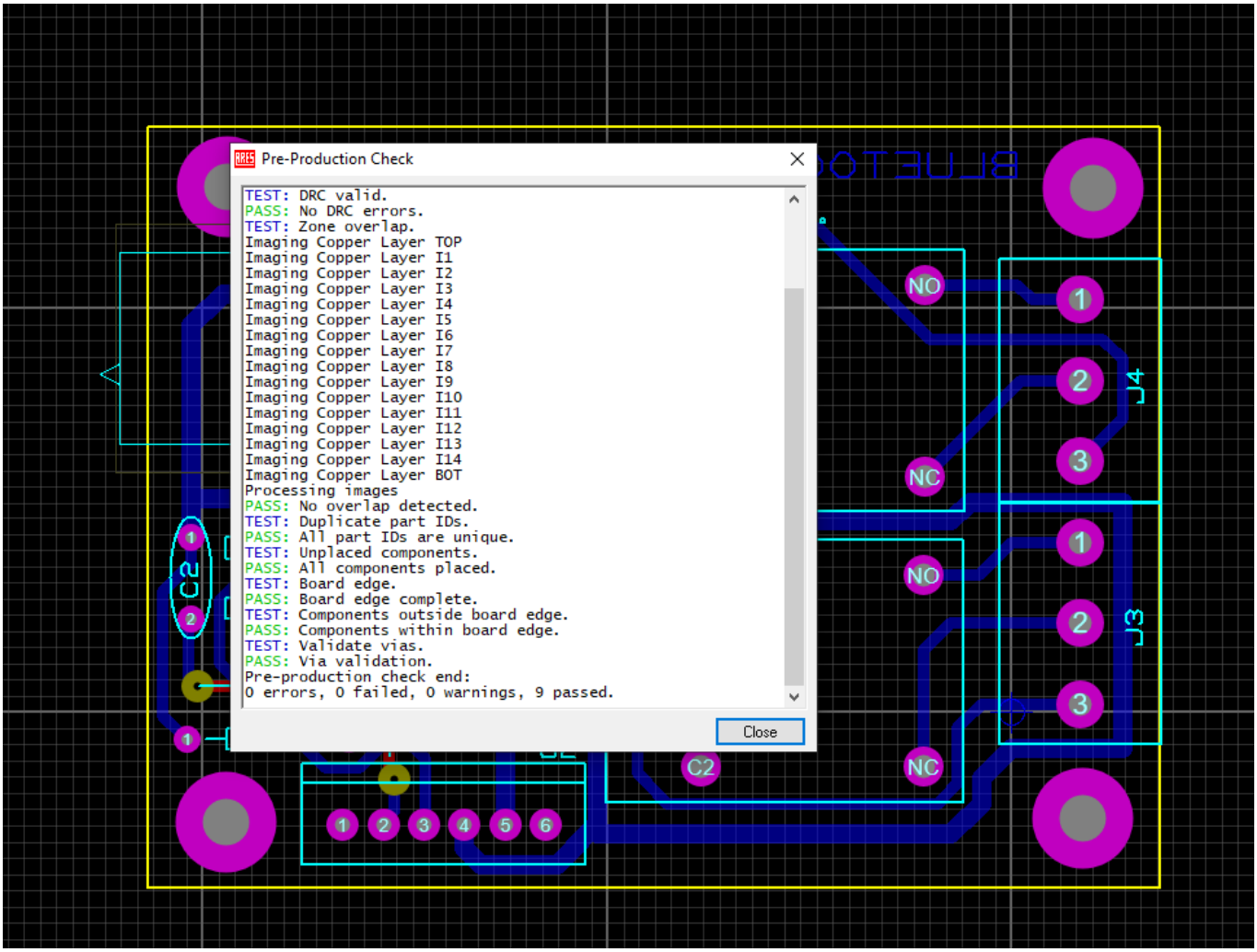
2. Click Generate Gerber/Excellon files.



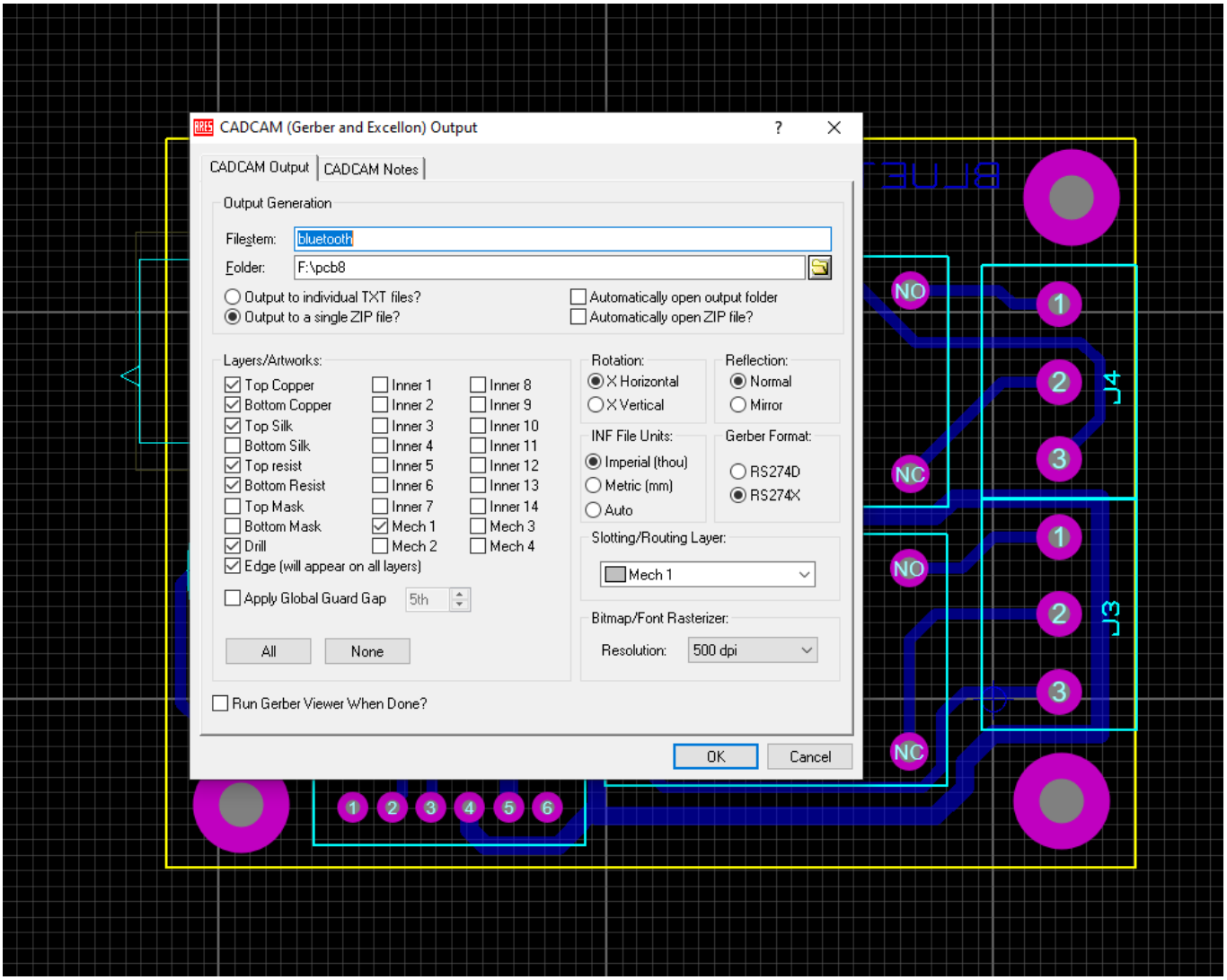
3. Proceed with Pre production check



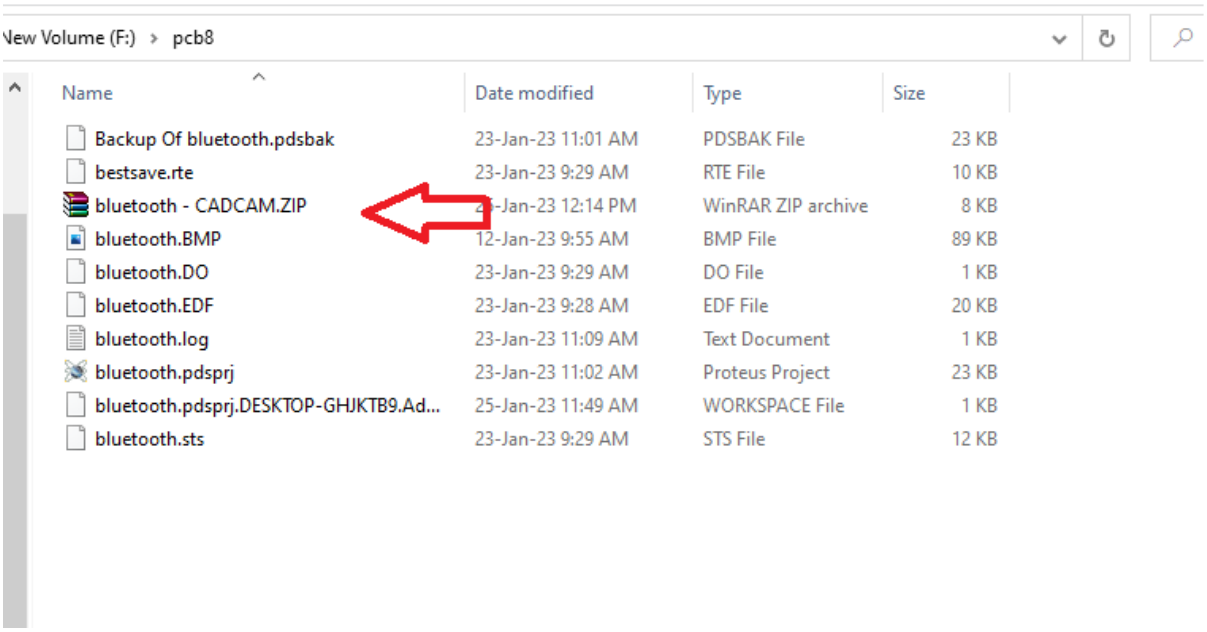
4. Proceed and complete the process. Click close.



5. Select the required layers and click output as single Zip file



6. **Now you will have the Gerber file in the folder**



Pre production check performed andGerber file of the schematic is generated.

Lab in charge	**Signature of the lab in charge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

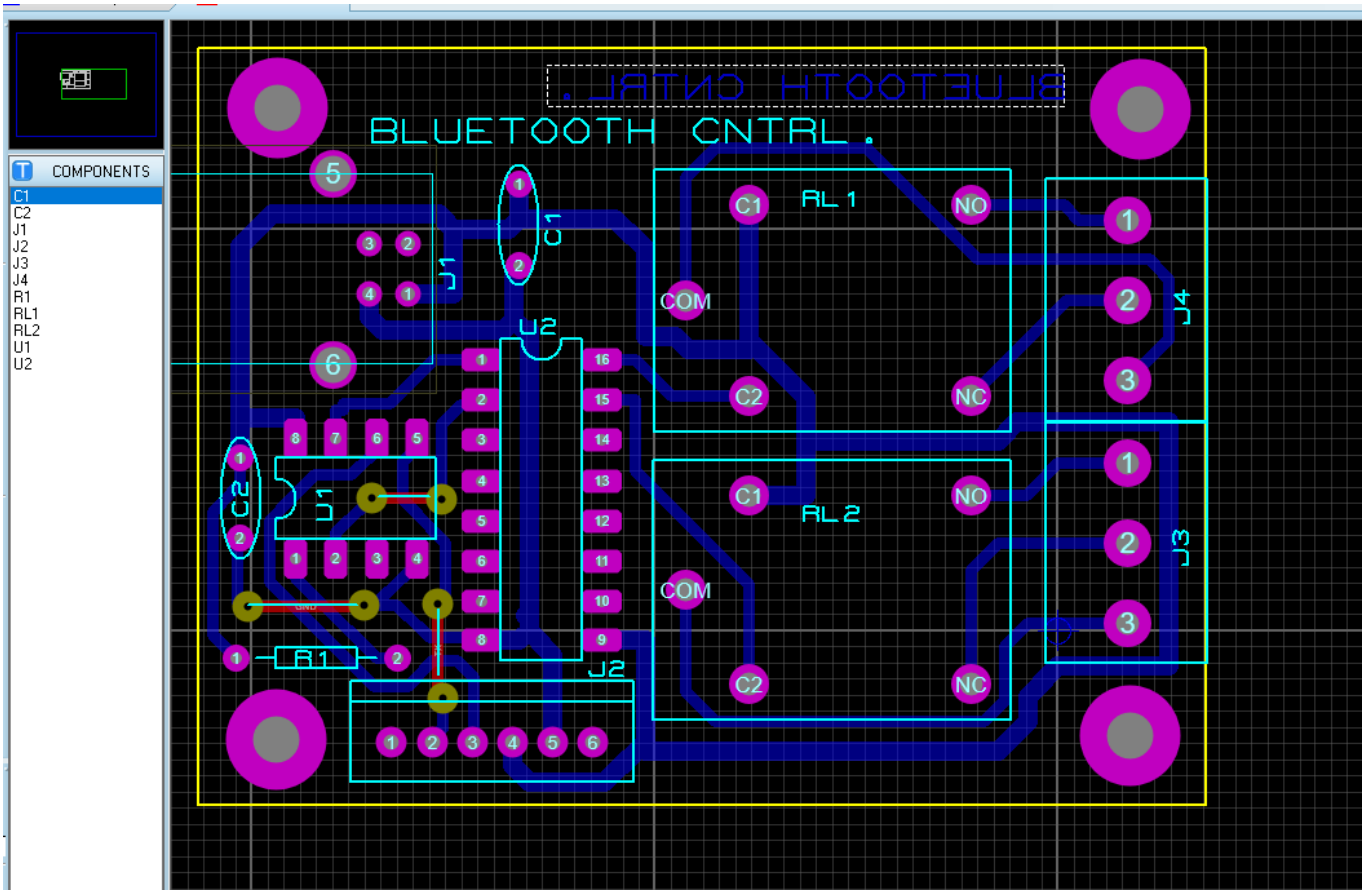
Exp: 13	Generating screen for PCB	Date :

Time : 30 minutes

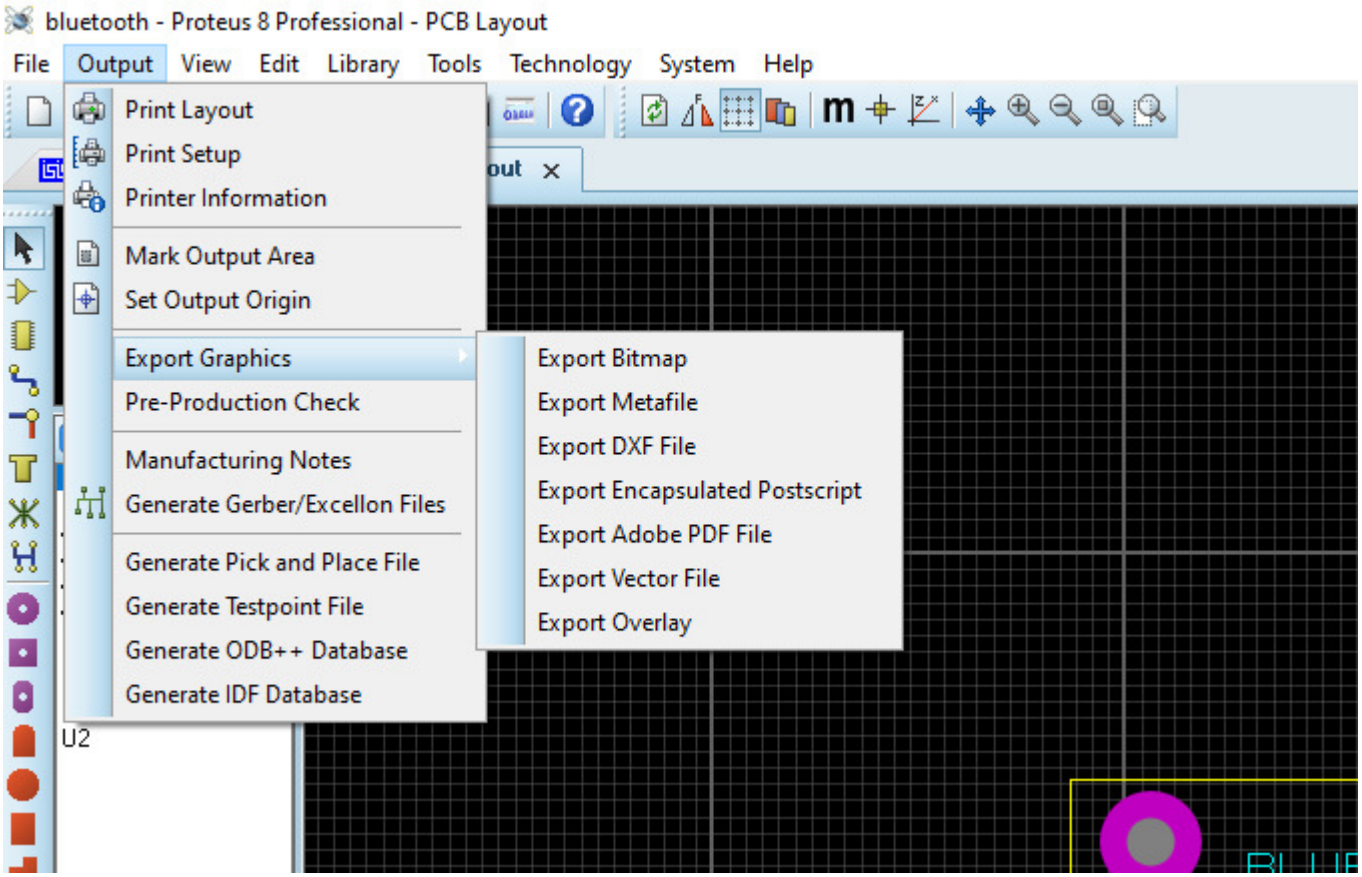
Problem Statement: Perform Generate screen for bottom layer, mask and silk screen for the PCB.

Procedure:

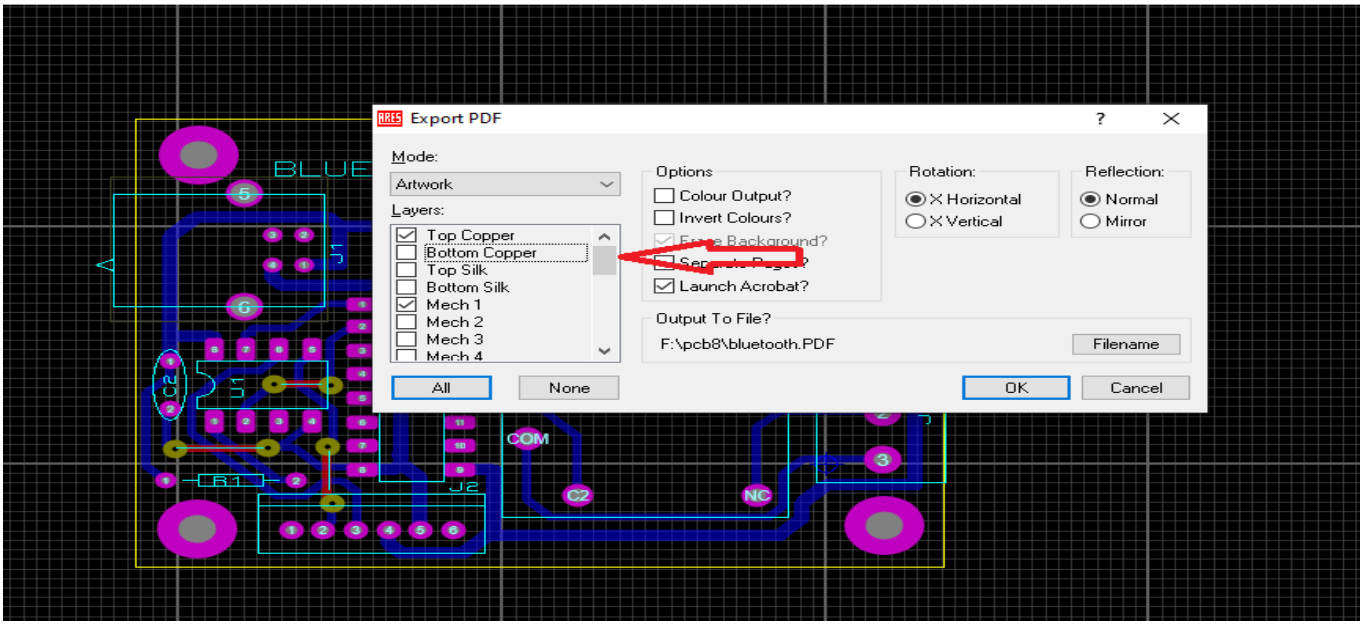
1. **Open the required PCB lay out**



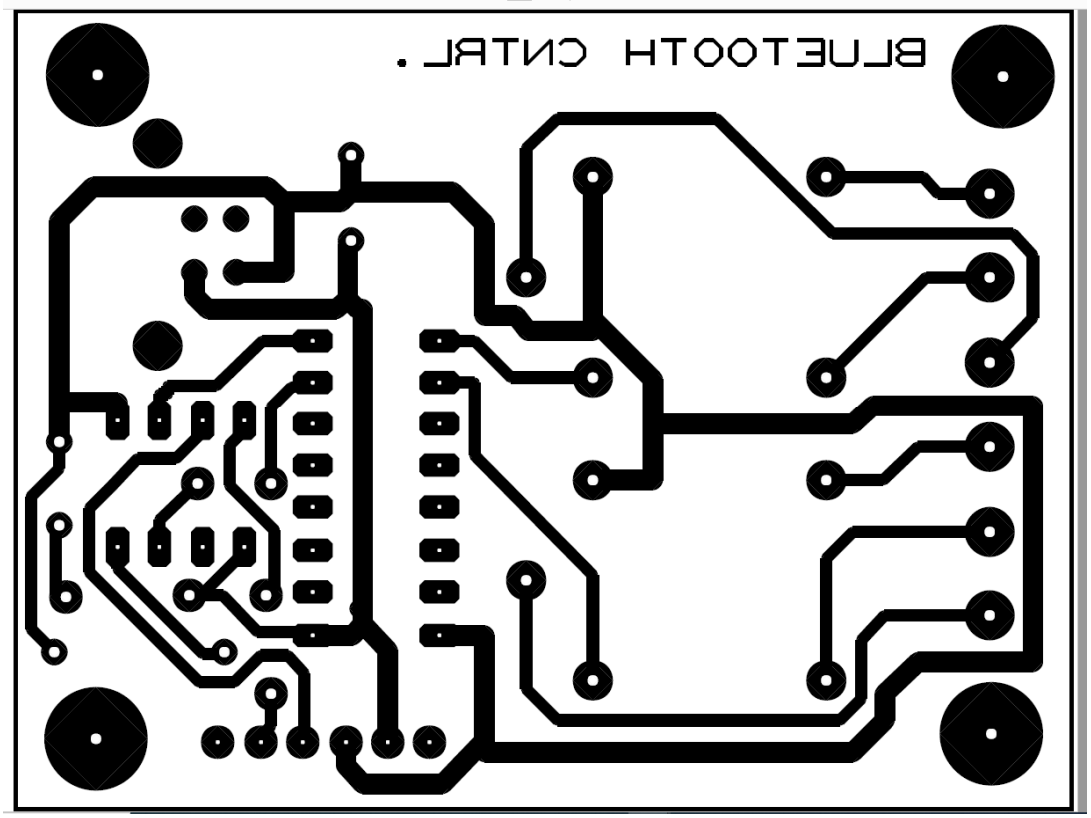
2. Select Output > Export Graphics > and required format (in this case as PDF)



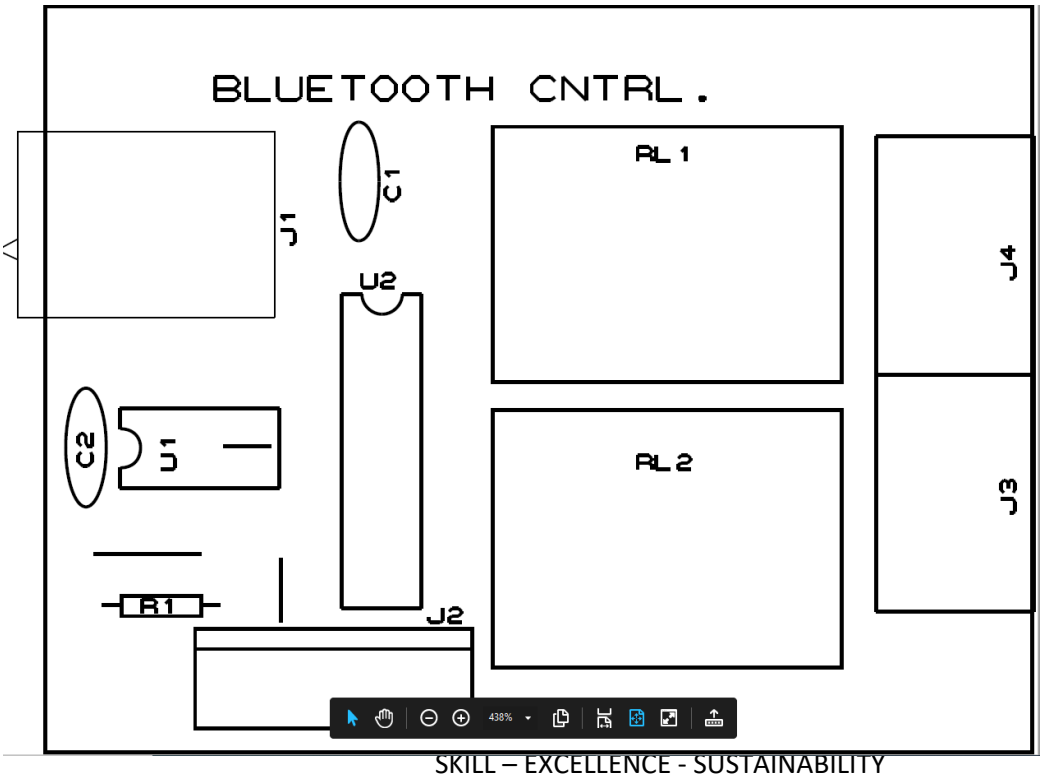
3. Select required screen and click ok.



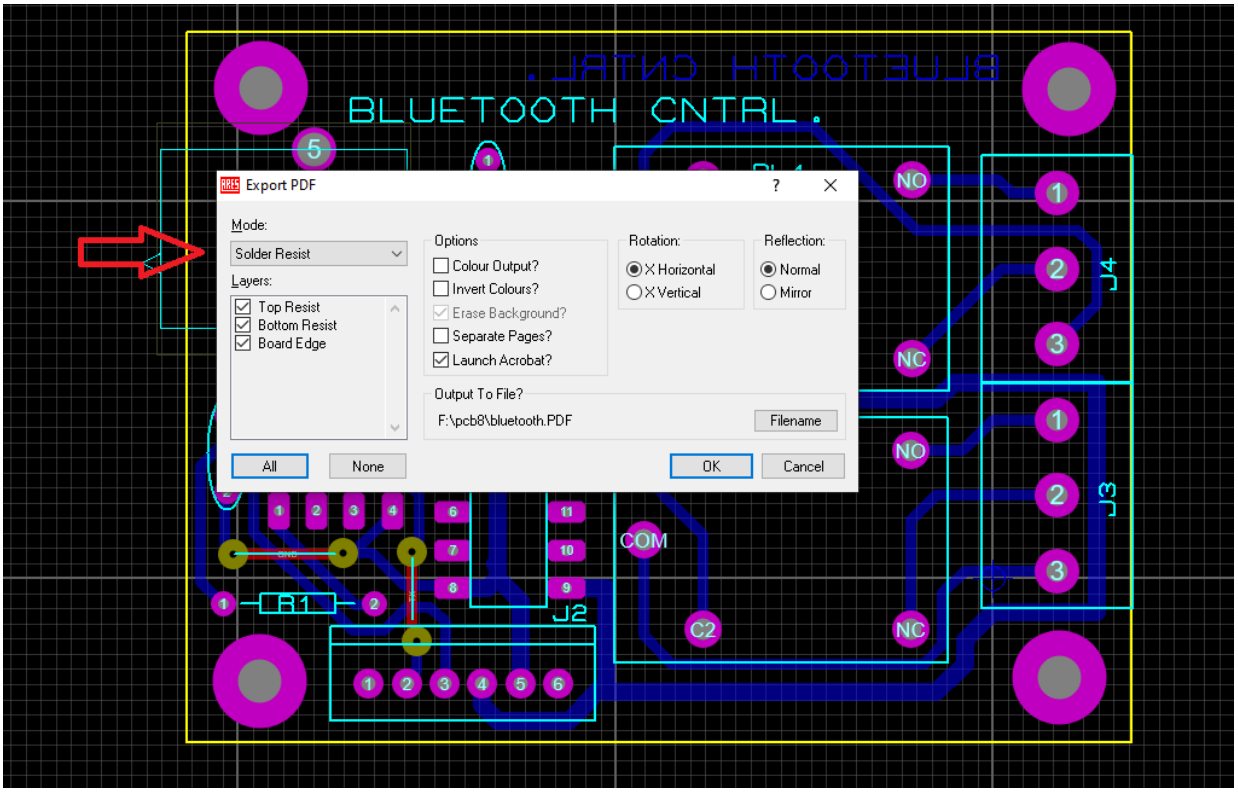
Bottom copper layer

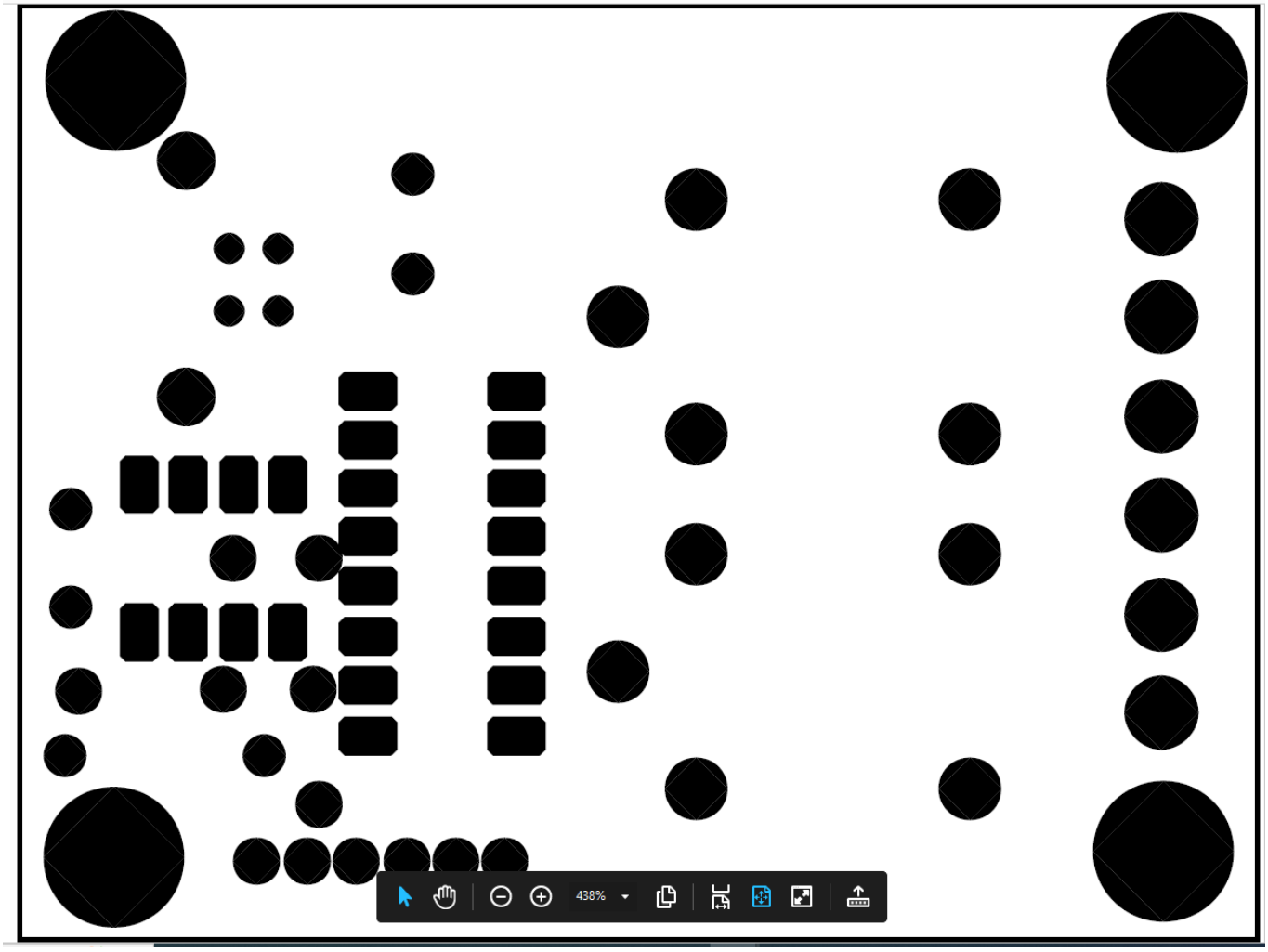


Silk Screen



Solder resist or mask





Various Screen for the PCB generated.

Lab in charge	**Signature of the lab in charge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

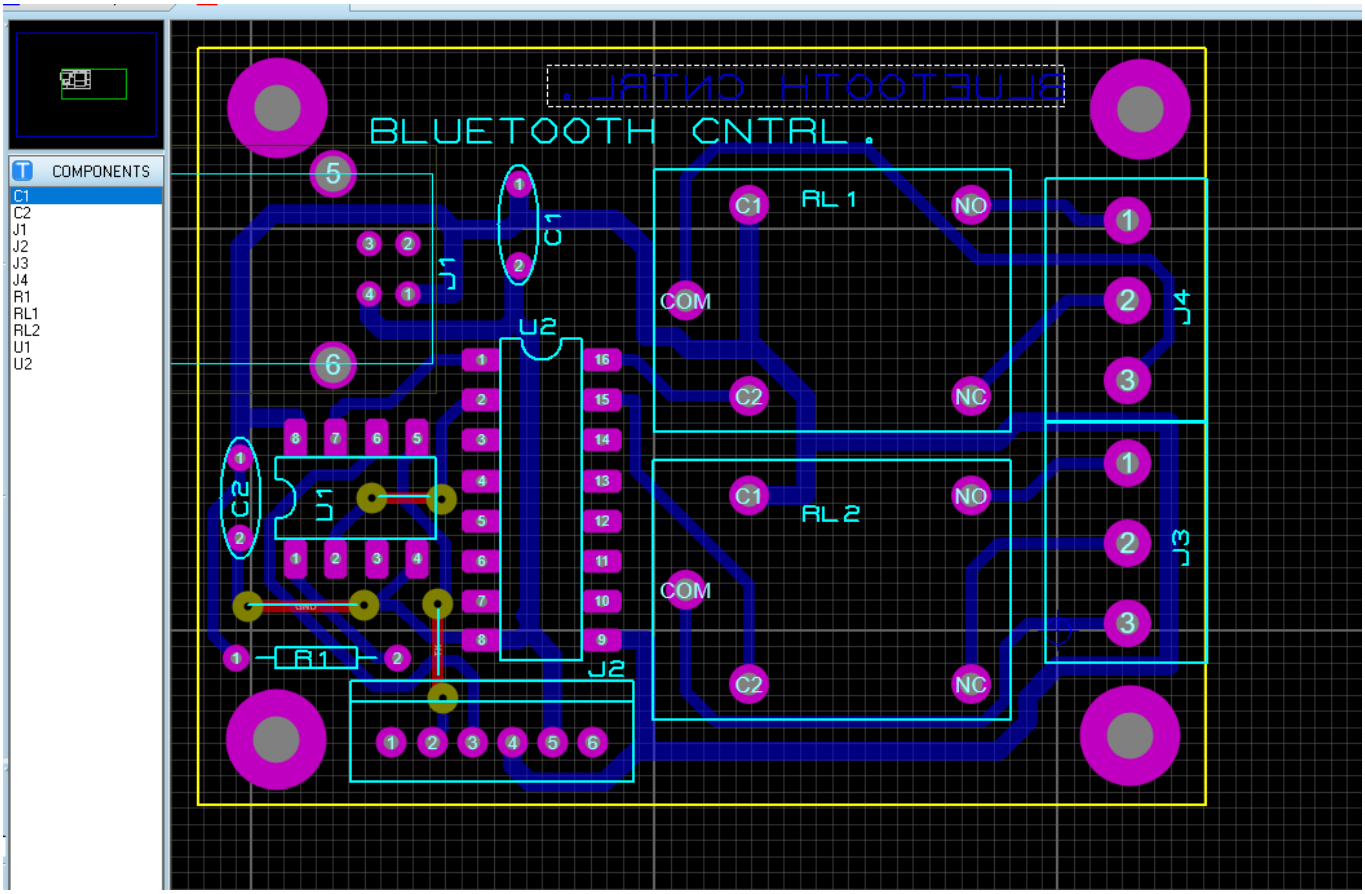
Exp: 13	DESIGN RULE CHECK	Date :

Time : 30 minutes

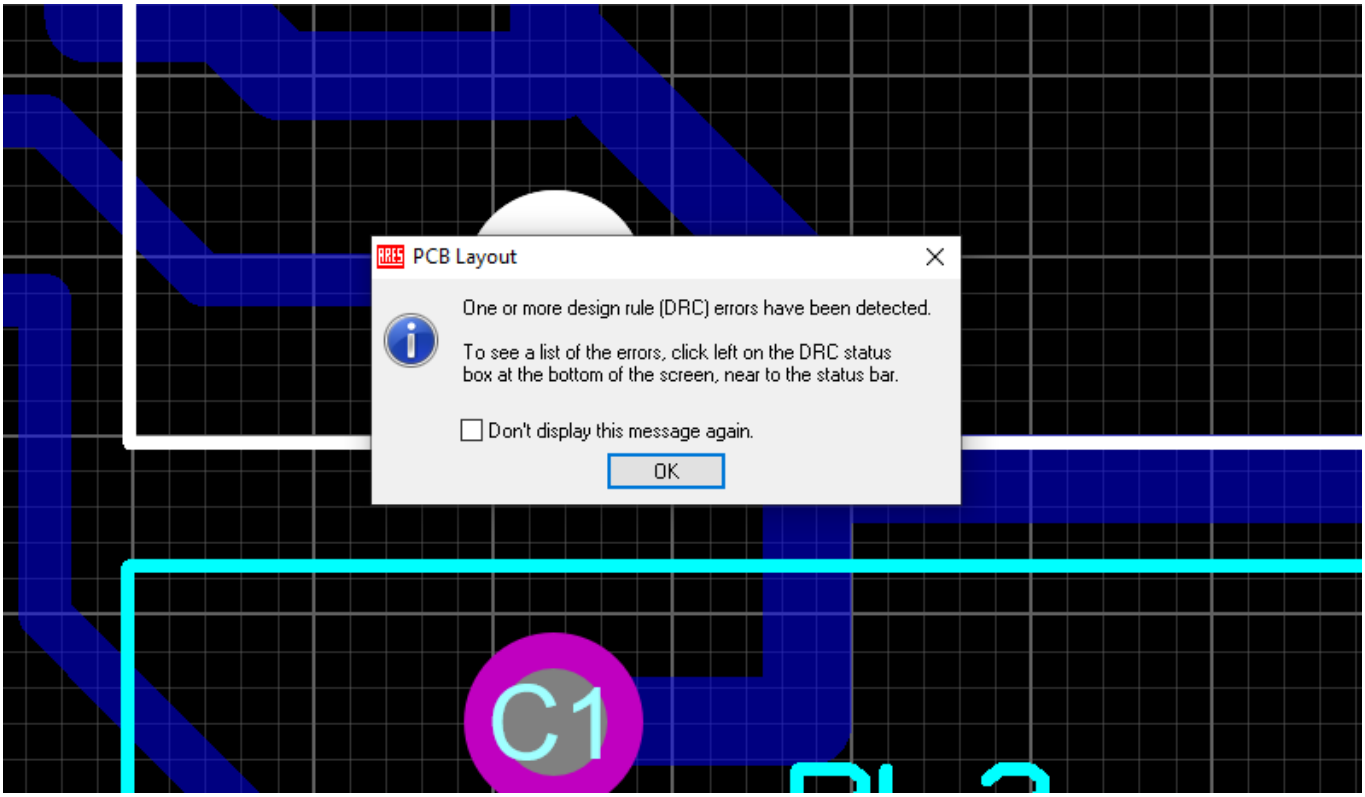
Problem Statement: Familiarize various design rule checks.

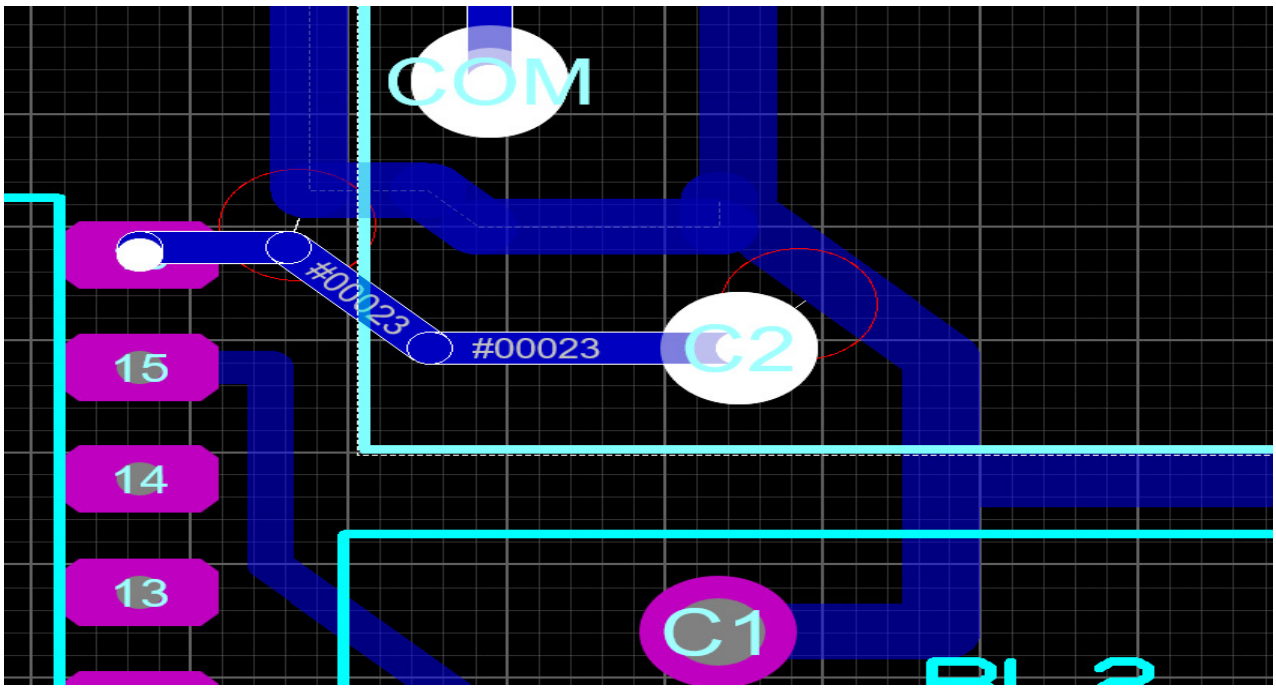
Procedure:

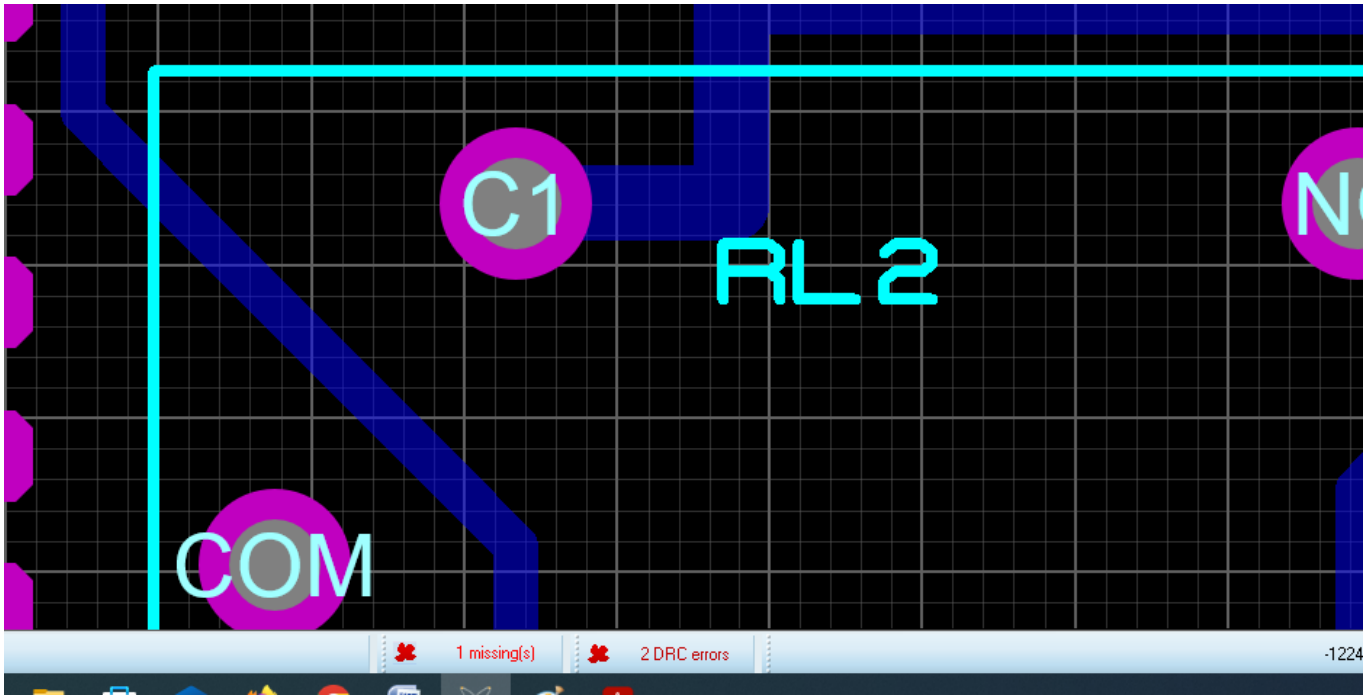
1. **Open the required PCB lay out**

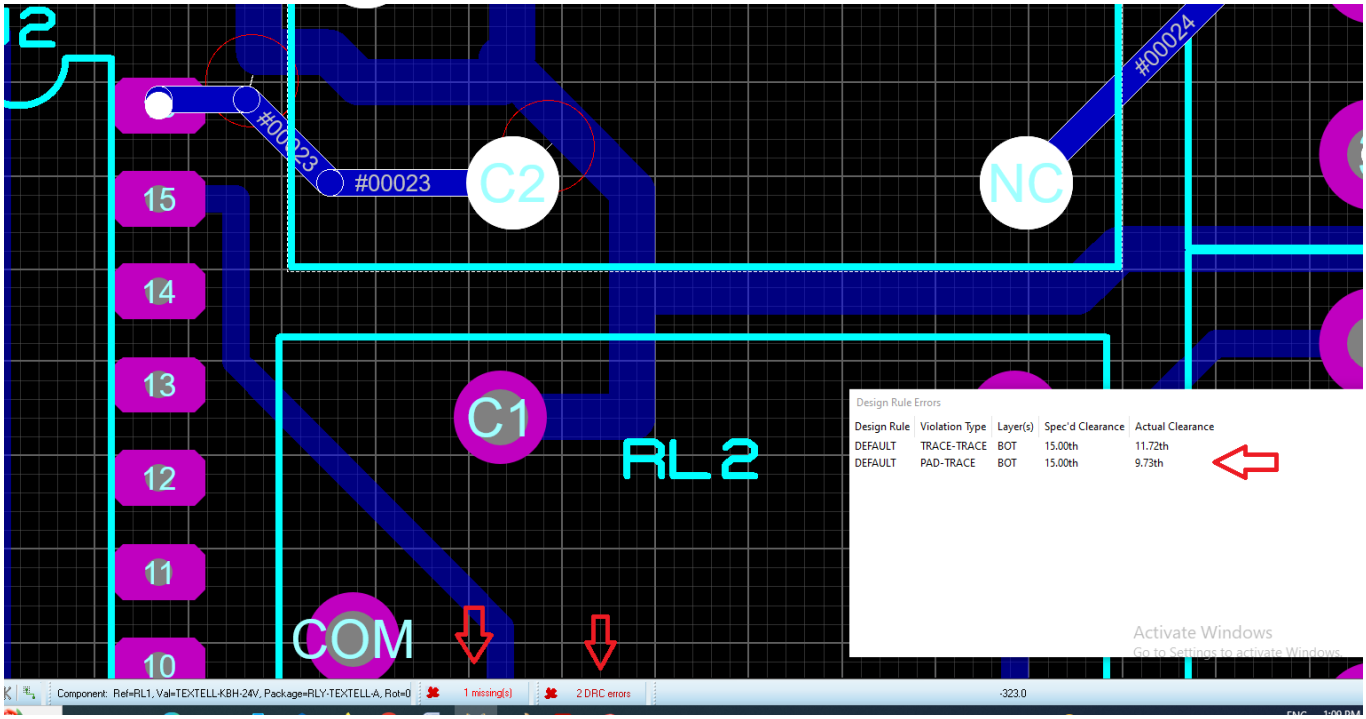


2. Identify and rectify various DRC errors









Double click to see various errors

Various DRC errors familiarized and rectified.

Lab in charge	**Signature of the lab in charge**	**Date**
Readiness to do the experiment		
Completion of the experiment		

Exp: 14	OPEN ENDED EXPERIMENT	Date :

Time : 45 + 45 minutes

1. **Provide schematics available in electronics magazines to prepare double sided PCB which do not involve any custom component or foot print design.**
2. **Provide schematics and instruct student to prepare single sided PCB with custom components and custom foot print. Instruct to generate print out of bottom layer, solder mask and silk screen. Also generate Gerber file after pre production check**

Experiments evaluated

Lab in charge	Signature of the lab in charge	Date
Readiness to do the experiment		
Completion of the experiment		

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