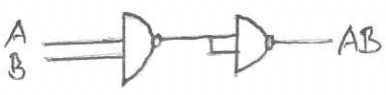
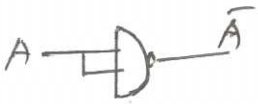
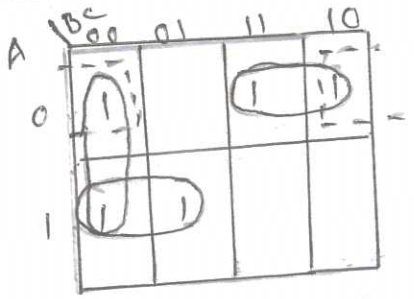
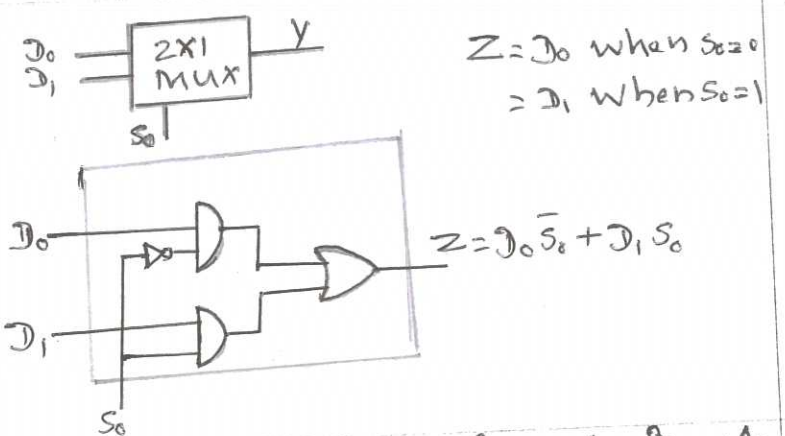
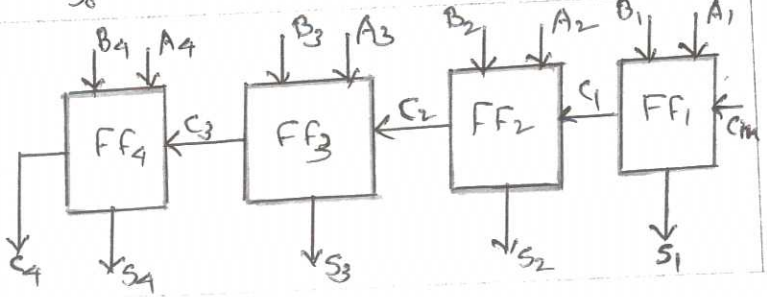
ScoringIndicators

COURSENAME:DIGITAL ELECTRONICS

COURSECODE: REV (21)-3044 **QID:2110220227**

QNo	ScoringIndicators	Splitscore	SubTotal	Totalscore
	PARTA			**9**
I.1	15_{16}		1	
I.2	0101		1	
I.3	NAND  NOR  any one		1	
I. 4	ECL		1	
I.5	Two		1	
I.6	Sequential circuits		1	
I.7	One input line and one output line		1	
I.8	Asynchronous counter		1	
I.9	RAM		1	
	PARTB			24
II.1	AC6 1010 1100 0110 9B 1001 1011 1011 0110 0001 Ans: $B61_{16}$ B59 1011 0101 1001 64 0110 0100 1011 1011 1101 Ans: BBD_{16}	1.5x2	3	
II.2	 	1.5x2	3	

II.3	 $Y_{min} = A\bar{B} + \bar{A}B + \bar{B}\bar{C}$ OR $Y_{min} = A\bar{B} + \bar{A}B + \bar{A}\bar{C}$	1 2	3	
II.4	Fan in = 8 Fan out = 10 Noise Margin = 0.4V Propagation Delay = 9ns Power Dissipation = 10mW/gate	1x3	3	
II.5	 $Z = D_0$ when $S_0 = 0$ $= D_1$ when $S_0 = 1$	1+2	3	
II.6		3	3	

PART C

III

(i)
$$\begin{array}{r} 1011 \times \\ 110 \\ \hline 0000 \\ 1011 \\ 1011 \\ \hline 1000010 \end{array}$$

(ii) $46 = 0010\ 1110$

$14 = 0000\ 1110$

$-14 = 1111\ 0010$

$46 + (-14)$

$$\begin{array}{r} 0010\ 1110 \\ 1111\ 0010 \\ \hline (1)0010\ 0000 \end{array}$$

ignore carry. MSB is zero

answer is the

Answer $= (0010\ 0000)_2$

$= (32)_{10}$.

(iii) $(2AB)_{16}$

2 A B

0010 1010 1011

2+2+3 | 7

IV

AB \ CD	00	01	11	10
00		1		
01	1	X	1	
11		1	X	X
10				1

$F_{min} = BD + AC\bar{D} + \bar{A}\bar{C}D + \bar{A}B\bar{C}$

4

3

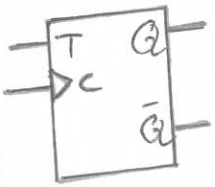
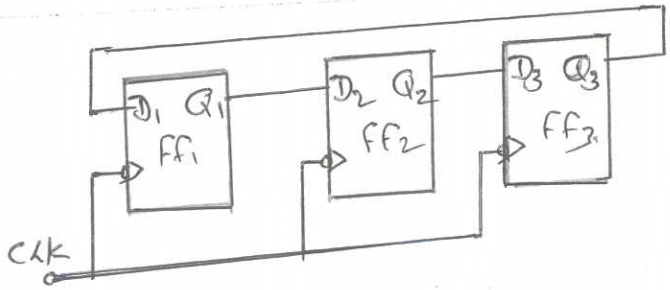
7

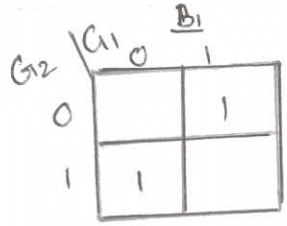
V

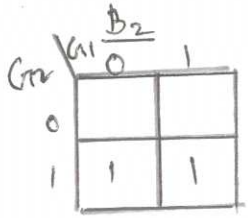
2 bit Gray		2 bit Binary	
G_2	G_1	B_2	B_1
0	0	0	0
0	1	0	1
1	1	1	0
1	0	1	1

2

7

II.7	 Application : Switch C T Q_n Q_{n+1} state ↑ 0 0 0 NC ↑ 0 1 1 ↑ 1 0 1 Toggle ↑ 1 1 0 0 X 0 0 NC 0 X 1 1 NC → No change.	1+1+1	3	
II.8		3	3	
II.9	① Design is simple ② Implementation is simple ③ All Flip Flops are not clocked simultaneously. ④ Output of first flip flop drives the clock for second and so on ⑤ Their speed is low.	1x3	3	
II.10	PROM : Programmable Read Only Memory. Done by user once EPROM: Erasable Programmable Read only Memory. Several times Programmable Erasing is done by using UV light	1 2	3	



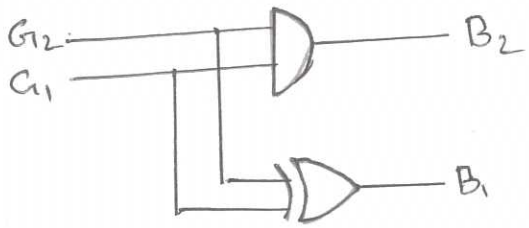


2

$B_1 = G_2\bar{G_1} + \bar{G_2}G_1$

$= G_2 \oplus G_1$

$B_2 = G_2 G_1$



3

VI

Inputs			Outputs							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

3

$D_0 = \bar{A}\bar{B}\bar{C}$, $D_1 = \bar{A}\bar{B}C$ $D_2 = \bar{A}B\bar{C}$ $D_3 = \bar{A}BC$

$D_4 = A\bar{B}\bar{C}$ $D_5 = A\bar{B}C$ $D_6 = AB\bar{C}$ $D_7 = ABC$

4

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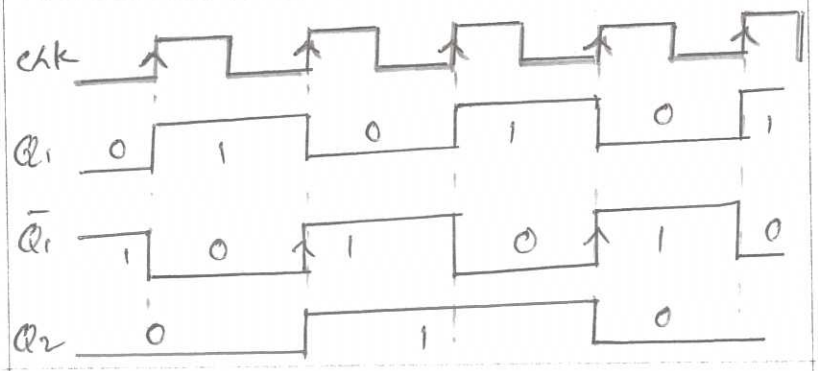
VII

External input	Present State	Next State	Flip flop inputs	
T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

3+4

7



3

XII

7

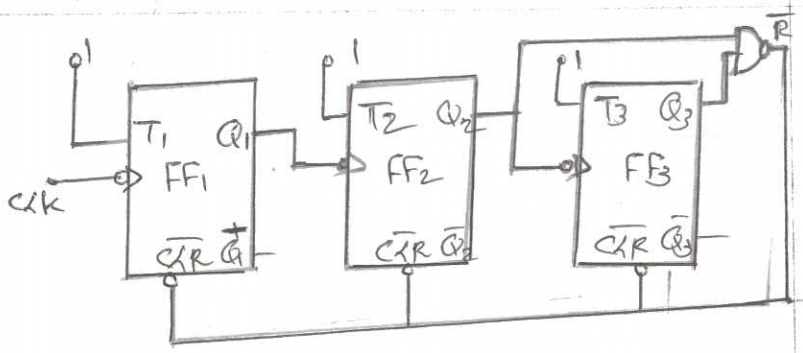
RAM (Random Access, Memory; Read/ write memory, temporary storage of Programs and data—, They are volatile, lose data when power failure occurs.
Any three points — 3

SRAM (Static RAM)
Memory cells are flip flops, store bits Available both in bipolar and MOS technologies. — 2

DRAM (Dynamic RAM)
Store Data as charges on capacitor. Periodical refreshment is needed — 2

XIII

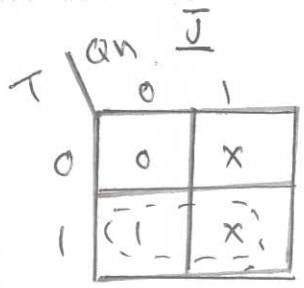
7



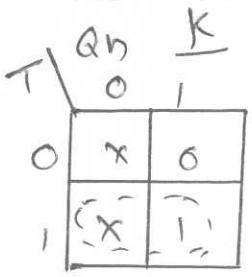
3

After pulses	State Q_3	Q_2	Q_1	R
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1	1	0	1
	↓	↓	↓	
7	0	0	1	0

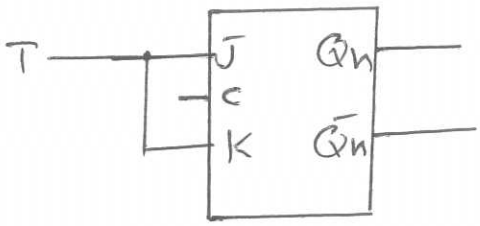
3



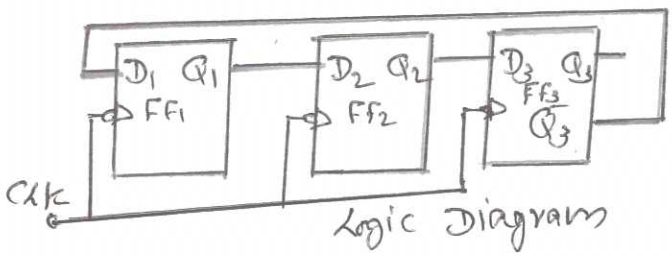
$J = T$



$K = T$



VIII



Logic Diagram

3

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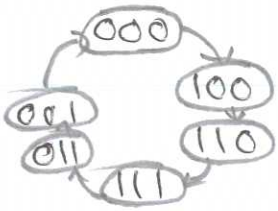

State Diagram

2

Explanation

o/p of first flip flop is the i/p of second and so on. Input of first flip flop is the complemented output of last flip flop

2

IX

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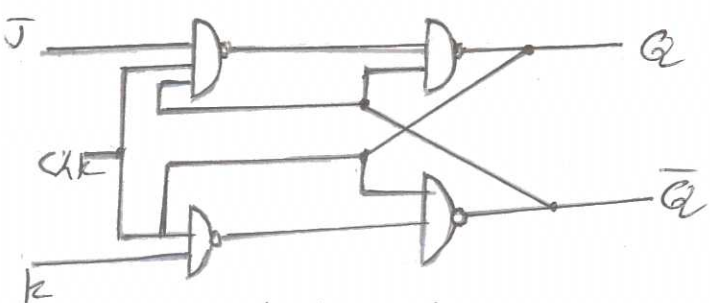


Logic Diagram

3

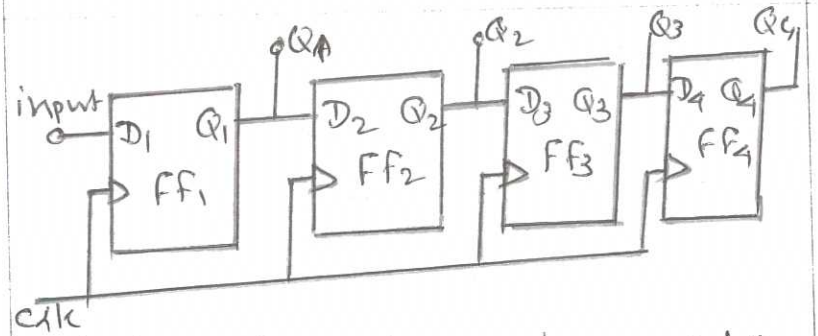
C	J	K	Q_n	Q_{n+1}	State
↑	0	0	0	0	No change
↑	0	0	1	1	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	1	Toggle
↑	1	1	1	0	
0	x	x	0	1	No change
0	x	x	1	1	

Truth Table

Explanation — 1

3

X

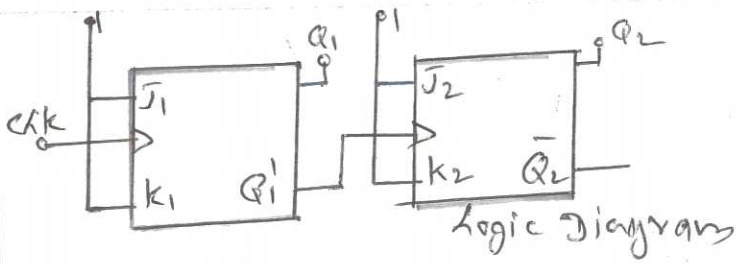


4

Explanation: Assuming a 4 bit input of any combination and defining the four outputs after each clock. — 3

7

XI



Logic Diagram

3

Explanation:-

Explanation regarding the ckt — 1

7

$R = Q_3Q_2$, $\bar{R} = Q_3\bar{Q}_2$

Explanation: Since Mod 6, only 6 states, counts from 0 to 5; when the next count is going to 6, it resets and start from initial state

1

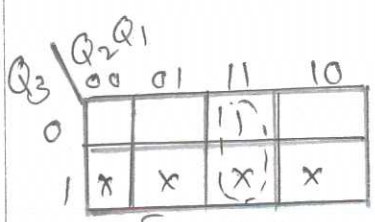
XIV

7

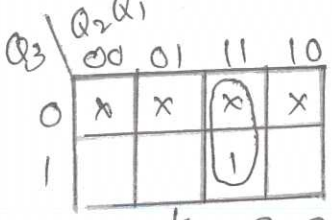
PS	NS	Required Excitations		
$Q_3\ Q_2\ Q_1$	$Q_3\ Q_2\ Q_1$	$J_3\ K_3$	$J_2\ K_2$	$J_1\ K_1$
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X 1
0 1 0	0 1 1	0 X	X 0	1 X
0 1 1	1 0 0	1 X	X 1	X 1
1 0 0	1 0 1	X 0	0 X	1 X
1 0 1	1 1 0	X 0	1 X	X 1
1 1 0	1 1 1	X 0	X 0	1 X
1 1 1	0 0 0	X 1	X 1	X 1

3

Excitation Table

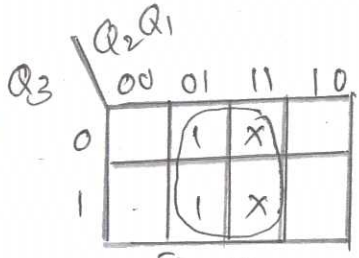


$\bar{J}_3 = Q_2Q_1$

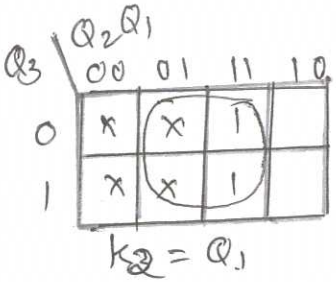


$K_3 = Q_2Q_1$

4



$\bar{J}_2 = Q_1$



$K_2 = Q_1$

$J_1 = K_1 = 1$