SET 1

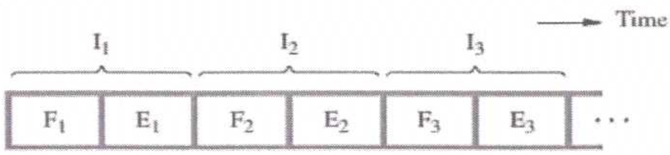
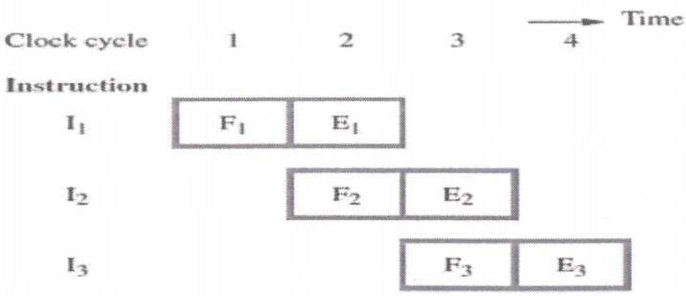
Scoring Indicators

COURSE NAME: COMPUTER ORGANISATION

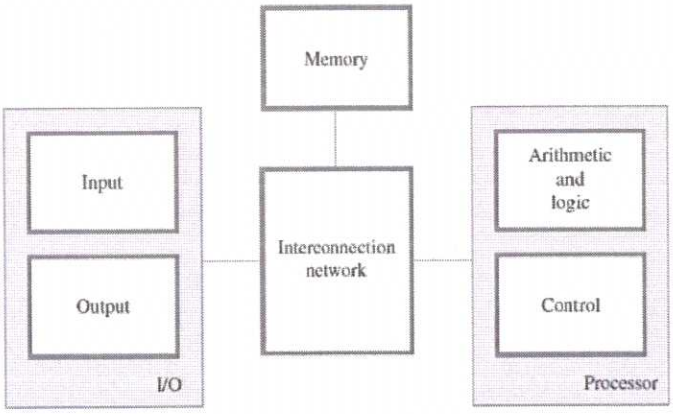
COURSE CODE:3131 QID: 2110220197

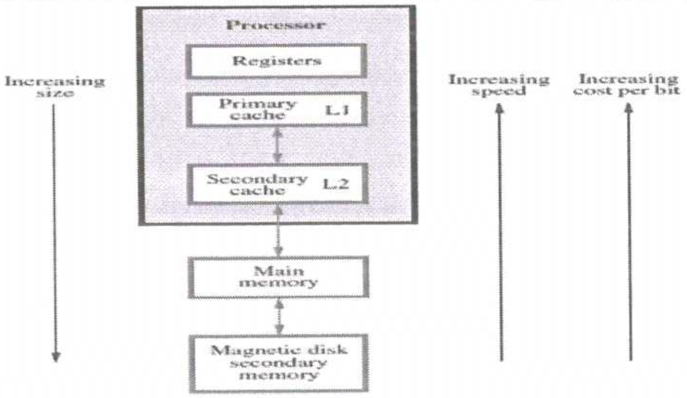
Q. No.	Scoring Indicators	Split Score	Sub Total	Total Score
	PART A			**9**
I. 1	Redundant Array of Independent Disks	1	1	1
I. 2	Electrically Erasable Programmable Read-Only Memory is a user-modifiable ROM.	1	1	1
I. 3	Impact and Non-Impact	0.5x2 = 1	1	1
I. 4	Peripheral Component Interconnect (PCI)	1	1	1
I. 5	• Program Counter (PC) • Memory Address Register (MAR) • Memory Data Register (MDR) • Instruction register (IR)	0.5x2 =1 (Any two)	1	1
I. 6	Microprogram counter is used to read control words sequentially from the control store.	1	1	1
I. 7	Control Word(CW) is a word whose individual bits represent various control-signals such as Add, PCin etc.	1	1	1
I. 8	A microprocessor is an integrated circuit designed to function as the CPU of a microcomputer.	1	1	1
I. 9	BP – Base Pointer and SP – Stack Pointer	0.5x2=1	1	1
	PART B			**24**
II. 01	***STATIC RAM*** • Capable of retaining their state as long as power is applied. • SRAMs are volatile memories. • Very low power consumption. • Static RAMs can be accessed very quickly.			

	DYNAMIC RAMS • Information is stored in a cell is in the form of charge in a capacitor. • Contents must be periodically refreshed to retain the information stored. • Less expensive. • High density.	1.5x2=3 Any 3 Points from each Section.	3	3
II. 02	**RAID 0**: Striping **RAID 1**: Mirroring **RAID 2**: Bit-Level Striping with Dedicated Hamming-Code Parity **RAID 3**: Bit-Level Striping with Dedicated Parity **RAID 4**: Block-Level Striping with Dedicated Parity **RAID 5**: Striping with Parity **RAID 6**: Striping with Double Parity	1x3=3 Expln. of Any 3	3	3
II. 03	• Provide a simple, low-cost, and easy to use interconnection system that overcomes the difficulties due to the limited number of i/o ports. • Accommodate a wide range of I/O devices and bit rates, including Internet connections, and audio and video applications. • Enhance user convenience through a "plug-and-play" mode of operation.	3x1=3	3	3
II. 04	**Step** **Action** 1 PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in} 2 Z_{out}, PC_{in}, Y_{in}, WMFC 3 MDR_{out}, IR_{in} 4 Offset-field-of-IR_{out}, Add, Z_{in} 5 Z_{out}, PC_{in}, End Step 1-3: Fetch phase - loads the instruction to **IR.** Step 4: The offset-value is extracted from IR by instruction-decoding circuit.	3	3	3

	Since the updated value of PC is already available in register Y, the offset X is gated onto the bus, and an addition operation is performed. Step 5: The result, which is the branch target address, is loaded into the PC.			
II. 05	Pipelining is a process of executing instructions concurrently. Let Fi and Ei refer to the fetch and execute steps for instruction Ii. Execution of a program consists of a sequence of fetch and execute steps, as shown below,  (a) Sequential execution This fetching and executing phases can be operated in an overlapped way. That is when the execution unit is executing the current instruction, the fetch unit can fetch the next instruction. This is basic idea of instruction pipelining.  (c) Pipelined execution ***Pipeline Performance*** The performance increase is proportional to the number of pipeline stages. In this example (Two stage), in each clock cycle, one instruction is completed execution, which means the rate of instruction processing is doubled.	2 Defn. & Expln. 1	3	3
II. 06	To fetch instruction/data from memory, 1. Processor transfers required address to MAR. ***MAR← Address*** 2. Processor issues Read signal on control-lines of	3		

	memory-bus. 3. Wait for the **MFC** response from memory. 4. Load **MDR** from memory bus. 5. From MDR, they are transferred to IR or other registers. ***IR← [MDR]***		3	3
II. 07	The execution of instruction involves, 1. **Fetch Phase**: Load the instruction pointed by the PC to instruction register. ***IR←[[PC]]*** 2. **Execution Phase**: Carry out the operation specified by the instruction in the IR and it may store data from processor registers to memory locations.	1.5x2=3	3	3
II. 08	• It has an instruction queue capable of storing six instruction bytes. • It is the first 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, and 16-bit external data bus resulting in faster processing. • 8086 has 20-bit address bus. • 8086 can access up to 1 Mb of memory. • It is available in 3 versions based on the frequency of operation – 8086 → 5MHz,8086-2 → 8MHz and 8086-1 → 10 MHz • It uses two stages of pipelining, i.e. fetch Stage and Execute Stage. • It has 256 vectored interrupts etc.	Any three 1x3=3	3	3
II. 09	A multi-core processor is an integrated circuit with two or more processor cores attached to it for faster simultaneous processing of several tasks, reduced power consumption, and for greater performance. Identical cores within the same chip forms a **homogeneous multicore**, whereas non identical cores constitute **heterogeneous** multicore processor.	1 Defn. 1x2=2	3	3

II. 10	There are 3 control flags in 8086 for enabling or disabling certain operations of the microprocessor. 1. **Directional Flag (D)** – This flag is specifically used in string instructions. If set (1), then access the string data from higher memory location towards lower memory location, else from lower memory location towards higher memory location. 2. **Interrupt Flag (I)** – This flag is for interrupts. If set (1), the microprocessor will recognize interrupt requests from the peripherals, else will not recognize any interrupt requests and will ignore them. 3. **Trap Flag (T)** – This flag is used for on-chip debugging. Setting trap flag puts the microprocessor into single step mode for debugging.	3x1=3	3	3
	PART C			**42**
III. 01	 ***Input Unit:*** Computers accept coded information through input units. The most common input device is the keyboard. ***Memory Unit :*** The function of the memory unit is to store programs and data. There are two classes of storage, called primary and secondary. ***Arithmetic and Logic Unit :*** Most computer operations are executed in the arithmetic and logic unit (ALU) of the processor. ***Output Unit :*** The output unit is the counterpart of the input unit. Its function is to send processed results to the outside world. Example Printer, Monitor etc. ***Control Unit :*** Control unit coordinates all the operation of the above mentioned units.	2 Figure 1x5=5 Functions	7	7

<table>
<tr>
<td>III. 02</td>
<td>

<table>
<tr><td>Memory</td><td>Speed</td><td>Size</td><td>Cost</td></tr>
<tr><td>Registers</td><td>Very high</td><td>Lower</td><td>Very Lower</td></tr>
<tr><td>Primary cache</td><td>High</td><td>Lower</td><td>Low</td></tr>
<tr><td>Secondary cache</td><td>Low</td><td>Low</td><td>Low</td></tr>
<tr><td>Main memory</td><td>Lower than Seconadry cache</td><td>High</td><td>High</td></tr>
<tr><td>Secondary Memory</td><td>Very low</td><td>Very High</td><td>Very High</td></tr>
</table></td>
<td>Figure 2.5
Compar-ison Speed Size Cost 1.5x3=4.5</td>
<td>7</td>
<td>7</td>
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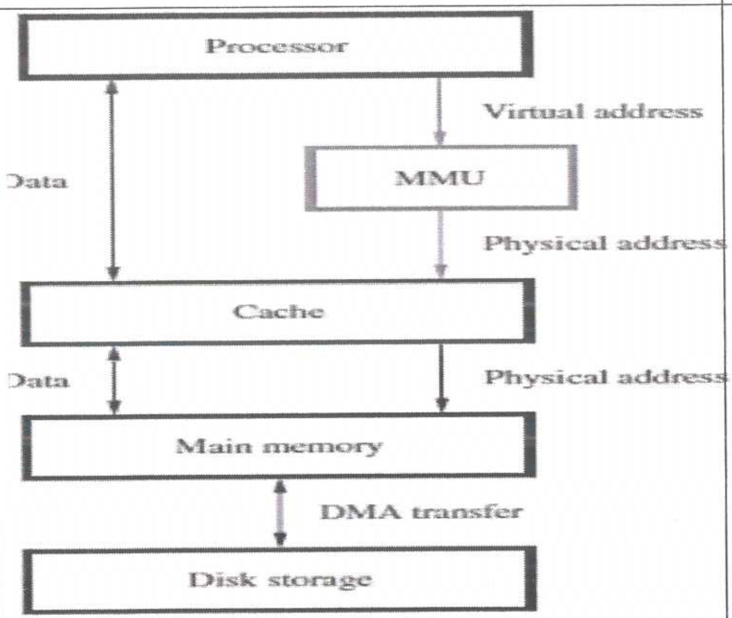
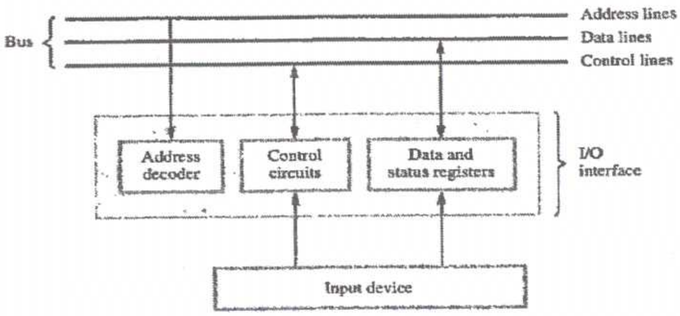
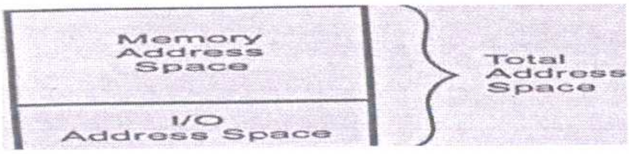
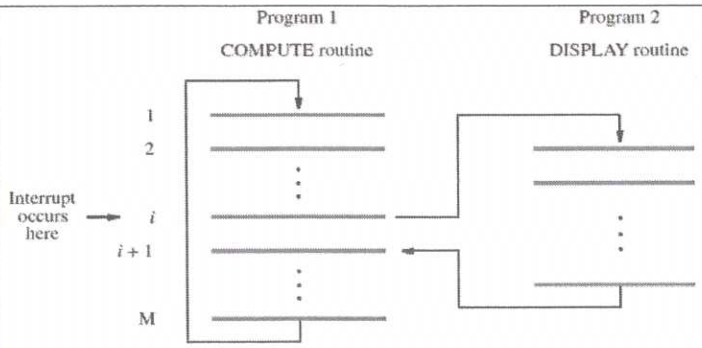
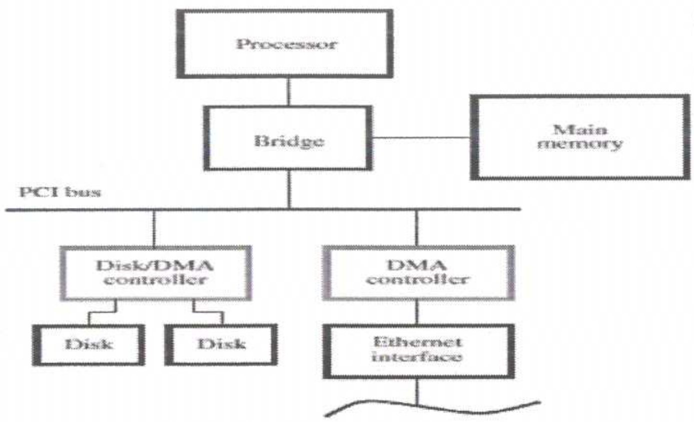
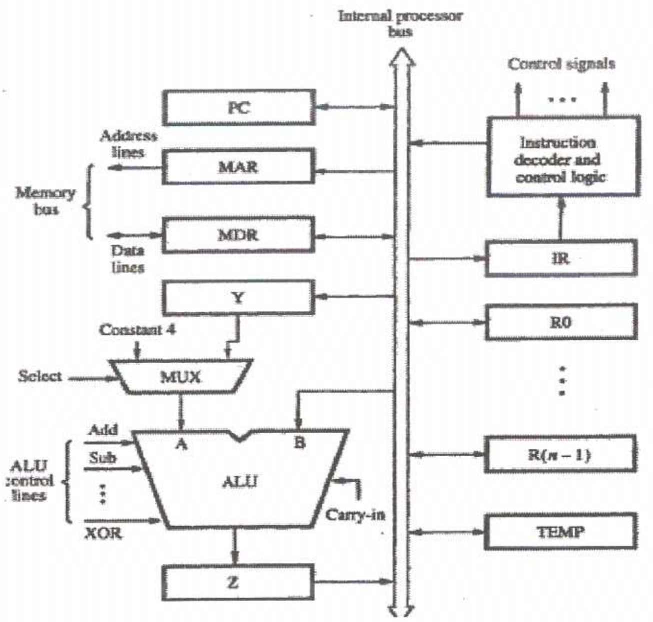
<td>III. 03</td>
<td>

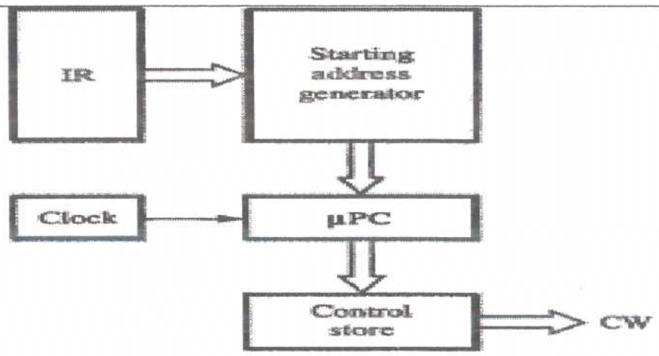
In most computer systems, the physical main memory is not as large as the address space of the processor. If a program does not completely fit into the main memory, the parts of it not currently being executed are stored on a secondary storage device. As these parts are needed for execution, they must first be brought into the main memory, possibly replacing other parts that are already in</td>
<td>Figure 3
Expln. 4</td>
<td>7</td>
<td>7</td>
</tr>
</table>

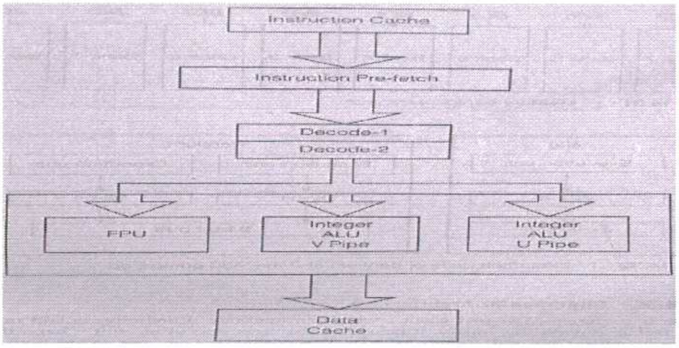
	the memory. The binary addresses that the processor issues for either instructions or data are called virtual or logical addresses. These addresses are translated into physical addresses by a combination of hardware and software actions. Figure shows a typical organization that implements virtual memory. A special hardware unit, called the Memory Management Unit (MMU), keeps track of which parts of the virtual address space are in the physical memory. When the desired data or instructions are in the main memory, the MMU translates the virtual address into the corresponding physical address.			
III. 04	• **Platters:** Disk *platter* has a flat circular shape. Its two surfaces are covered with a magnetic material and information is recorded on the surfaces. The disk surface is logically divided into *tracks*, which are subdivided into *sectors.* • **Head:** It is a device present on the arm of the hard drive that reads or writes data on the magnetic platters. • **Spindle:** It is the spinning shaft on which holds the platters in a fixed position such that it is feasible for the read/write arms to get the data on the disks. • **Actuator:** It is a device, consisting of the read-write head that moves over the hard disk.	Names 1 Expln 1.5x4=6	7	7
III. 05	Figure illustrates the interfacing of I/O devices. The address decoder enables the device to recognize its address when this address appears in the address line. The data register holds the data being transferred to or from the processor. The status register contains status information of the operation. **Program-Controlled I/O:** Program-Controlled I/O repeatedly checks (polls) the status flag of the device to achieve the required synchronization between the processor	3		

	and I/O device.  **Memory Mapped I/O:** I/O devices and Memory share the same address space. The total memory address space is partitioned and part of this space is devoted to I/O addressing. So machine instruction that can access memory can be used to transfer data to or from an I/O device also.  	2 2	7	7
III. 06	An **interrupt** is a signal emitted by hardware or software when a process or a device needs immediate attention. **Sequence of events involved in handling an interrupt request from a device.** 1. The device raises an interrupt request. 2. The processor interrupts the program currently being executed and saves the contents of the PC and PS registers. 3. Interrupts are disabled by clearing the IE bit in the PS to 0. 4. The action requested by the interrupt is performed by the interrupt-service routine. 5. Upon completion of the interrupt-service routine, the saved contents of the PC and PS registers are restored and enables interrupts by setting the IE bit to 1. 6. Then execution of the interrupted program is resumed.	Defn. 1 Steps 4	7	7

	 For example, assume that an interrupt request arrives during execution of instruction 'i' in Figure. The processor first completes execution of instruction 'i'. Then, it loads the program counter with the address of the first instruction of the interrupt-service routine. After execution of the interrupt-service routine, the processor returns to instruction i + 1.	Expln. 2		
III. 07	Direct memory access, or DMA is used to transfer blocks of data directly between the main memory and I/O devices without continuous intervention of the processor. The unit that controls DMA transfers is referred to as a DMA controller.  The DMA controller performs the functions that would normally be carried out by the processor when accessing the main memory. For each word transferred, it provides the memory address and generates all the control signals needed. It increments the memory address for successive words and keeps track of the number of transfers. To initiate the transfer of a block of words, the processor sends to the DMA controller the starting address, the	Defn. 2 2 Figure Expln. 3	7	7

	number of words in the block, and the direction of the transfer. The DMA controller then proceeds to perform the requested operation. When the entire block has been transferred, it informs the processor by raising an interrupt.			
III. 08	A flat-panel display (FPD) is an electronic display used to display visual contents. They are thin, lightweight, provide better linearity and are capable of higher resolution. Flat-panel displays use LCD or light-emitting diode (LED) technologies, sometimes combined. Flat-panel displays can be divided into two, **volatile and static**. The former requires that pixels be periodically electronically refreshed to retain their state (e.g. liquid-crystal displays (LCD)), and can only show an image when it has power. Static flat-panel displays rely on materials whose color states are bistable, such as displays that make use of e-ink technology, and as such retain content even when power is removed.	2 2 LED/ LCD Expln. 3	7	7
III. 09	 ALU and all the registers are interconnected via a Single Common Bus. Data & address lines of the external memory-bus is connected to the internal processor-bus	7	7	7

	via MDR and MAR respectively. Data may be loaded into MDR either from memory-bus (external) or from processor-bus (internal).			
III. 10	 Control-signals are generated by a program similar to machine language programs. **Control Word(CW)** is a word whose individual bits represent various control-signals (like Add, PCin etc). Individual control-words in microroutine are referred to as microinstructions. A sequence of CWs corresponding to control-sequence of a machine instruction constitutes the microroutine. The microroutines for all instructions in the instruction-set of a computer are stored in a special memory called the Control Store (CS). Control-unit generates control-signals for any instruction by sequentially reading CWs of corresponding microroutine from CS. μPC is used to read CWs sequentially from CS. Every time new instruction is loaded into IR, o/p of Starting Address Generator is loaded into μPC. Then, μPC is automatically incremented by clock, causing successive microinstructions to be read from CS.	3 4	7	7
III. 11	General Purpose registers labeled as **AX,BX,CX,DX** **AX (Accumulator)** -This is accumulator register. It is of 16 bits and is divided into two 8-bit registers AH and AL to also perform 8-bit instructions. It is used in arithmetic, logic and data transfer instructions	Names 1		

	BX (Base Register)-This is the base register. It is of 16 bits and is divided into two 8-bit registers BH and BL. BX register is an address register. It usually contains a data pointer used for based, based indexed or register indirect addressing. **CX (Count register)**-This is Count register. It is of 16 bits and is divided into two 8-bit registers CH and CL to also perform 8-bit instructions. This serves as a loop counter. **DX (Data Register)** -This is data register. It is of 16 bits and is divided into two 8-bit registers DH and DL to also perform 8-bit instructions. It is used in multiplication and division.	1.5x4=6	7	7
III. 12	Pentium has superscalar pipelined architecture which means, CPU can execute two or more instructions per cycle. It has, • Execution unit with two integer pipeline (U-pipe and V-pipe). • Pipelined floating point unit. • 8K code cache and 8K data cache • Branch prediction logic etc. 	Defn. 1 1.5x4=6 Expln.	7	7
