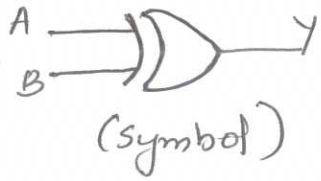
SCHEME OF VALUATION

Scoring Indicators

Revision: 2015 Course code: 3042

Course Title: DIGITAL ELECTRONICS

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	PART - A			
I 1.	$(111000)_2 \Rightarrow 1\times2^5 + 1\times2^4 + 1\times2^3 + 0+0+0$ $= 32 + 16 + 8 + 0 = (56)_{10}$	2	2	2
2.	2 i/p EX-OR gate  (symbol) Truth Table			

i/p		o/p
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

		1+1	2	2
3.	Fan out is defined as number of similar gates that a logic gate can drive.	2	2	2
4.	Applications of Shift register * To provide time delay * Keyboard Encoder * Ring Counter * Serial to parallel and parallel to serial data conversion	0.5x4	2	2
5.	. Counter (Ramp) type ADC . Successive approximation ADC . Dual slope integration type & . flash ADC	0.5x4	2	2

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	PART B			
II 1.	Demorgan's Theorems :			
	• First theorem states that Complement of a product is equal to sum of complements. i.e, $\overline{A \cdot B} = \overline{A} + \overline{B}$	3		
	• Second theorem states that the complement of sum is equal to the product of complements. i.e, $\overline{A + B} = \overline{A} \cdot \overline{B}$ where A and B are variables	3	3+3=6	6
2.	• Binary code is a coding system that uses the binary digits 0 and 1 to represent a letter, digit or other character in a computer or in other electronic device.	2		
	• Binary codes are further classified into (i) weighted code — which assigns specific weight to each bit position. eg: BCD, binary codes.	2		
	(ii) Non weighted code — which assigns no specific weights to bit position eg: Excess - 3 code and gray code	2	2+2+2	6

SCHEME OF VALUATION

Scoring Indicators

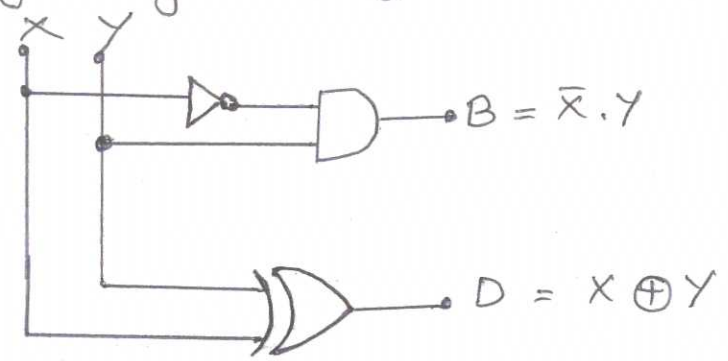
Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
II 3.	Half Subtractor Truth table is shown below			

Input		Output	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

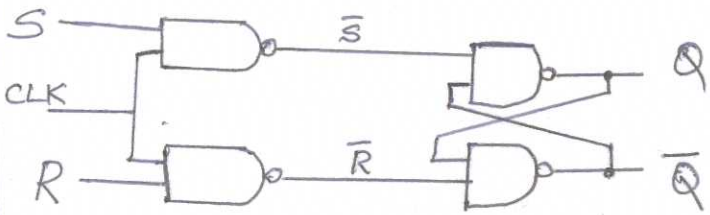
Expression for Difference, $D = X\bar{Y} + \bar{X}Y$ $= X \oplus Y$	2		
and for Borrow is, $B = \bar{X}.Y$	2		
Logic diagram is given below			



		2	2+2+2	6
II 4.	ECL features : (i) Logic levels are normally −0.8V(logic1) and −1.70V (logic 0) (ii) Switching speed is very high because transistors never saturate.			

SCHEME OF VALUATION

Scoring Indicators

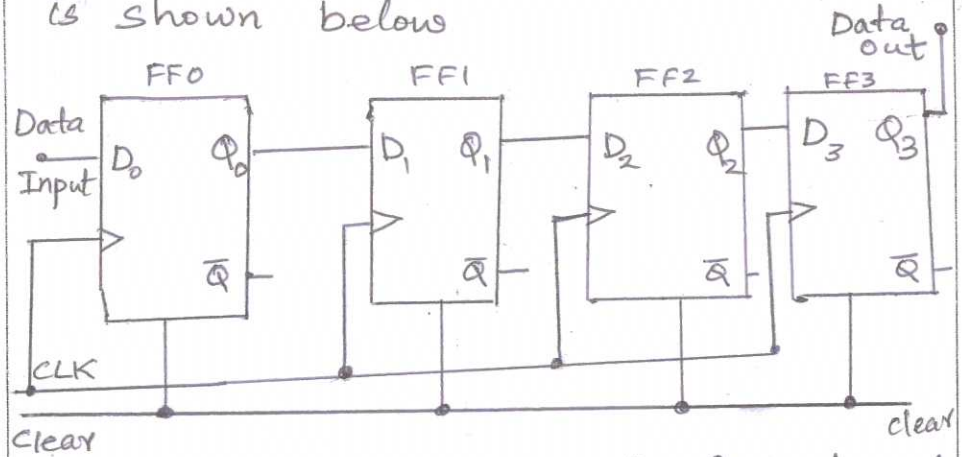
Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	(iii) Typical Power dissipation for a basic ECL gate is 40 mW. (iv) Fan-outs are typically around 25	3		
	CMOS Features : (i) Low power consumption (10mW) (ii) Small propagation delay (25ns to 150ns) (iii) High Noise margin (45% of V_{DD}) (iv) Large Fan out capability (>50)	3	3+3	6
II 5.	Circuit diagram of SR Flipflop using NAND gates only is shown below:			
		3		
	• When clock is zero, $\bar{S}=1$ & $\bar{R}=1$ Therefore there is no change in o/p. • when clock is 1, the inputs $\bar{R}$ & $\bar{S}$ are equal to complement of R & S. Therefore clocked SR flipflop follows the below truth table.	3		

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	CLK | R | S | Q | Comment 0 | X | X | NC | No change in o/p. 1 | 0 | 0 | NC 1 | 0 | 1 | 1 | Set 1 | 1 | 0 | 0 | Reset 1 | 1 | 1 | .. | Forbidden		(3+3) = 6	6
16.	Serial In Serial Out (SISO) using DFF is shown below  Operation : • The register is first cleared forcing all outputs to zero • The input is then applied sequentially to D i/p of first flipflop (FF0) • During each clock pulse, one bit is transmitted from left to right. • In order to get the data out of register they must be shifted out serially.	3 3	(3+3) = 6	6

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
II 7.	Specifications of DACs : (i) Accuracy : This indicates how close the measured value is to the true value (ii) Offset voltage : This is the voltage appears at the output when all the binary inputs are 0s. (zeros) (iii) Resolution : It is defined as the smallest change that can occur in the analog output as a result of a change in the digital input (iv) Settling time : The time required for the output of the DAC to settle to within ±(1/2) LSB of the final value for a given digital input.	1.5 x 4	6	6
	PART C			
	UNIT - I			
III (a)	(i) $(F329)_{16} = (1111001100101001)_2$	2		
	(ii) $(48.625)_{10}$ $48 \Rightarrow$ 2|48 0; 2|24 0; 2|12 0; 2|6 0; 2|3 1; 1 $= 110000$			

SCHEME OF VALUATION

Scoring Indicators

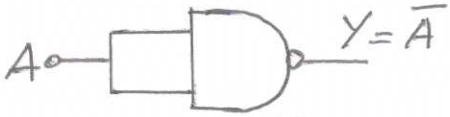
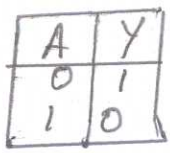
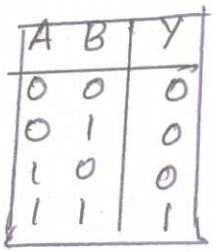
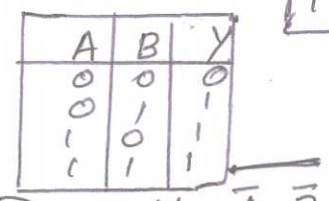
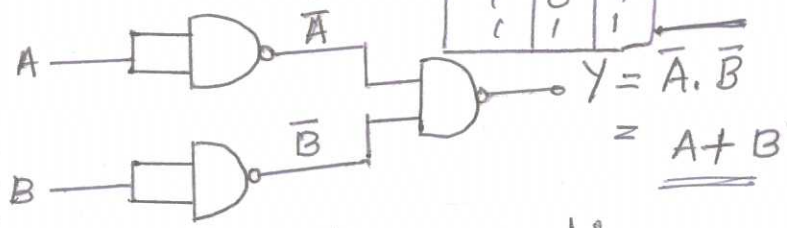
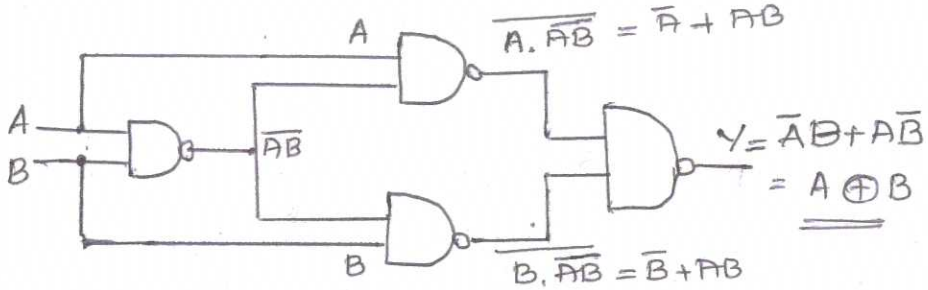
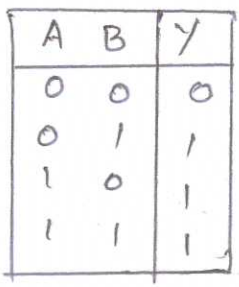
Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	$(0.625) \Rightarrow$ $0.625 \times 2 = 1.250$ $0.250 \times 2 = 0.500$ $0.500 \times 2 = 1.000$ $= (0.101)_2$ $(48.625)_{10} = (110000.101)_2$ - 2			
	(iii) Gray code 1 1 0 0 1 1 ↓↗↗↗↗↗ [Perform XOR-operation] 1 0 0 0 1 0 $= (100010)_2$ - 2			
	(iv) $(423)_{10} \Rightarrow$ 2 | 423 — 1 2 | 211 — 1 2 | 105 — 1 2 | 52 — 0 2 | 26 — 0 2 | 13 — 1 2 | 6 — 0 2 | 3 — 1 1 → $(110100111)_2$ $\Rightarrow (110100111)_2 = (1A7)_{16}$ - 2	2	2+2+2+2 2 = 8	

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title: Digital Electronics

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
III (b) (i)	NOT operation using NAND gates only  	1		
	(ii) AND operation  	2		
	(iii) OR operation  	2		
	(iv) EX-OR gates operation 	2		
	 Truth table gives the working principle for above gates.		1+2+2+2=7 (8+7=15)	

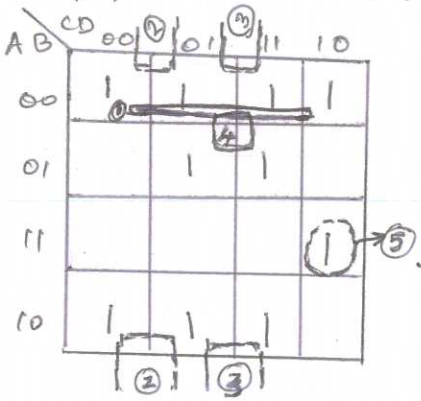
SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
IV (a)	$f(A,B,C,D) = \Sigma m\,(0,1,2,3,5,7,8,9,11,14)$			



Group 1: $\bar{A}\bar{B}\bar{C}\bar{D}$, $\bar{A}\bar{B}C\bar{D}$, $\bar{A}\bar{B}CD$, $\bar{A}B\bar{C}\bar{D}$ → $\bar{A}\bar{B}$

Group 2: $\bar{A}\bar{B}\bar{C}\bar{D}$, $\bar{A}\bar{B}C\bar{D}$, $A\bar{B}\bar{C}\bar{D}$, $A\bar{B}C\bar{D}$ → $\bar{B}\bar{C}$

Group 3: $\bar{A}\bar{B}\bar{C}D$, $\bar{A}\bar{B}CD$, $A\bar{B}\bar{C}D$, $A\bar{B}CD$ → $\bar{B}D$

Group 4: $\bar{A}\bar{B}\bar{C}D$, $\bar{A}\bar{B}CD$, $\bar{A}B\bar{C}D$, $\bar{A}BCD$ → $\bar{A}D$

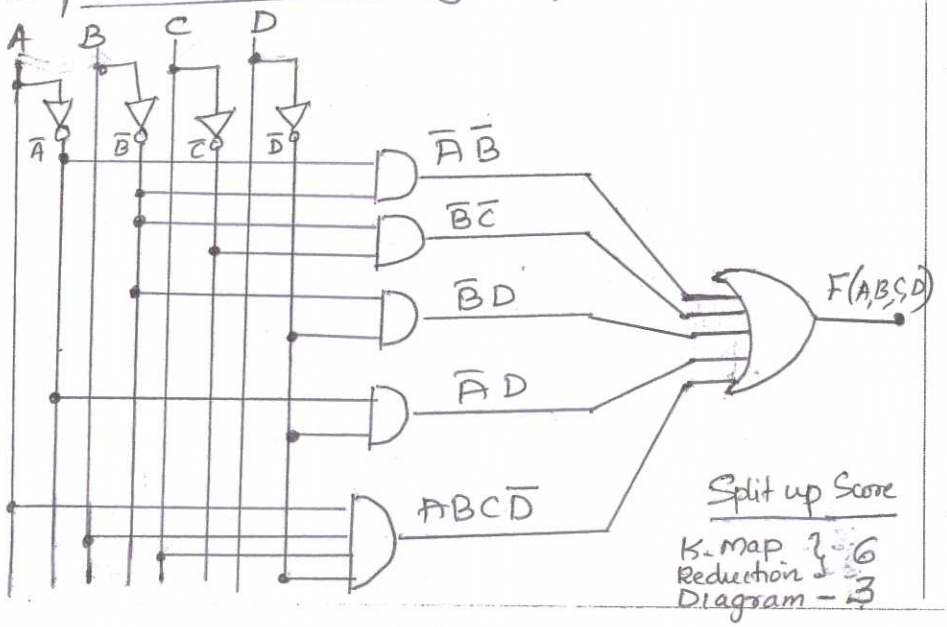
Group 5: $AB\bar{C}\bar{D}$

6

$\therefore f(A,B,C,D) = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{B}D + \bar{A}D + AB\bar{C}\bar{D}$

Implementation using logic gates :

3



Split up Score

K-map → 6

Reduction → 3

Diagram – 3

(6+3)

=9

SCHEME OF VALUATION

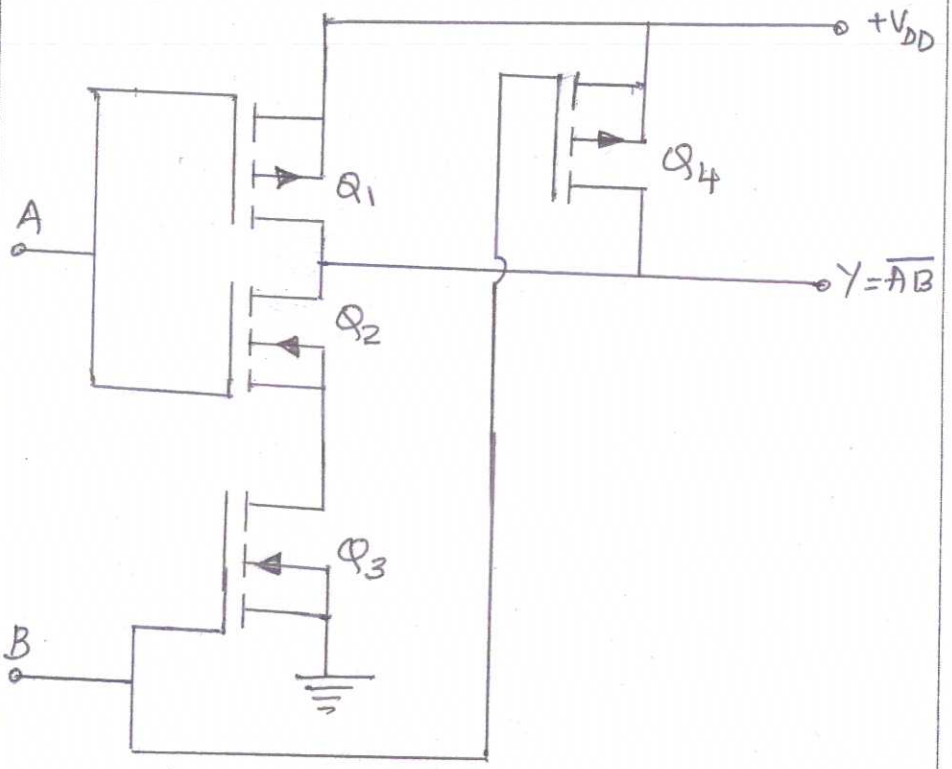
Scoring Indicators

Course code: 304 2		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
IV(b)	The basic laws of Boolean Algebra are: (i) Commutative Law: i.e, $A+B = B+A$ and $A \cdot B = B \cdot A$	2		
	(ii) Associative Law: $(A+B)+C = A+(B+C)$ $(A \cdot B) \cdot C = A \cdot (B \cdot C)$	2		
	(iii) Distributive Laws $A \cdot (B+C) = A \cdot B + A \cdot C$ $(A+B) \cdot C = A \cdot C + B \cdot C$	2	(2+2+2) = 6	(9+6) = 15

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Course Title:		Revision: 2015		
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	UNIT II			
V.a	Circuit diagram of CMOS NAND gate:	4		



Operation: • Circuit consists of two p-type units in parallel and two n-type units in series as shown in figure 4

• When both inputs are HIGH, both p-transistors turn OFF and both n-transistors turn ON. Output is LOW state

• When any input is Low, associated N channel transistor is turned OFF &

SCHEME OF VALUATION

Scoring Indicators

Course code:		Revision: 2015		
Course Title:				
Qn. No.	3042 Scoring indicator	Split up score	Subtotal	Total

p transistor is turned ON. The output is coupled to V_{DD} and goes to HIGH. This functions as NAND gate

(4+4) = 8

V(b) • 4x1 MUX is the circuit which selects one input from 4 inputs and transmits same over a single o/p line. — 3½

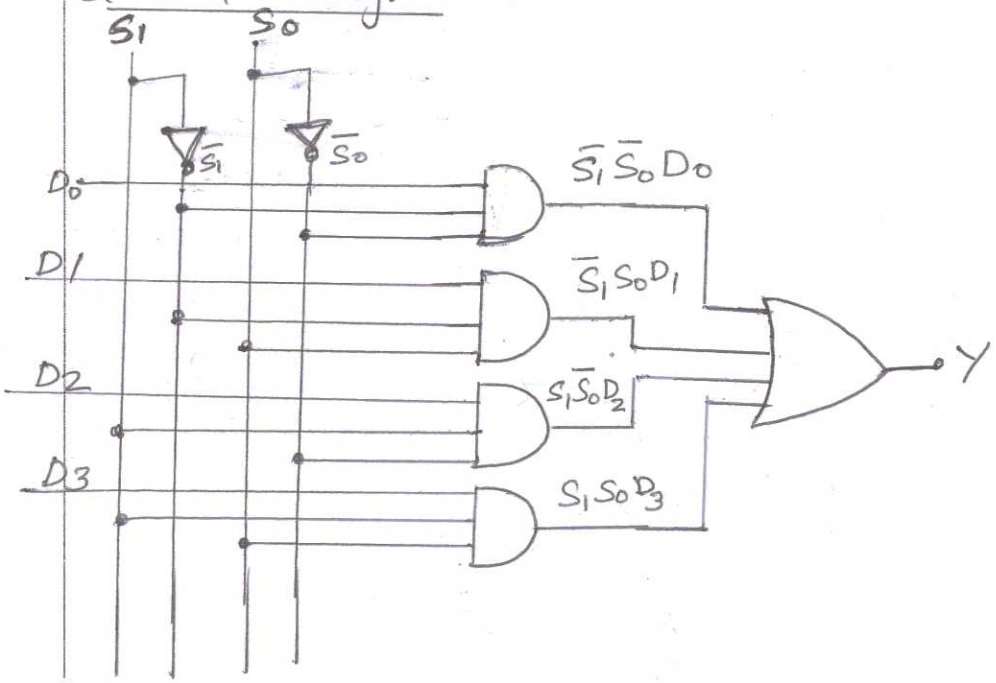
• Truth table ⇒

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

S_1, S_0 → Select lines
$D_0 - D_3$ → input lines
Y → o/p line

Expression, $Y = \bar{S}_1\bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1\bar{S}_0 D_2 + S_1 S_0 D_3$

Circuit diagram :



3½

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	The logic levels applied to S_1 and S_0 determines which AND gate is enabled, so that its data input passes through the OR gate to the output.		$(3\frac{1}{2}+3\frac{1}{2})$ = 7	(8+7) 15
VI(a)	3-bit encoder is a combinational logic circuit. It has 8 inputs and 3 outputs. The circuit accepts an active level on one of inputs and converts it to a coded output (eg: binary)	2		

Truth table ⇒

Decimal Digit	3 bit code C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

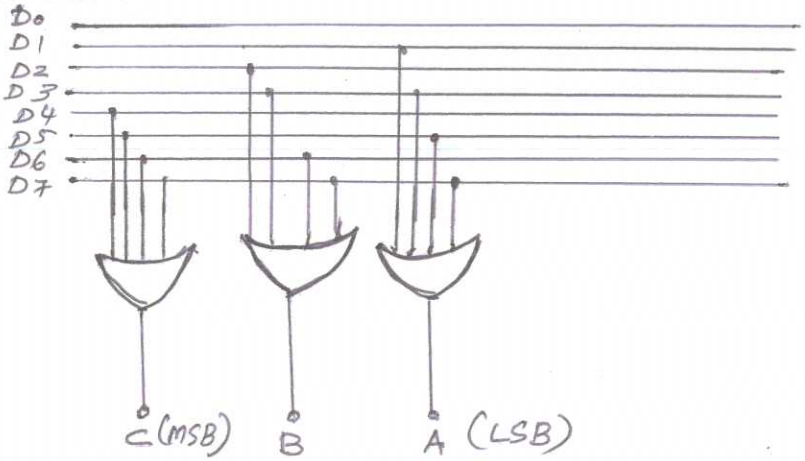
Operation: When one of the decimal digit input lines is at HIGH, the appropriate level occur on the 3 output lines. For eg: If input line 6 is HIGH, o/p ⇒ C=1, B=1 and A=0 Hence 110 is the binary code for decimal 6 — 2

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	Logic diagram of 3 bit encoder is shown below:  From truth table, we have $C = D_4 + D_5 + D_6 + D_7$ $B = D_2 + D_3 + D_6 + D_7$ and $A = D_1 + D_3 + D_5 + D_7$ which is implemented in above logic diagram.	4	(2+2+4) = 8	
VI(b)	Full Subtractor is a combinational logic circuit which can subtract 3-bit at a time. It has 3 i/ps and 2 o/ps (Difference, D and borrow, B_0) Expression for o/ps Difference $D = A \oplus B \oplus C$ Borrow $B_0 = \bar{A}B + (\overline{A \oplus B}).C$			

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	Truth table:			

A	B	C	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

2

Circuit diagram Design

From truth table

2

Difference $D = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C$

Borrow, $Bo = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

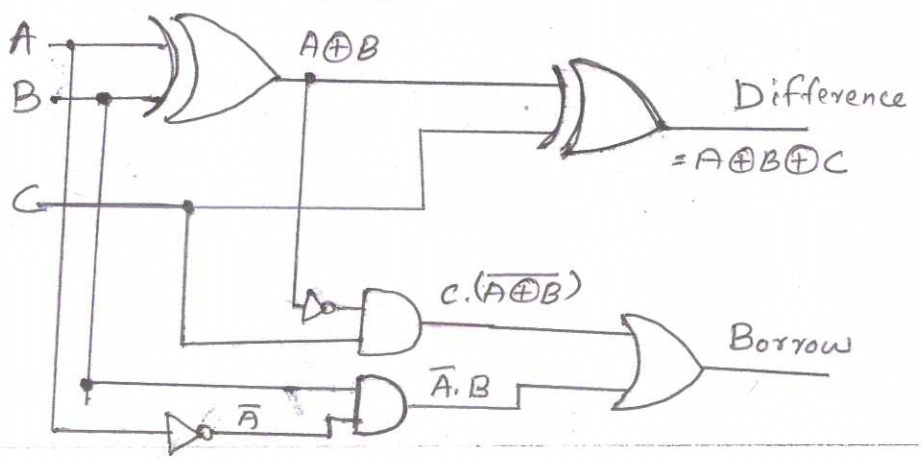
$= \bar{A}\bar{B}C + \bar{A}B(C+\bar{C}) + ABC$

$= \bar{A}B + (\bar{A}\bar{B} + AB)C$

$= \bar{A}B + C(\overline{A \oplus B})$

Circuit Diagram

3



(2+2+3)= 7

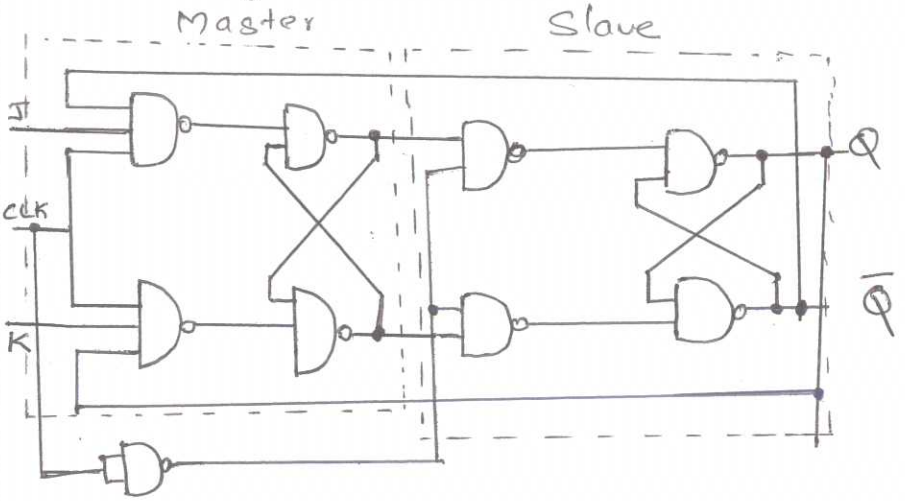
(8+7)= 15

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042	Revision: 2015
Course Title:	

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	UNIT III			
VII (a)	Circuit diagram of Master Slave JKFF			



4

Operation:

- There are 2 flipflops – Master and Slave flipflops.
- Whenever clock is HIGH, master is active and when clock is LOW slave flipflop is active
- According to the data inputs, the output of master is set or reset.
- The information at J and K inputs is transmitted to master flipflop on positive edge of a clock and pass through slave after the arrival of negative clock edge.

3

The entire logical operation is summarised in the truth table below.

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total

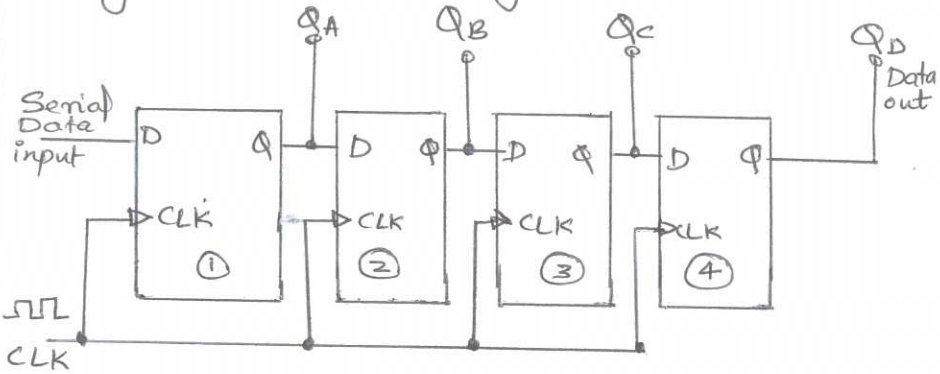
Inputs			Outputs		Mode of operation
CLK	J	K	Q	$\overline{Q}$	
⎍	0	0	Q_0	$\overline{Q}_0$	No change
⎍	0	1	0	1	RESET
⎍	1	0	1	0	SET
⎍	1	1	Q_0	Q_0	TOGGLE

2

(4+3+2) = 9

VII (b)

- A shift register which moves the stored bits towards 'right' side is known as shift right register. Figure shows a right shift register.



3

Operation :- The Q output of each flipflop is connected to D input of the flipflop at right side.

- Each clock pulse shifts the contents of the register one bit position to the right.

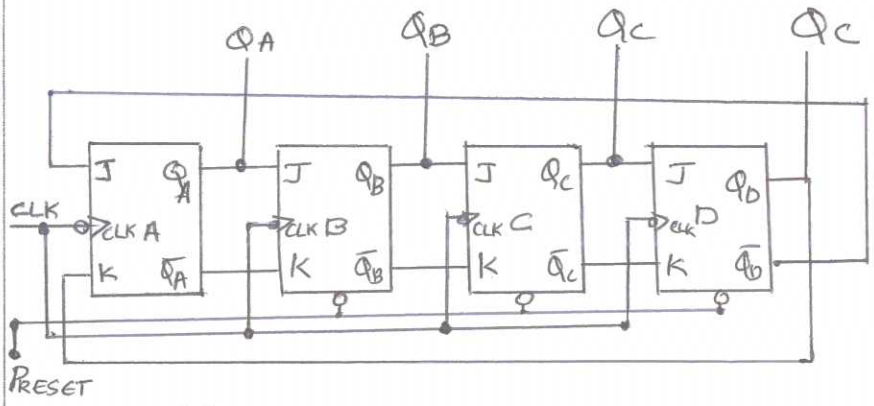
3

- On the fourth clk pulse, the fourth bit of the given word is entered into

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	first flipflop and contents from first flipflop moves to second flipflop and so on.		(3+3) = 6	(9+6) = 15
VIII (a)	Circuit operation of Johnson Counter can be explained with given diagram			



4

Operation

- Here Q and $\bar{Q}$ outputs connected to J and K inputs of the next flipflop and the outputs from last flipflop are crossed over and then connected to first flipflop
- Initially Q_D is 0 and Q_A is 1 and other flipflop remains in RESET state.
- On the 2nd clock pulse Q_A and Q_B are 1 and Q_C and $\bar{Q}_C$ in RESET. 3
- On the 3rd clock pulse flipflop C also set and flipflop D in RESET

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total

- During 4th pulse Q_D also Sets.
- During 5th pulse, $\overline{Q}_D = 0$ then flip-flop A resets and process continues.

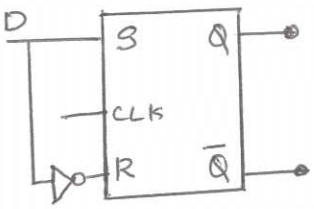
Truth table is shown below

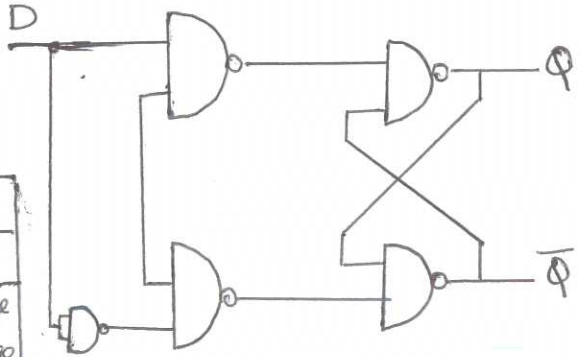
State	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

2

(4+3+2) = 9

VIII(b) Logic Circuit of D Flipflop is shown:





Truth Table

Inputs		Output	
CLK	D	Q	$\overline{Q}$
0	0	No change	
0	1	No change	
1	0	0	1
1	1	1	0

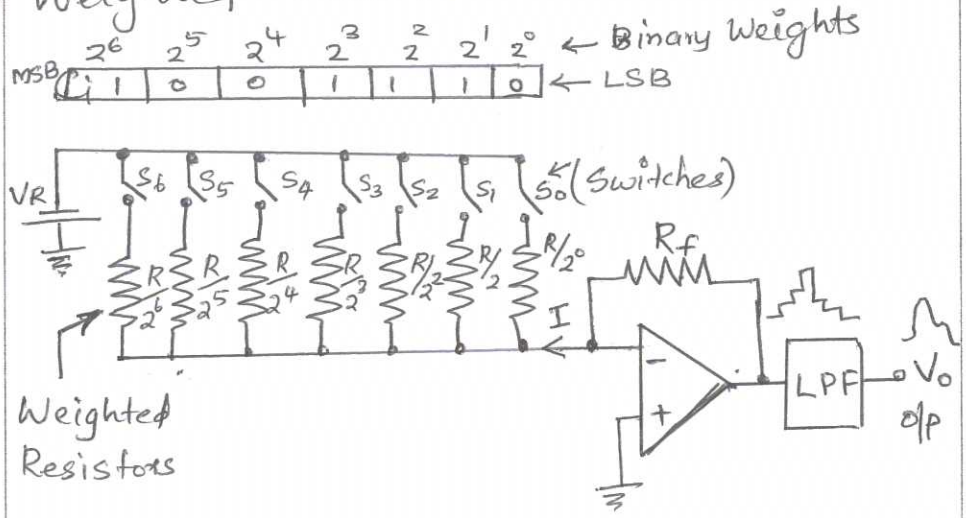
3

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	Operation: • As long as CLK is at Low level, the output is 'no change' condition whatever the value for input D is. • When CLK is HIGH, input D controls output Q. If D = 0, the output Q goes to 0 and DFF in RESET state • When CLK is HIGH and D i/p also HIGH, then out-put Q goes to 1 and DFF in Set state.	3	(3+3) = 6	(9+6) = 15
	UNIT IV			
IX(a)	Weighted Resistor DAC 	4		
	Working: In this Resistance values are weighted according to binary weights.			

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total

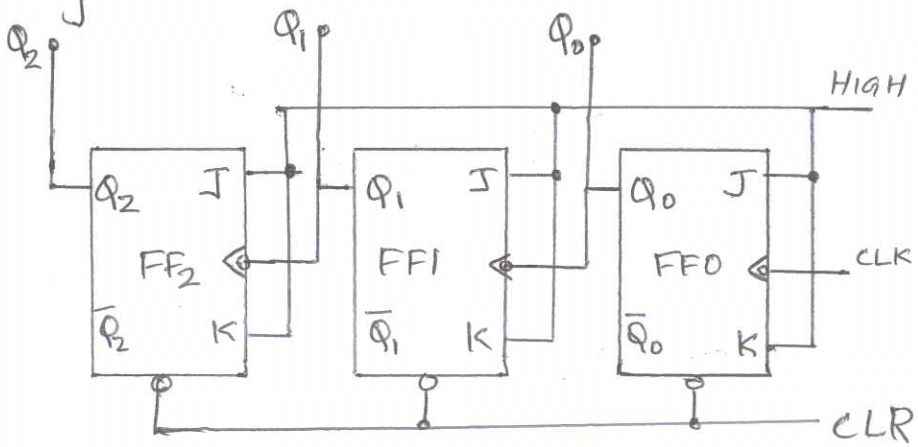
- The logic voltage levels of binary numbers are used to operate switches connected in series with resistors. — 4
- When any bit is 1, corresponding switch is closed to V_R. The binary number to be converted is applied to switches, so that a current I proportional to binary number is given out.
- This current is converted to output voltage through OP-AMP It is then filtered to get analog signal.

The Current $I = \frac{V_R}{R}\left(2^6 S_6 + 2^5 S_5 + 2^4 S_4 + 2^3 S_3 + 2^2 S_2 + 2 S_1 + S_0\right)$

Output $V_0 = -I \cdot R_F = -\frac{V_R \cdot R_F}{R} \cdot I$

4+4 = 8

18(b) Asynchronous Counter (3 bit)



3

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042 Revision: 2015

Course Title:

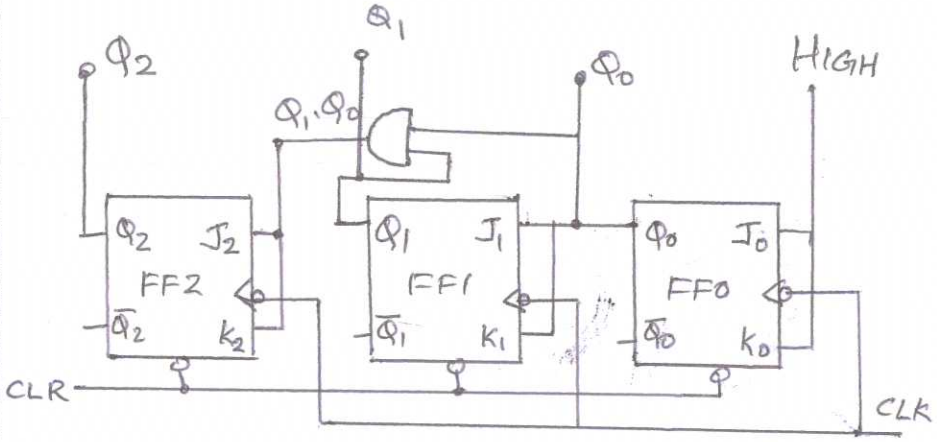
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	Working • Reset all flipflops by applying clear pulse • When first clock pulse is applied at FF0, then Q_0 toggles from 0 to 1. • When second pulse is applied at FF0 its output again toggles from 1 to 0. • This change of output (Q_0) act as clock input to FF1 and its o/p changes to 1 from 0. • This continues for each clock pulse and transition of o/p from 1 to 0 of Q_1 changes Q_2 output of FF2. • For the seventh clock pulse output $Q_2Q_1Q_0 = 111$ Count sequence is given below	4	(3+4)= 7	(8+7)= 15

Clk pulse	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1
8	0 0 0

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
X(a)	Mod - 8 Synchronous Counter			



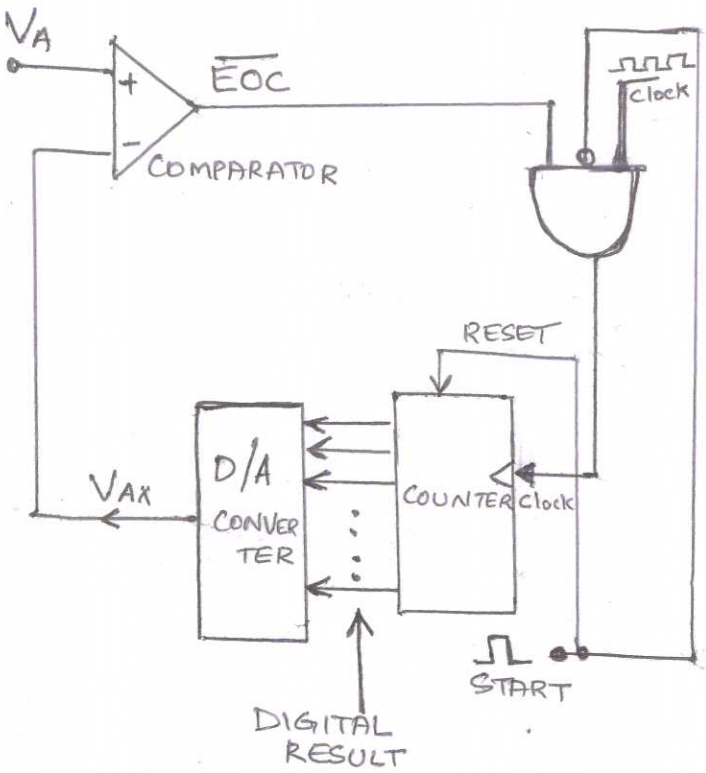
4

Working:

- Connect J_0 and k_0 of first flipflop to HIGH (1).
- To start counting apply clear pulse to all flipflops to make $Q_2Q_1Q_0 = 000$
- On applying first clock pulse to FF_0 Q_0 toggles to 1 from 0. Hence $J_1 = k_1 = 1$ and output Q_1 toggles to 1 from 0 of second flipflop (FF1) on second clock pulse. 4
- On next clock pulse Q_1 again toggles and this continous.
- The output of third flipflop Q_2 changes to 1 when both Q_0 and Q_1 equal to 1 i.e, $J_2 = K_2 = Q_0 \cdot Q_1$
- The counting proceeds this way

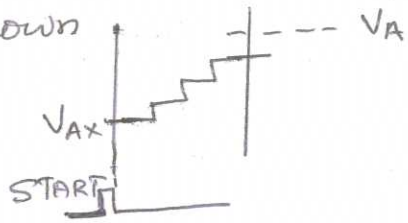
SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	until $Q_2Q_1Q_0 = 111$ on the 7th clock pulse and on next clock pulse all flipflops would reset.		4+4 = 8	
X(b)	Counter Type DAC			
		3		
	Operation : Let V_A be the analog voltage (input) to be converted. following are the steps for conversion	4		
	1. START pulse is applied to reset the counter to zero. High at			

SCHEME OF VALUATION

Scoring Indicators

Course code: 3042		Revision: 2015		
Course Title:				
Qn. No.	Scoring indicator	Split up score	Subtotal	Total
	START also inhibits clock pulses from passing through AND gate into counter. 2. With all 0's at its input, DAC's output will be $V_{AX} = 0V$ 3. Since $V_A > V_{AX}$, comparator output $\overline{EOC} = 1$ 4. When START = LOW, AND gate is enabled and clock pulses get through to the counter 5. As the counter advances, DAC output V_{AX} increases one step at a time as shown  6. When $V_{AX} > V_A$, $\overline{EOC}$ = Low and Counter will stop counting. 7. Counter will hold the digital value untill next START pulse initiates a new conversion.		(3+4)= 7	(8+7)= 15