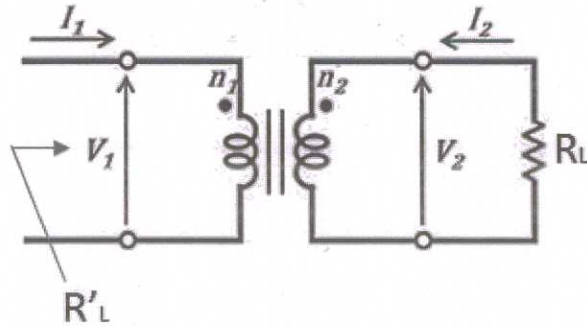


SCHEME OF VALUATION

(Scoring Indicators)

Revision: 2015		Course Code: 3044		
Course Title:		ELECTRONIC DEVICES AND CIRCUITS		
Qn. No.	Scoring Indicator	Split Up Score	Sub Total	Total
Part A				
I.1	Bandwidth of an amplifier is defined as the range of frequencies for which the gain of an amplifier is greater than or equal to 70.7% of the maximum gain.	2	2	10
I.2	Q-point must be stabilized to make it independent of temperature and transistor parameters.	2	2	
I.3	The ratio of inductive reactance to resistance in a resonant circuit is called its quality factor. (Quality factor $Q = X_L/R$)	2	2	
I.4	If the net input signal increases as a result of feedback, such a feedback is called positive feedback. (If the feedback signal is in-phase with the input signal, such a feedback is called positive feedback)	2	2	
I.5	Input voltage at which the output of a Schmitt trigger circuit switches from High to Low is called lower threshold point (LTP).	2	2	
Part B				
II.1	<p>Features</p> <ol style="list-style-type: none"> 1. Very high input resistance. 2. Very low output resistance. 3. High current gain. 4. Unity voltage gain. <p>Applications</p> <ol style="list-style-type: none"> 1. It is commonly used as an impedance matching circuit. 2. Used as a buffer amplifier. 3. Used to provide current amplification with no voltage gain. <p>(Any six)</p>	6	6	30
II.2	A transformer used for impedance matching is shown in figure. R_L is the load connected to the secondary. Let R_L' be the reflected load at the primary. Let the turns ratio be $N_1:N_2$. I_1 and V_1 are the	6	6	

primary current and voltage. I_2 and V_2 are the secondary current and



voltage. Then

$$\begin{aligned} \frac{R_L'}{R_L} &= \frac{\frac{V_1}{I_1}}{\frac{V_2}{I_2}} \\ &= \frac{V_1}{V_2} \times \frac{I_2}{I_1} \\ &= \frac{N_1}{N_2} \times \frac{N_1}{N_2} \\ &= \left(\frac{N_1}{N_2}\right)^2 \\ R_L' &= \left(\frac{N_1}{N_2}\right)^2 \times R_L \end{aligned}$$

Whatever be the value of R_L , the value of the reflected load R_L' is decided by the turns ratio N_1/N_2 . Thus by choosing a transformer with suitable turns ratio, any load impedance can be matched with the output impedance of the amplifier.

II.3

At resonance,

$$\begin{aligned} XC &= XL \\ 2\pi frL &= \frac{1}{2\pi frC} \\ fr^2 &= 1/4\pi^2 LC \\ fr &= 1/2\pi\sqrt{LC} \end{aligned}$$

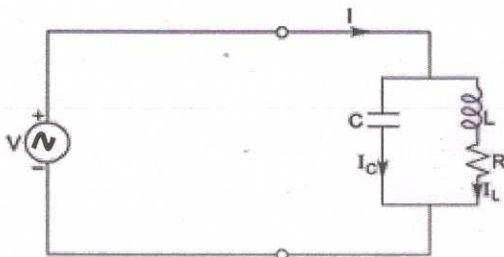
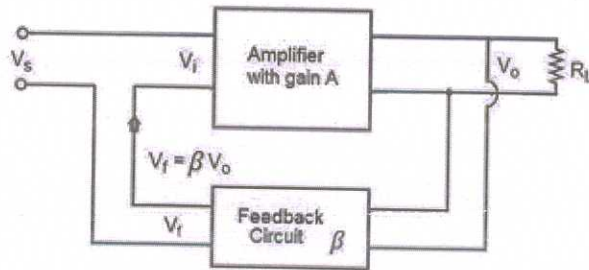


Fig:3
Derivation:3

6

II.4

The block diagram of a feedback amplifier with negative feedback is shown in figure. 'A' is the open loop gain of the amplifier and 'β' the feedback factor.



Here V_s is the applied input voltage and V_i the net input to the amplifier. V_o is the output voltage with feedback and V_f the feedback voltage. Since the feedback is negative, V_f has a polarity opposite to that of V_s .

$$\therefore V_i = V_s - V_f$$

Gain of the amplifier with feedback, $A_f = \frac{V_o}{V_s}$

$$\begin{aligned} V_o &= AV_i \\ &= A(V_s - V_f) \\ &= A(V_s - \beta V_o) \\ V_o &= AV_s - A\beta V_o \end{aligned}$$

$$V_o + A\beta V_o = AV_s$$

$$V_o (1 + A\beta) = AV_s$$

$$\therefore \frac{V_o}{V_s} = \frac{A}{(1 + A\beta)}$$

ie, $A_f = \frac{A}{(1 + A\beta)}$

Fig:2
Derivation:4

6

II.5

BJT	JFET
1. Bipolar device	Unipolar device.
2. Current controlled device	Voltage controlled device.
3. Noisy	Low noise device.
4. Low input impedance	High input impedance
5. Low package density	High package density due to lesser size.
6. Intermodulation distortion is present	No intermodulation distortion.
7. Less thermal stability	Better thermal stability.

(Any 6)

6

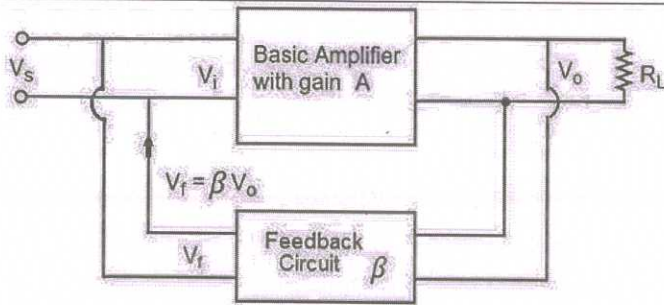
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II.6

Basically oscillators are amplifiers with positive feedback and loop gain equal to one.

Fig:2
Expl:4

6



The expression of the gain of a feedback amplifier with positive feedback is given by

$$A_f = \frac{A}{(1 - A\beta)}$$

If the loop gain $A\beta = 1$, then the gain

$$A_f = \frac{A}{0} = \infty$$

ie, $\frac{V_o}{V_s} = \infty$

ie, $V_s = 0$

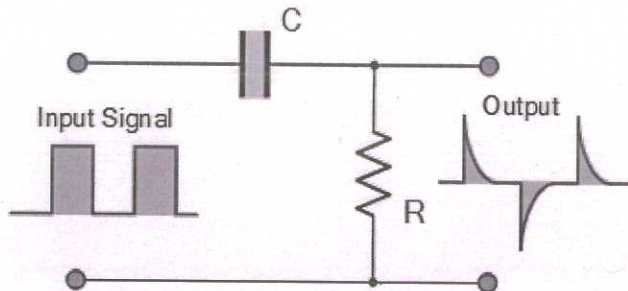
Gain equal to infinity means the circuit no longer works as an amplifier, but gives output without an input ($V_s = 0$). That is the circuit is generating a signal and thus works as an oscillator.

Thus the necessary condition for an amplifier to work as an oscillator is that it should have positive feedback and the loop gain $A\beta$ should be equal to 1.

II.7

The circuit diagram of a RC Differentiator is shown in figure. The RC time constant of the circuit is very much less than the time period of the input signal.

$$RC = 0.0016T \text{ and the reactance } X_C \gg R$$



Let a square wave signal of sufficient time period is applied to the input. Initially the voltage across the capacitor is zero. When the square wave signal goes up, the sudden change in voltage passes through the capacitor and reaches the output as a positive pulse. As the RC time constant is very small, the capacitor instantly charges to the peak input voltage. As the capacitor charges, the output voltage drops simultaneously and reaches zero volt as $V_o = V_i - V_c$. When the

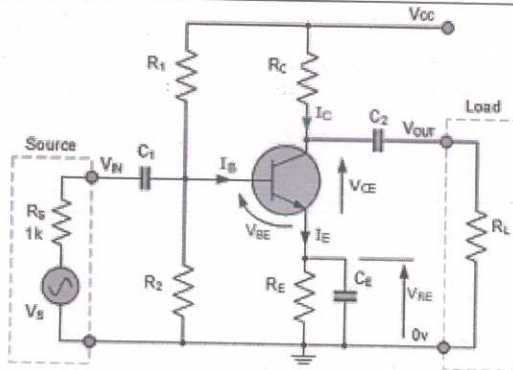
Fig(Ckt + waveform):3
Expl:3

6

square wave signal goes down, the entire voltage across the capacitor appears at the output as a negative pulse ($V_o = 0 - V_c$). The capacitor instantly discharges and the output again reaches back to the zero level. Thus a pulse waveform is obtained at the output with a positive pulse at the leading edge and a negative pulse at the trailing edge.

III.a

Part C



R_1 and R_2 are the biasing resistors. R_E stabilizes the collector current. R_C acts as the load resistor along with R_L . C_1 and C_2 are the coupling capacitors that block DC and pass AC signals. C_E is the emitter bypass capacitor.

When an input AC signal is applied to the input, it gets added up with the base voltage. This results in fluctuations in the base emitter voltage V_{BE} and base current I_B . Variation in I_B causes large variations in I_C , since $I_C = \beta I_B$. Varying I_C also causes variation in the voltage drop across R_C and thus variation in collector voltage. Fluctuating collector voltage has a DC component and an AC component. The coupling capacitor C_2 passes only the AC component to the output load resistor. This AC signal will be an amplified version of the input AC signal but with 180° phase difference.

Waveform

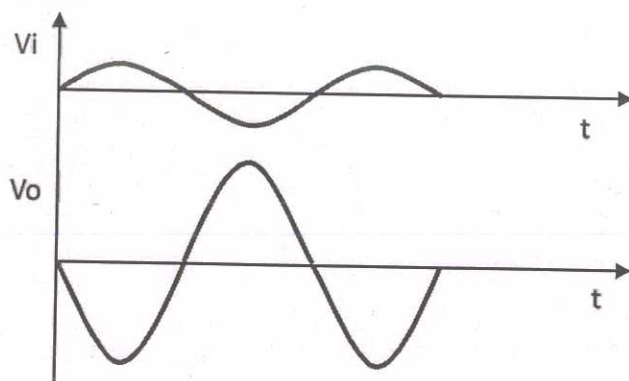
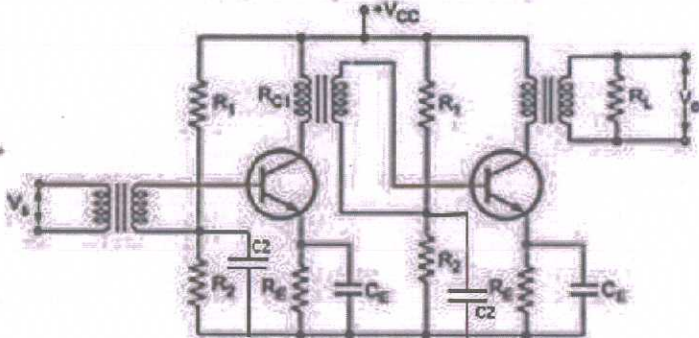


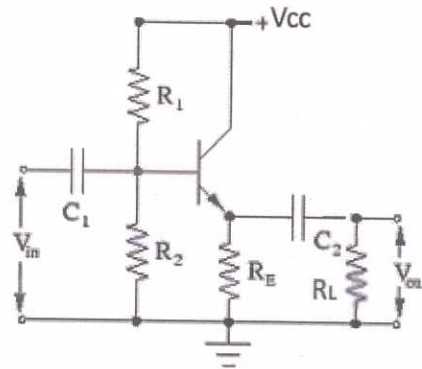
Figure- 4
Expl- 4
Waveform-1

9

15

III.b	Particulars	RC Coupling	Transformer Coupling	Direct Coupling	6	6	
	Frequency Response	Very good in AF range	Poor	Best			
	Size	Small	Most	Least			
	Impedance Matching	Poor	Very good	Good			
	Cost	Low	High	Least			
	Application	Voltage amplifier	Power amplifier	DC amplifier			
IV.a	<p>The circuit diagram of a transformer coupled amplifier is shown in figure. Here the signal from one stage to the other is coupled through mutual induction. Since the primary and the secondary windings of a transformer are electrically isolated, it prevents dc passage and thus preserves the dc conditions of the circuit. Transformers also have excellent impedance matching properties.</p> 				Fig:5 Expl:4	9	15
	<p>Transformer T1 couples the signal from the source to the input of the first amplifier stage. The amplifier amplifies the signal and the amplified signal appears across the primary winding of transformer T2 which acts as the load impedance. T2 couples this signal to the secondary winding and the input of the next stage through mutual induction. The second stage again amplifies this signal and the final amplified signal appears across the primary winding of T3. This signal is coupled to the load resistor again through mutual induction.</p> <p>Frequency response of transformer coupled amplifiers are not linear. They make sharp peaks at certain frequencies. They are usually used as tuned amplifiers at radio frequency range.</p>						
IV.b	The circuit diagram of an emitter follower is shown in figure. Here the transistor is working in common collector configuration. R_1 and R_2 are the biasing resistors that fixes the base voltage. R_E sets the				Fig:3 Expl:3	6	

emitter current, stabilizes I_C and acts also as the load resistor along with R_L .



When the input AC signal is applied to the input, due to the clamping action of C_1 , the signal gets added up with the base voltage. This causes the base voltage to vary in accordance with the variation in the input signal. Variations in base voltage causes variations in base emitter voltage V_{BE} and base current I_B . Variations in I_B causes variations in I_E , the emitter current. Variation in I_E causes the voltage drop across R_E to vary. The coupling capacitor C_2 passes this variation in voltage to the load resistor R_L .

Since the output voltage (ac emitter voltage) is always less than the input voltage (ac base voltage) due to a small ac voltage drop across the base emitter junction, the gain of the amplifier is always less than but almost equal to 1.

V.a

A single tuned amplifier uses a single tuned circuit as its load impedance. The circuit is similar to a normal CE amplifier with the collector resistor R_C replaced by a single tuned circuit. The tuned circuit is tuned to the centre frequency of a particular band to be amplified. The amplifier provides sufficient gain only for that particular band and so rejects all other frequencies.

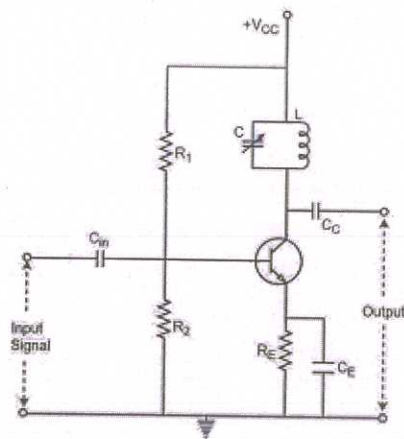
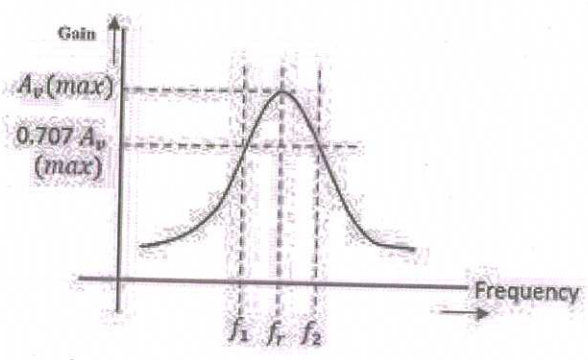


Fig:4
Expl:3
FR:1

8

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The centre frequency is decided by the value of the inductance and capacitance in the parallel tuned circuit. The parallel tuned circuit has very high impedance at the resonant frequency which sharply decreases as the frequency moves away from that frequency. The gain of the amplifier, which depends on the value of the load impedance, just follows the variations in the load impedance. So the amplifier provides high gain at the resonant frequency and the gain sharply decreases as the frequency moves away from the resonant frequency.



V.b

Single ended power amplifier is a class A power amplifier having a single transistor. The circuit is similar to a single stage CE amplifier with the R_C replaced with a coil. Absence of R_C saves around 40% dc power. The coil acts as the load impedance. Usually the coil is the primary of a step down transformer. Then the load can be connected at the secondary with proper impedance matching. A transistor with high current rating and low output impedance is used in the circuit.

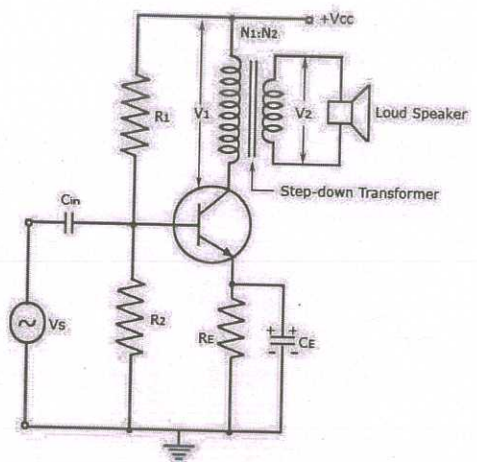
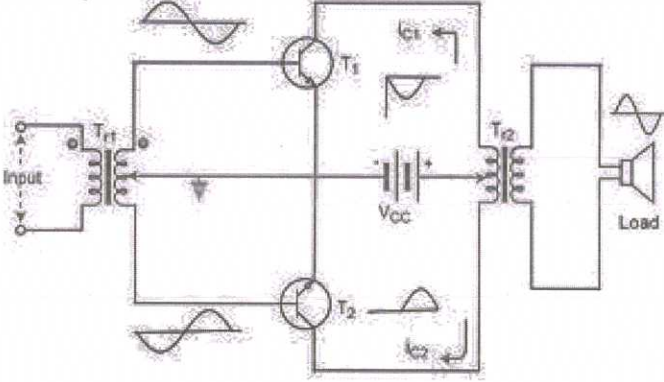


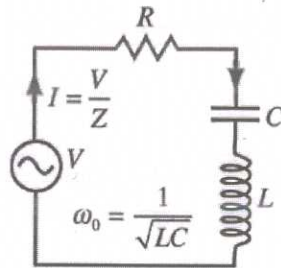
Fig:4
Expl:3

7

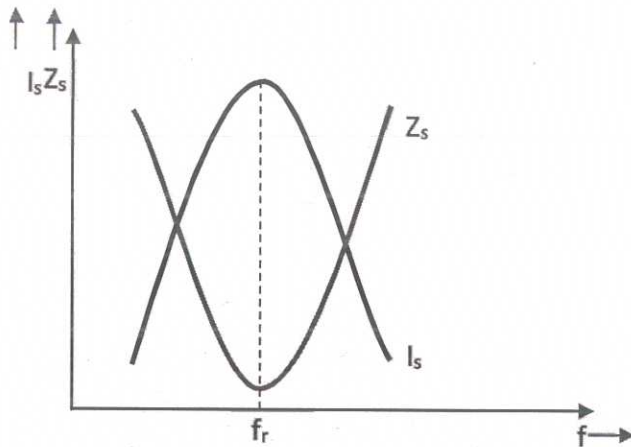
	<p>Input should be a signal with sufficient voltage level to extract maximum power out of the circuit. The amplifier raises the power level of the input signal and it appears across the primary of the transformer. A step down transformer with suitable turns ratio transfers this power to the load without any loss.</p> <p>As the circuit draws constant average dc power irrespective of the input signal strength, the wastage is more and the efficiency is poor. Theoretically the efficiency is 50% and practically much less than that.</p>			
VI.a	<p>Push pull power amplifier circuit has two parallel amplifiers. A driver transformer derives two identical and 180° out of phase signals from the input signal to feed these amplifiers. One of the amplifier amplifies the positive half cycles of the input signal and the other the negative half cycles. The amplified half cycles are then combined by an output transformer to reconstruct the complete cycle. In a class B amplifier, when one amplifier is active the other remains cut off.</p>  <p>During positive half cycle of the input, the base emitter junction of T_1 is forward biased and it conducts. The base emitter junction of T_2 is reverse biased by the inverted input signal and it remains cut off. Current flows upwards through the upper half of the primary winding of output transformer. An amplified half cycle is obtained at the output through mutual induction.</p> <p>During negative half cycle of the input, T_2 conducts and T_1 remains cut off. This time the current flows downwards through the lower half of the primary winding of output transformer. An amplified half cycle, which is just opposite to the earlier one is obtained at the output. Thus the output transformer combines the two half cycles to obtain the complete cycle.</p>	Fig:4 Expl:4	8	15

VI.b

A circuit in which the inductor and capacitor are connected in series with the signal source is called series resonant circuit. A practical inductor has some resistance. So the circuit behaves as an RLC circuit. Such a circuit is shown in figure.



The inductive reactance $X_L = 2\pi fL$ and capacitive reactance $X_C = \frac{1}{2\pi fC}$ vary with the variation in signal frequency f . Capacitive reactance is higher at low frequencies and inductive reactance at high frequencies. At a particular frequency, f_r , the inductive reactance becomes equal to capacitive reactance. When it happens the circuit is said to be in resonance and f_r is called the resonance frequency. Below f_r , the circuit behaves capacitive and above f_r , it behaves inductive.



At resonance,

$$\begin{aligned}
 XC &= XL \\
 2\pi frL &= \frac{1}{2\pi frC} \\
 fr^2 &= 1/4\pi^2 LC \\
 fr &= 1/2\pi\sqrt{LC}
 \end{aligned}$$

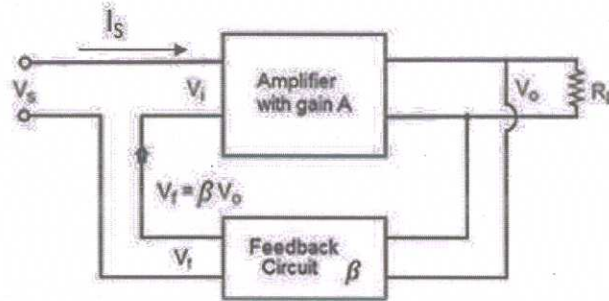
Inductive reactance and capacitive reactance are 180° out of phase with each other. When their magnitudes are equal they cancel each

Fig:3
Expl:4

7

other and circuit becomes a purely resistive network. The total impedance of the circuit is minimum and the circuit current maximum.

VII.a **Negative feedback increases input impedance.**



An amplifier with negative feedback is shown in figure. Let Z_i be the actual input impedance of the amplifier and Z_f the input impedance with feedback. Let I_s be the input current. The net input voltage V_i is given by

$$V_i = V_s - \beta V_o$$

$$V_i = V_s - A\beta V_i \text{ Since } V_o = AV_i$$

$$V_s = V_i + A\beta V_i$$

$$V_s = V_i (1 + A\beta)$$

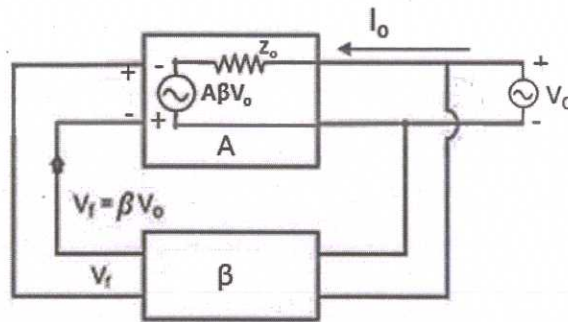
Dividing both sides by I_s gives

$$\frac{V_s}{I_s} = \frac{V_i}{I_s} \times (1 + A\beta)$$

$$Z_f = Z_i (1 + A\beta)$$

Thus by negative feedback, the input impedance is increased by a factor $(1 + A\beta)$.

Negative feedback reduces output impedance.



The output circuit of the feedback amplifier is replaced with its Thevenin equivalent circuit consisting of the voltage source and a series impedance. Here the Thevenin equivalent voltage is ' $A\beta V_o$ ' and Thevenin equivalent impedance is Z_o . For analysing the circuit,

Fig:2
Expl:2

8

15

Fig:2
Expl:2

the output resistance is replaced with a voltage source V_o which sends a current I_o through the circuit. The feedback signal βV_o is the only input.

Applying KVL,

$$V_o = I_o Z_o - A\beta V_o$$

$$V_o + A\beta V_o = I_o Z_o$$

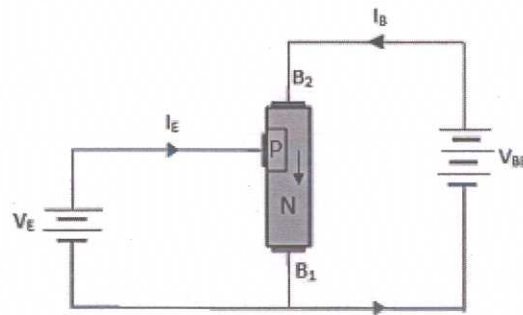
$$V_o(1 + A\beta) = I_o Z_o$$

$$\frac{V_o}{I_o} = \frac{Z_o}{(1 + A\beta)}$$

$$Z_{of} = \frac{Z_o}{(1 + A\beta)}$$

It is evident from the equation that negative feedback reduces output impedance by a factor $(1+A\beta)$.

VII.b



For proper operation, a dc voltage V_{BB} is applied between the two base terminals with the positive terminal of the battery connected to base-2. The emitter terminal is then made positive with respect to base 1 by connecting a battery V_E . Let the emitter voltage is initially zero and gradually increases. The p-n junction remains reverse biased until the emitter voltage reaches a threshold voltage called peak voltage. This is the voltage at which $V_E = 0.6 + \eta V_{BB}$, where $\eta = R_{B1}/(R_{B1}+R_{B2})$. When the p-n junction is forward biased, the heavily doped p-region injects holes into the base. This holes moves to the base-1 region under the influence of V_{BB} . These holes increase the carrier concentration of base-1 region and reduce the resistance. This causes the forward bias to increase and increased carrier injection into the base. The base-1 resistance further decreases. This process goes on like this until the carrier concentration in the base-1 region reaches a saturation level. During this process, the emitter current goes on increasing while the emitter voltage goes on decreasing. Thus the UJT exhibits a negative resistance property during this period. When the base-1 region reaches the saturation level, the emitter voltage reaches the minimum value called the valley voltage. Any further increase in current increases the emitter voltage.

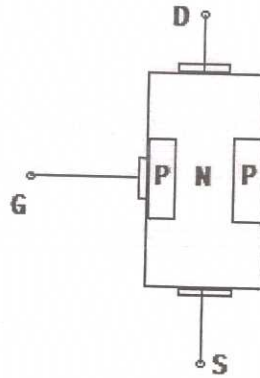
Fig:3
Expl:4

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VIII.a

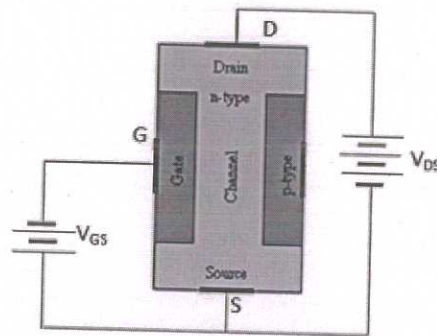
Junction Field Effect Transistor (JFET) is a three terminal semiconductor device. The three terminals are Drain (D), Source (S) and Gate (G). There are two types of JFETs; n-channel JFET and p-channel JFET. The symbols and constructional details are shown in figure.

Figure shows the structure of an n-channel JFET. A lightly doped n-type silicon bar is acting as the channel. Two terminals are attached on either side of the bar called Drain and Source. Two heavily doped p-type regions are formed on either side of the channel by diffusion. These two regions are interconnected and attached a terminal called Gate.



Working:

For proper working, a voltage V_{DS} is applied between the drain and source such that the drain is positive with respect to source. A negative gate to source voltage V_{GS} is applied to the gate. When the gate voltage V_{GS} is zero, the channel is completely open and the drain current I_D flows freely through the channel between the two p-regions. When a gate voltage is applied, the p-n junctions get reverse biased and wedge shaped depletion regions are formed at the p-n junctions which extends more into the channel due to its comparatively light doping. The depletion region is wider at the drain side due to the potential gradient along the length of the channel.

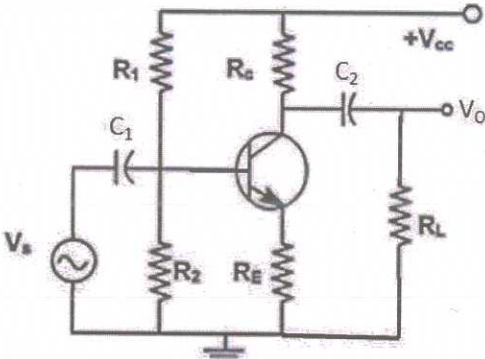


If the drain to source voltage V_{DS} increases, the drain current increases. Also the depletion regions widen due to increased reverse bias and the channel width reduces. The reduced channel restricts the current flow. As V_{DS} further increases, a point reaches when the two wedge shaped depletion regions meet and the channel get completely closed. The drain to source voltage at which this happens is called the pinch off voltage. When the current flow stops, the potential

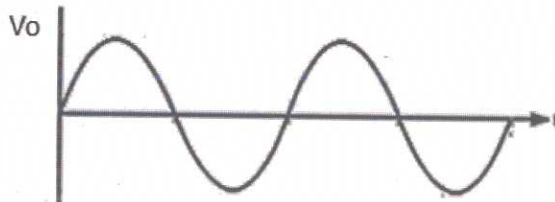
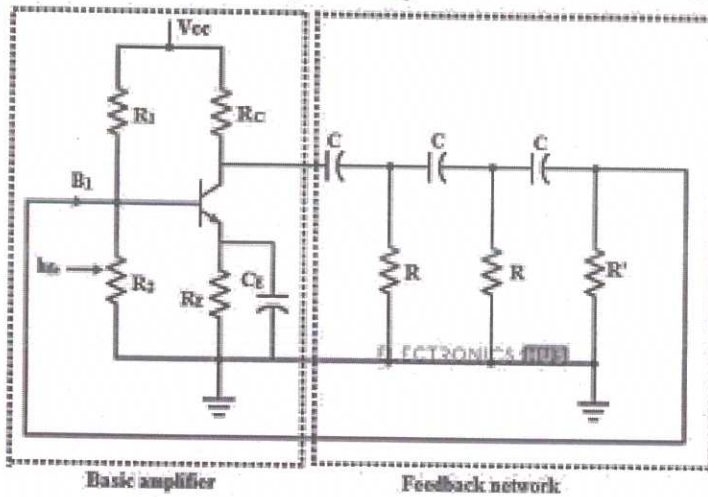
Fig:4
Expl:4

8

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	<p>gradient along the channel disappears and the depletion regions start to become uniform. This causes the channel to open up and the current flow to re-establish. This process repeats. The current never stops but reaches a saturation value. If the gate to source voltage V_{GS} is set at a higher value, the drain current I_D reaches the saturation level at a lesser value of V_{DS}.</p>			
VIII.b	<p>A typical current series feedback circuit is shown in figure. It is a normal CE amplifier circuit except the absence of bypass capacitor C_E. In the absence of C_E, the ac voltage drop $i_E \times R_E$ across the emitter resistor R_E acts as a feedback signal that comes in series with the input voltage V_s. The feedback voltage is opposite in polarity with the input signal and so it is a kind of negative feedback. The feedback voltage is proportional to the output current ($i_E = i_C$) and so it is a type of current feedback.</p> 	Fig:4 Expl:3	7	
IX.a	<p>The circuit diagram of an RC phase shift oscillator is shown in figure. It consists of an amplifier and a feedback network. The amplifier is a common emitter one that produces 180° phase shift. The feedback network consists of three identical RC circuits each of which produces 60° phase shift. Altogether they produce an additional 180° phase shift. The amplifier and the feedback network together produces 360° phase shift or 0° phase shift. Thus positive feedback is ensured. The feedback network produces 180° phase shift only for a frequency</p> $f = \frac{1}{2\pi RC\sqrt{6}}$ <p>Positive feedback happens only at this frequency and it is the frequency of oscillation of the circuit. The feedback factor β of the feedback network is $1/29$. The gain of the amplifier A is made equal</p>	Fig:4 Expl:3 Waveform:1	8	15

to 29 so that the Barkhausen criterion ($A\beta = 1$) is satisfied. The necessary conditions for oscillation are thus satisfied and the circuit works as an oscillator, producing sinusoidal waveform at the output.



IX.b

The circuit diagram of an astable multivibrator is shown in figure. It is a free running oscillator that generates square wave signals. The circuit has two transistors. These transistors work in ON-OFF condition. When one transistor is ON, the other is OFF. So the circuit has two states; State 1: Q_1 ON and Q_2 OFF, State 2: Q_1 OFF, Q_2 ON. The circuit stays in one state for a predefined time and then automatically shifts to the other state. Since the states are temporary, it is called quasi-stable states.

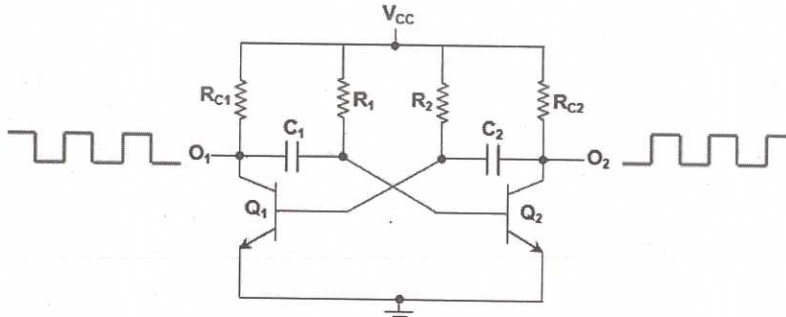


Figure 1 Astable Multivibrator Using BJTs

When the power is switched ON, because of the differences in characteristics, one of the transistors turns ON first causing the other transistor to turn OFF. Let Q_1 is ON and Q_2 is OFF. Now the capacitor C_2 charges to V_{CC} through R_{C2} and base-emitter junction of

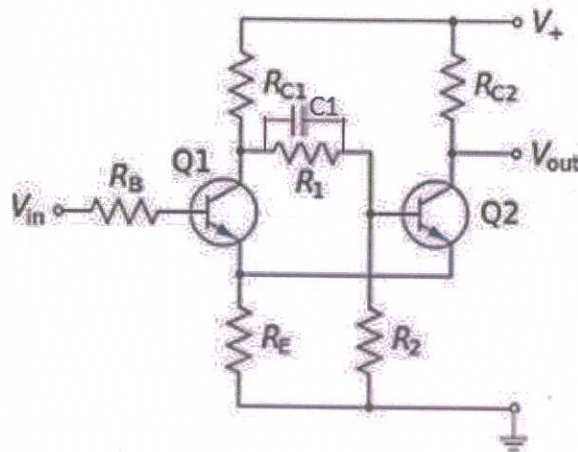
Fig:4
Expl:3

7

Q1. Capacitor C₁, which was charged to -V_{CC} in the previous state now discharges and recharges towards V_{CC} through Q1. But when the voltage across the capacitor reaches 0.6V, transistor Q2 turns ON. When Q2 turns ON, the entire voltage -V_{CC} across C₂ reaches across the base-emitter junction of Q1 and turns it OFF. Now the state has changed and the process repeats. Alternate turning ON and turning OFF of the transistors generates square waves at their collectors.

The expression for the frequency of oscillation $f = \frac{1}{1.38 RC}$ Hz,
where $R = R_1 = R_2$ and $C = C_1 = C_2$

X.a



Schmitt trigger is a circuit that creates rectangular waves from a continuously varying input signal. The output of the circuit goes up when the input voltage reaches a voltage called upper threshold voltage (UTP) and the output goes down when the input voltage goes below a voltage called lower threshold voltage (LTP).

When no input voltage is present, the first transistor Q₁ is OFF and the large collector voltage that reaches the base of Q₂ via the voltage divider network keeps it ON. Now let a continuously varying signal like sinewave is applied to the input. When the voltage at the input crosses a voltage called UTP, T₁ turns ON. Collector voltage of Q₁ drops and this drop in voltage generates a negative pulse that reaches the base of Q₂ through C₁ and turns it OFF. The collector voltage of Q₂ which was almost zero, now rises to V_{CC}. The circuit remains in this state until the input voltage goes below a second threshold voltage called LTP. When this happens, Q₁ turns OFF and the large collector voltage drives Q₂ ON. The collector voltage of Q₂, which is the output, now drops to a low value (V_{CEsat} + V_{RE}). This process repeats.

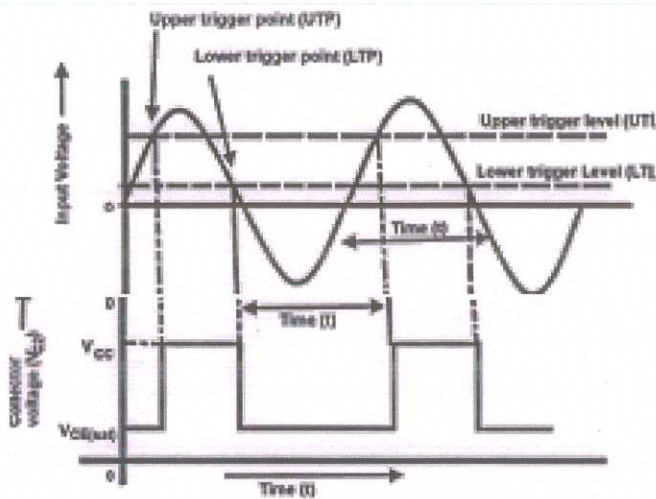
Upper Threshold Voltage, $UTP = V_{BE1} + I_{E2}R_E$

Lower Threshold Voltage, $LTP = V_{BE1} + I_{E1}R_E$

Fig:3
Expl:3
Waveform:2

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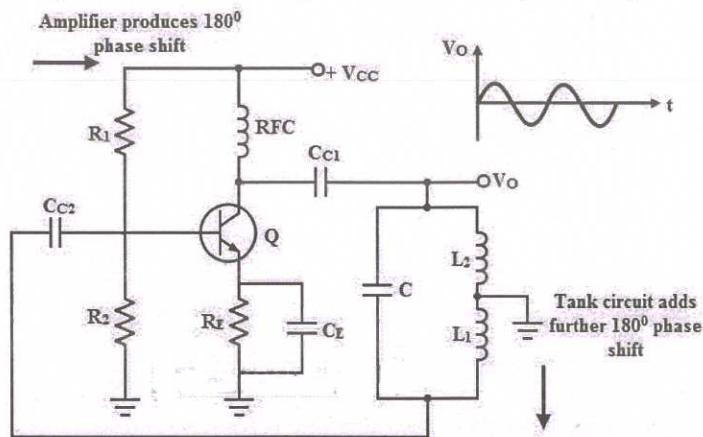
15



Schmitt trigger thus works as a comparator with two reference levels. The voltage difference between these two levels acts as a noise margin.

X.b

The circuit diagram of a Hartley oscillator is shown in figure. It consists of an amplifier and a parallel LC circuit that acts as the oscillating circuit as well as the feedback network. The inductor in the circuit is a split one and the tap is grounded. The tap divides the inductor into two parts, L_1 and L_2 . Grounding the tap makes L_2 part of the output circuit of the amplifier and L_1 the part of input circuit.



When the circuit is switched ON, the collector current builds up from zero to the normal value. This changing current induces a voltage across the radio frequency choke. This energy is then transferred to the LC circuit, as L_2 is part of the output circuit. Oscillations are thus initiated in the LC circuit. A part of this oscillations are fed back to the input as L_1 is part of the input circuit. The amplifier amplifies this signal and supplies it back to the LC tank

Fig:4
Expl:3

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<p>circuit. The voltages across L_1 and L_2 are 180° out of phase with each other. So the feedback is positive (considering the 180° phase shift produced by the amplifier). The value of L_1 and L_2 and the gain of the amplifier are so chosen that the loopgain $A\beta = 1$.</p>			
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The LC tuned circuit receives adequate energy from the amplifier at proper intervals and sustained oscillations are generated.

The frequency of oscillations $f = 1/2\pi\sqrt{LC}$ where $L = L_1 + L_2$.