TED (15/19) – 3131
(Revision – 2015/19)

A23 - 06547

Reg.No……..
Signature……...

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE , APRIL – 2023

COMPUTER ARCHITECTURE

(Maximum Marks : 100) (Time : 3 hours)

PART – A
(Maximum Marks : 10)

Marks

I. Answer **all** questions in one or two sentences. Each question carries 2 marks.

1. Define Interrupt.
2. List any two functions of I/O module.
3. Define tracks and sectors.
4. Define instruction pipelining.
5. Define micro program.

(5x2=10)

PART – B
(Maximum Marks : 30)

II. Answer any **five** of the following questions. Each question carries 6 marks.

1. Draw and explain Von-Neumann Architecture.
2. Explain Advanced DRAM types.
3. Explain physical characteristics of magnetic disk.
4. Explain the I/O module structure with a neat diagram.
5. Write short notes on user visible registers.
6. Draw and Explain the block diagram of control unit.
7. Describe Micro operations.

(5x6=30)

PART – C

(Maximum Marks : 60)

(Answer **one full** question from each unit. Each full question carries 15 marks)

UNIT – I

III. (a) Draw and explain the memory cell structure of Static RAM and Dynamic RAM. (8)

(b) Explain Multiple Bus Hierarchy with diagram. (7)

OR

IV. (a) Explain the elements of cache design. (8)

(b) List and explain the characteristics of computer memory system. (7)

UNIT – II

V. (a) List and explain any four RAID levels. (8)

(b) Explain the working principle of optical disk. (7)

OR

VI. (a) Explain the block diagram of an external device. (8)

(b) Explain Interrupt driven I/O. (7)

UNIT –III

VII. (a) Explain processor organization with the help of a diagram. (8)

(b) Explain control and status registers. (7)

OR

VIII. Explain Data flow in instruction cycle. (15)

UNIT – IV

IX. Explain hardwired implementation and micro programmed implementation of control unit. (15)

OR

X. (a) Explain symbolically the different sequence of events occur during fetch, indirect, interrupt and execute cycle. (10)

(b) Explain multiple processor organization. (5)

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