SCHEME OF VALUATION

(Scoring Indicators)

Revision 2015 Course title MICROCONTROLLER AND INTERFACING			Course Code 4043		
Qust.No.	Scoring Indicator		Split up score	Sub Total	Total
I (1)	**PART A** a) 8 bits Micro Controller b) 16 bits address line c) 64 KB total memory d) 128 bytes internal RAM e) 4 KB internal ROM f) 40 pin DIP IC g) + 5 Volts VCC h) 12 MHZ clock frequency (Approax.) (Any four)		4 X 1/2	2	10
I (2)	MOV A, #FF H MOV P1,A (Port 1 I/P)	MOV A,# 00H MOV P2,A (Port 2 O/P)	1 + 1	2	
I (3)	IP is Interrupt priority register. It is an 8 bits register. Used to prioritise 5 interrupts by using instruction.		2	2	
I (4)	Timer is used to generate time delay. Timer will count internal clock pulses. Counter is used to count external events. Counter will count output pulses from sensor or switch.		1 + 1	2	
I(5)	Used to interconnect microcontroller and peripheral devices. Properly match voltage , current and impedance level between MC and peripherals		1+1	2	
II (1)	**PART B** **MP** All main functional blocks in separate ICs Bulky More power consumption One functional block can be replaced if it is damaged Mainly used for general purpose applications Low speed (With same configuration) **MC** All main functional blocks in single IC package Small in size Less power consumption The whole IC package has to be replaced if any one functional block is damaged Mainly used in embedded system High speed (with same configuration) (Any four)		4 X 1.5	6	

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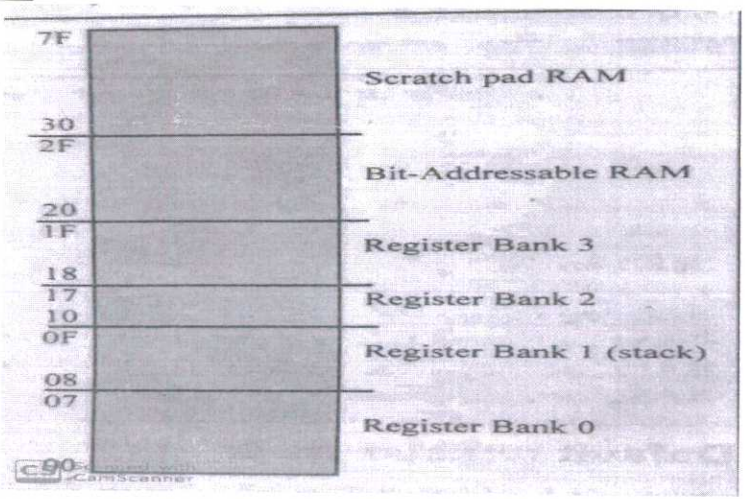
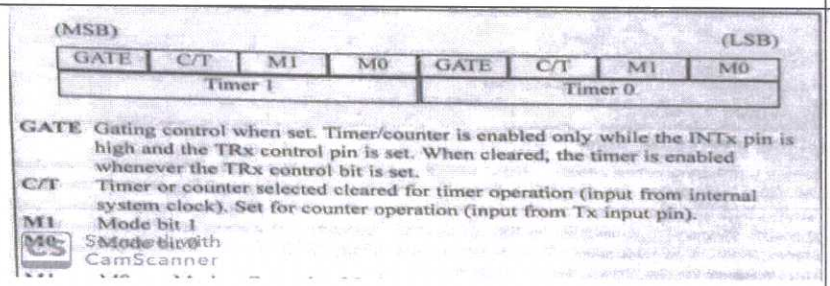
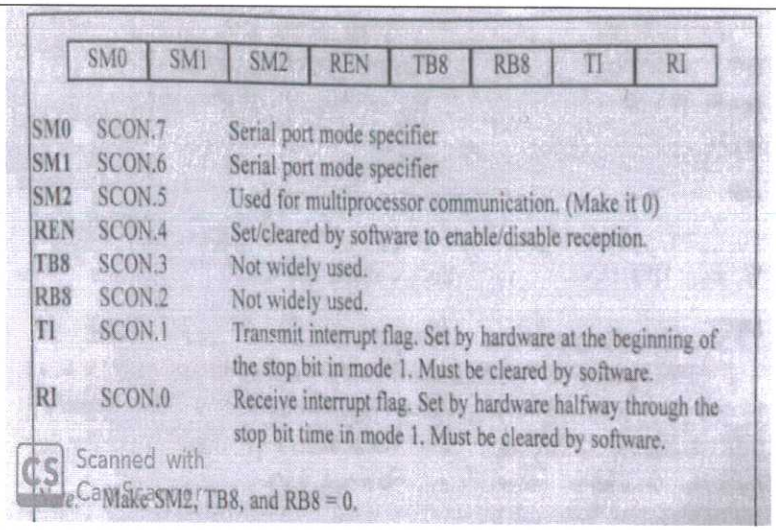
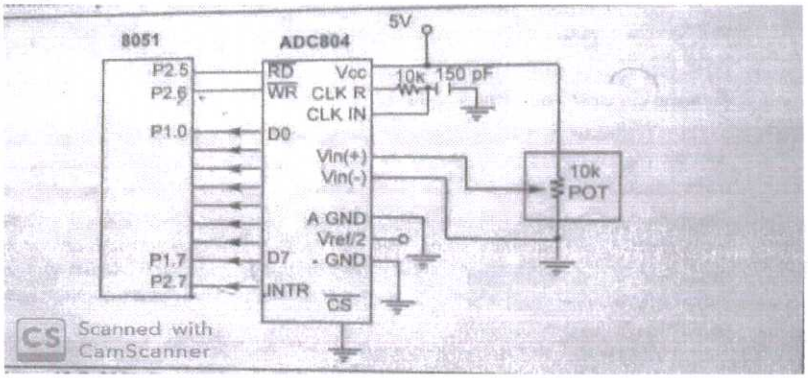
II (2)	**PART B**  - Data memory is 128 bytes capacity (Internal RAM). -A total of 32 bytes location are for register banks and stack -A total 16 bytes are for bit addressable read/write memory -A total of 80 bytes are used for read/write storage(scratch pad).	Fig. 4 + Expln.2	6	10
II (3)	There are six interrupts in 8051 including reset. They are, reset, external hardware interrupt 0(INTO), external hardware interrupt1 (INT1), Timer0 interrupt (TF0), timer1 interrupt (TF1) and serial communication interrupt. Reset is used to initialize the system at the time of power on or going to unknown state. It is having highest priority. INT0 and INT1 are external hardware interrupts. Pin No 12 and 13 in 8051 are used to connect sensors or switches for these interrupts. Timer interrupts flag bits will be set to one when corresponding timer/counter overflows. Serial comm..interrupts are two types-transmit and receive	6 X1	6	

II (4)	MOV A,#08H ; A=08H, diviser
	MOV B, #02H ; B=02 H, dividend
	DIV AB ; A/B, Quotient in A and
	; remainder in B
	MOV DPTR, # 8400 H ; DPTR=8400H
	MOVX @DPTR, A ; Store Quotient in
	;8400 h location
	INC DPTR
	MOV A,B
	MOVX @DPTR,A ; Store remainder in 8401
	END
		Program 4 + Comments 2	6	

II (5)	 (MSB) (LSB) GATE C/T M1 M0 GATE C/T M1 M0 Timer 1 Timer 0 GATE Gating control when set. Timer/counter is enabled only while the INTx pin is high and the TRx control pin is set. When cleared, the timer is enabled whenever the TRx control bit is set. C/T Timer or counter selected cleared for timer operation (input from internal system clock). Set for counter operation (input from Tx input pin). M1 Mode bit 1 M0 Mode bit 0 Scanned with CamScanner MOV TMOD, #0010 0110 B	Format 3+ Instruction 3	6	
II(6)	 SM0 SM1 SM2 REN TB8 RB8 TI RI SM0 SCON.7 Serial port mode specifier SM1 SCON.6 Serial port mode specifier SM2 SCON.5 Used for multiprocessor communication. (Make it 0) REN SCON.4 Set/cleared by software to enable/disable reception. TB8 SCON.3 Not widely used. RB8 SCON.2 Not widely used. TI SCON.1 Transmit interrupt flag. Set by hardware at the beginning of the stop bit in mode 1. Must be cleared by software. RI SCON.0 Receive interrupt flag. Set by hardware halfway through the stop bit time in mode 1. Must be cleared by software. Scanned with CamScanner Make SM2, TB8, and RB8 = 0.	3+3	6	

II (7)	**ADC**  WR Signal used to start conversion (Active low). It is an input to ADC. INTR → End of Conversion. output signal from ADC. Active low. RD → Input Signal to ADC. To read converted data by CPU.	4 X 1.5	6	

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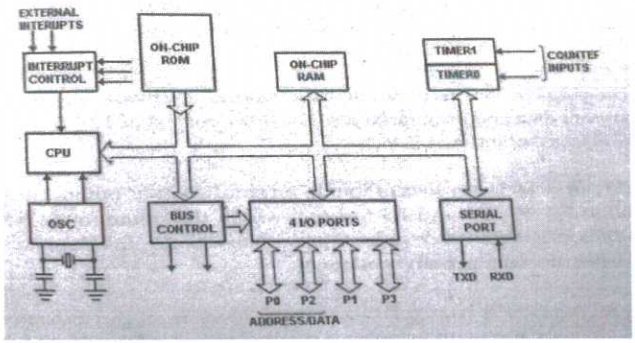
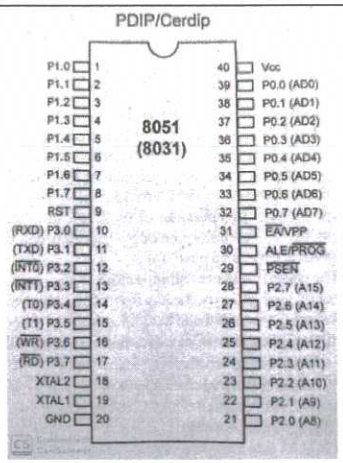
III (a)	PART C  - CPU is the core part - 128 bytes internal RAM. - 4 KB internal ROM - 6 interrupts including reset - 4 parallel input/output ports - One serial port - Two 16 bits timers/counters - Crystal oscilla	Fig 4+ details 4	8	
III (b)	 TxD (Transmit Data) pin is used to transmit data in Serial communication. RxD (Receive data) in Serial Communication.	Fig 4 + Expln.3	7	

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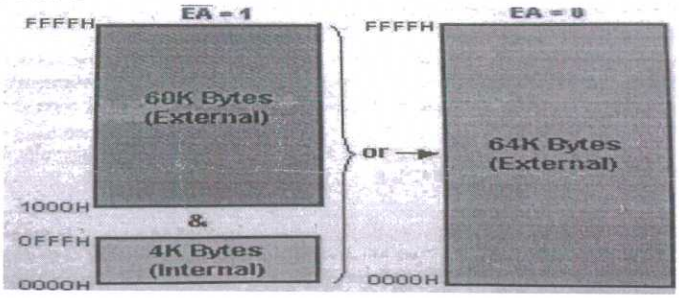
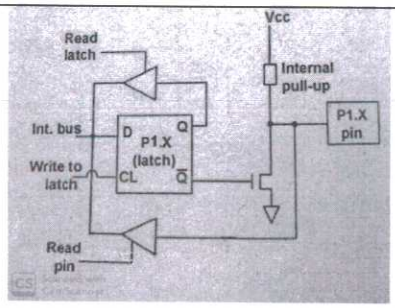
IV (a)	PART C  _There is a 4 KB internal ROM in 8051 -60 KB external ROM can also connect if required -Total 64 KB ROM memory -ROM memory is used to store program codes	Fig 3+ details 3	6	
IV (b)	 - A DFF, 2 buffers, one MOSFET and pull up resistor - If D bit is loaded with bit 1, Q=1, MOSFET off - Port pin will act as input - If D bit is loaded with bit 0, Q=0, MOSFET on - Port bit will act as output port	Fig 5 + Expln.4	9	

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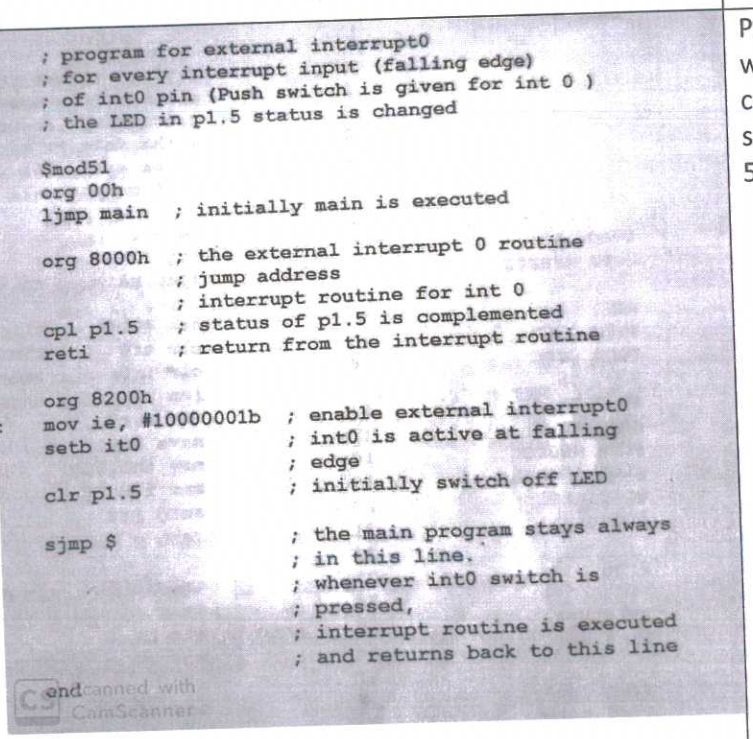
Qust.No.	Scoring Indicator	Split up score	Sub Total	Total
V (a)	PART C Addressing mode is the way or method to access data for CPU processing. There are five addressing modes in 8051. 1 Immediate, 2 Register 3 Direct 4 Register Indirect 5 Indexed Immediate - In this AM, the source operand is a constant. Eg. MOV A, # 25 H, MOV DPTR, # 8200 H Register:- Source and destination operands are registers. MOV B,A Direct addressing mode:- One of the operand is RAM address. Eg MOV A,30H Register indirect addressing mode:- Tow general purpose registers R0 and R1 are used to point RAM memory. Eg MOV A,@R0 MOV @R1,A Indexed Addressing mode:- Used to access data elements of look up table. Eg. MOVC A,@A+DPTR	5 X 2= 10	10	
V (b)	 ; program for external interrupt0 ; for every interrupt input (falling edge) ; of int0 pin (Push switch is given for int 0) ; the LED in p1.5 status is changed $mod51 org 00h ljmp main ; initially main is executed org 8000h ; the external interrupt 0 routine ; jump address ; interrupt routine for int 0 cpl p1.5 ; status of p1.5 is complemented reti ; return from the interrupt routine org 8200h mov ie, #10000001b ; enable external interrupt0 setb it0 ; int0 is active at falling ; edge clr p1.5 ; initially switch off LED sjmp $; the main program stays always ; in this line. ; whenever int0 switch is ; pressed, ; interrupt routine is executed ; and returns back to this line Scanned with CamScanner	Program with commands 5 marks	5	

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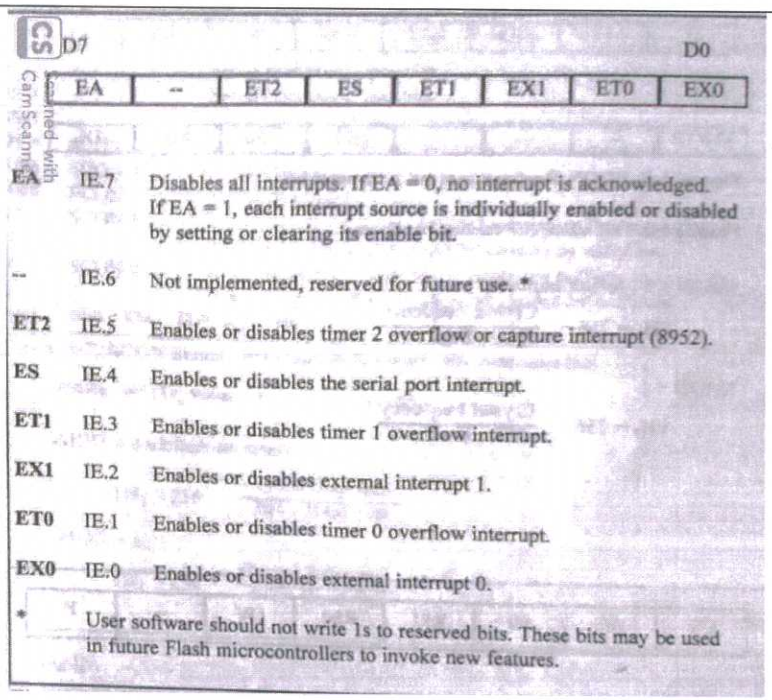
Qust.No.	Scoring Indicator	Split up score	Sub Total	Total
VI (a)	PART C Instruction set 8051 instruction set can be classified into 5 groups. 1 Data transfer 2 Arithmetic 3 Logical 4 Branching or program control 5 Bit manipulation Data transfer:- Eg. MOV A, R2 MOV A,#25H Arithmetic:- Addition , subtraction multiplication, division. Eg. ADD A, R0 SUBB A,R2 MUL AB DIV AB Logical (All logical operations):- ANL A,R3 ORL A,#34H XRL A, @R1 Branching or program control :- Unconditional and conditional JMP LOOP1 JNC LABEL Bit manipulation:- Eg. SETB P1. 5 CLR P1.3	9	9	
VI (b)	 D7 D0 EA -- ET2 ES ET1 EX1 ET0 EX0 EA IE.7 Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit. -- IE.6 Not implemented, reserved for future use. * ET2 IE.5 Enables or disables timer 2 overflow or capture interrupt (8952). ES IE.4 Enables or disables the serial port interrupt. ET1 IE.3 Enables or disables timer 1 overflow interrupt. EX1 IE.2 Enables or disables external interrupt 1. ET0 IE.1 Enables or disables timer 0 overflow interrupt. EX0 IE.0 Enables or disables external interrupt 0. * User software should not write 1s to reserved bits. These bits may be used in future Flash microcontrollers to invoke new features.	3 +3	6	

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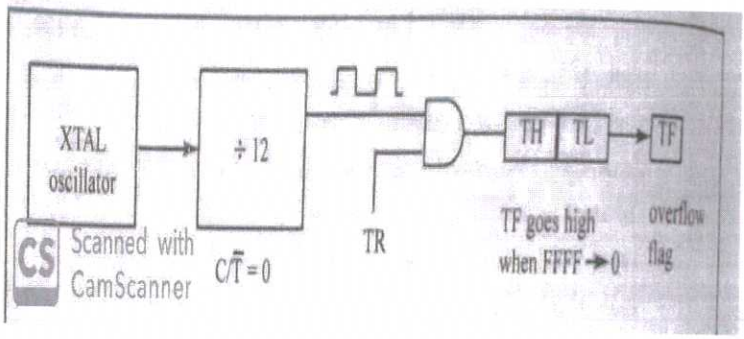
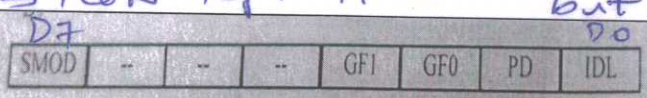
Qust.No.	Scoring Indicator	Split up score	Sub Total	Total
VII (a)	PART C  Cry stal osc. o/p is passed through ÷12 circuit. - C/T̄ bit = 1, Counter mode (T1MOD reg). When C/T̄ = 0, Timer mode. TR → Timer RUN bit → TCON Reg. TF → Timer Flag bit.	Fig 4+ details 4	8	
VII (b)	 Option 1 is not feasible in many situations since the system crystal is fixed. More importantly, it is not feasible beause the new crystal may not be compatible with the IBM PC serial COM ports baud rate. Therefore, we will explore option 2. There is a software way to double the baud rate of the 8051 while the crystal frequency is fixed. This is done with the register called PCON (power control). The PCON register is an 8-bit register. Of the 8 bits, some are unused, and some are used for the power control capability of the 8051. The bit which is used for the serial communication is D7, the SMOD (serial mode) bit. When the 8051 is powered up, D7 (SMOD bit) of the PCON register is zero. We can set it to high by soft- $D_7 = 0$, Normal baud-rate. $D_7 = 1$, baud-rate in Serial communication is doubled.	4 + 3	7	

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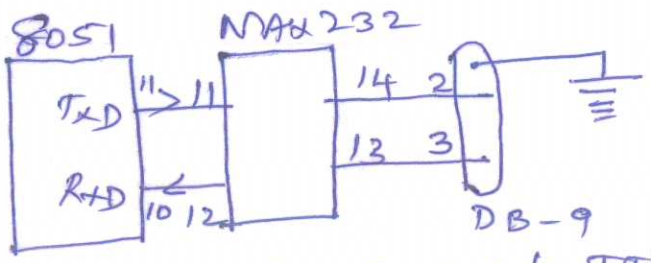
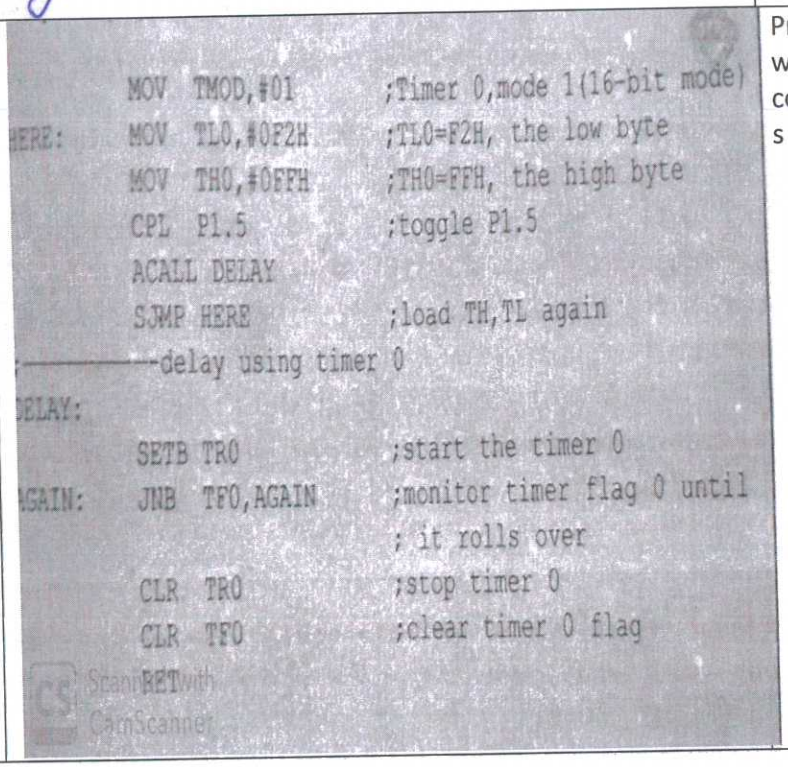
Qust.No.	Scoring Indicator	Split up score	Sub Total	Total
VIII (a)	PART C Serial Communication is possible with minimum 3 wires – Transmit Data, Receive data and Ground.  MAX 232 will convert TTL logic to RS-232 standard logic.	8	7	

VIII (b)	
	MOV TMOD,#01 ;Timer 0,mode 1(16-bit mode)
	HERE: MOV TL0,#0F2H ;TL0=F2H, the low byte
	MOV TH0,#0FFH ;TH0=FFH, the high byte
	CPL P1.5 ;toggle P1.5
	ACALL DELAY
	SJMP HERE ;load TH,TL again
	;-----delay using timer 0
	DELAY:
	SETB TR0 ;start the timer 0
	AGAIN: JNB TF0,AGAIN ;monitor timer flag 0 until
	; it rolls over
	CLR TR0 ;stop timer 0
	CLR TF0 ;clear timer 0 flag
	RET
	
		Program with comments 7 marks	7	

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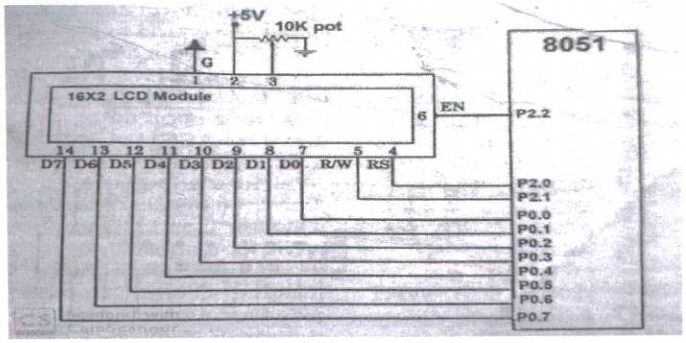
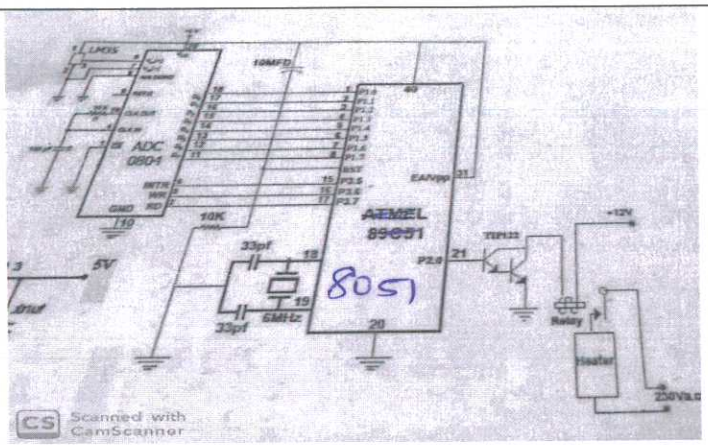
IX (a)	PART C  LCD module is connected to Port 2 of 8051. It has to be declared as o/p port.	Fig 4+ details 3	7	
IX (b)	 Thermistor (LM35) sensor o/p is connected to ADC for conversion. When actual temp. falls below set value, Relay will be on, heater will be switched on.	Fig 5 + Expln. 3	8	

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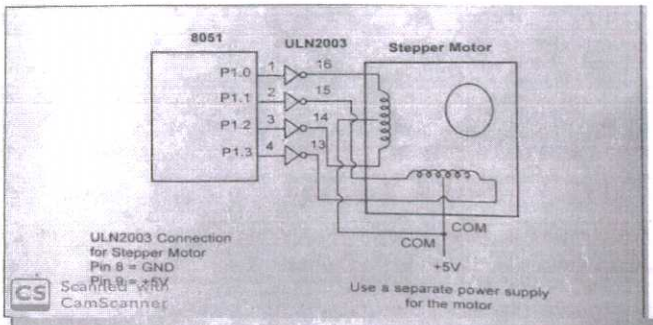
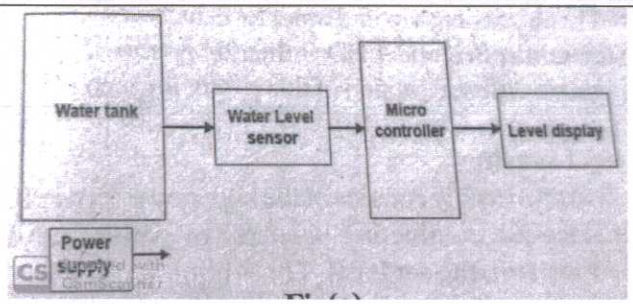
X (a)	PART C 	Fig 4+ program 4	8	
X (b)		Fig 4 + Expln. 3	7	

```
                MOV  A,#66H     ;load step sequence
BACK:           MOV  P1,A       ;issue sequence to motor
                RR   A          ;rotate right clockwise
                ACALL DELAY     ;wait
                SJMP BACK       ;keep going

                ...
DELAY
                MOV  R2,#100
H1:             MOV  R3,#255
H2:             DJNZ R3,H2
                DJNZ R2,H1
                RET
```