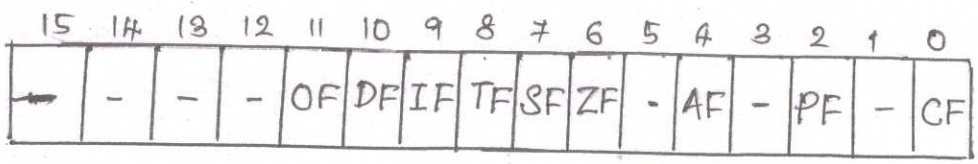
SCHEME OF EVALUATION
(Scoring Indicators)

Que. No.	Revision : 2015 Course Title: MICROPROCESSORS AND INTERFACING Course Code: 5131		
I	Part-A		
1.	* 16-bit Processor * 16-bit data bus * 20-bit address bus * 1MB memory capacity * Available in various clock speeds: 5MHz, 8MHz, 10MHz etc. * 40-pin DIP IC	Any two - 2 marks	2
2.	Code Segment Register (CS), Data Segment Register (DS), Extra Segment Register (ES), Stack Segment Register (SS)	2	2

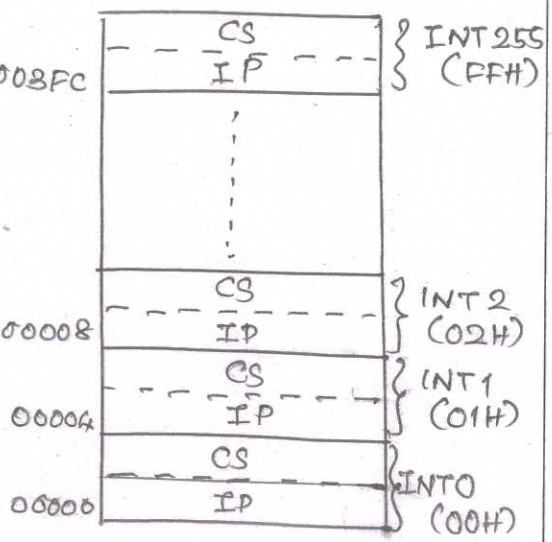
3.	ADD dest, source
	ADC dest, Source
	INC dest.
	MUL Source
	IMUL Source
	SUB dest, source
	SBB dest, source
	DEC dest.
	DIV Source
	IDIV Source
	CBW
	CWD
	NEG dest.
	DAA
	DAS
	AAA
	AAS
	AAM
	AAD
	CMP dest, Source
		Any 4 - 2 marks	2

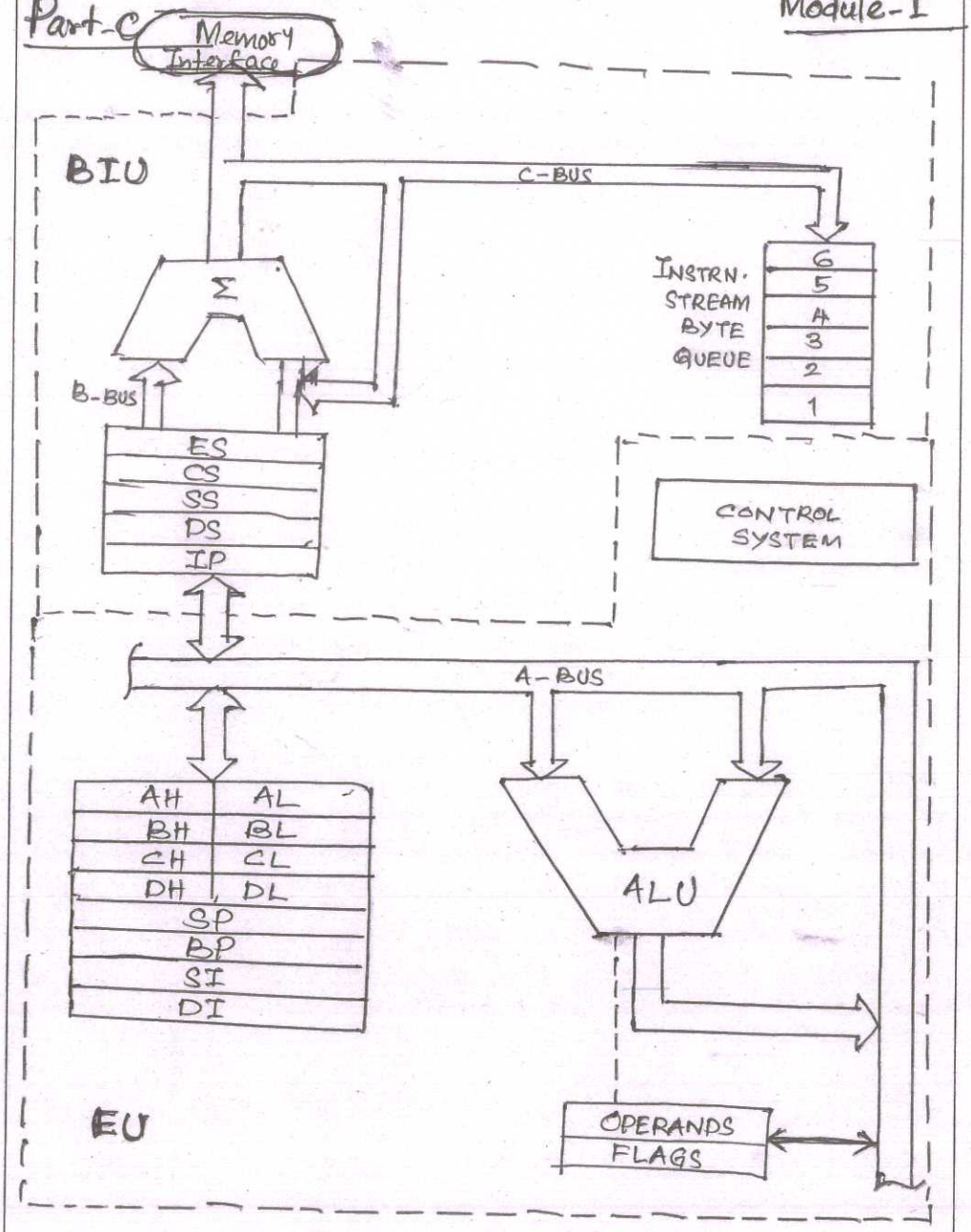
4.	When an interrupt occurs, the microprocessor suspends the current program, and executes another program for the requested task. This program is called Interrupt Service Routine (ISR).	2	2
5.	Real Addressing mode and Protected Virtual Addressing mode (PVAM)	2	2

II	**Part-B**  		
1.	**Control Flags:** IF : Interrupt Enable Flag DF : Direction Flag TF : Trap Flag **Conditional Flags:** CF : Carry Flag PF : Parity Flag AF : Auxilliary Carry Flag ZF : Zero Flag SF : Sign Flag OF : Overflow Flag.		6

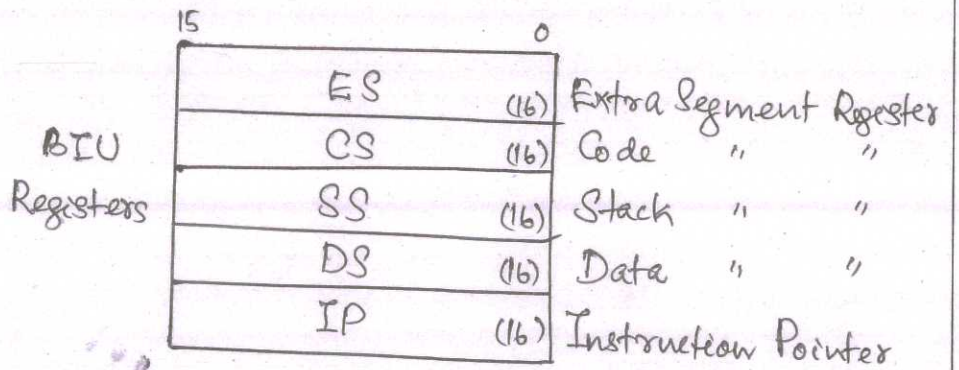
2.	(i) Register addressing → eg: MOV AL, BL
	(ii) Immediate addressing → eg: MOV AL, 05H
	MOV CX, 5A82H
	(iii) Direct addressing → eg: MOV AL, [8040H]
	(iv) Register Indirect
	MOV [2050H], AX
	addressing → eg: MOV AL, [BX]
	MOV CX, [SI]
	(v) Based addressing → eg: MOV AL, [BX+08H]
	(vi) String addressing
	MOV [BP+5012H], CX
	→ eg: MOVS BYTE
	(vii) Relative addressing ↔ eg: JMP Next
	JZ AGAIN
	(viii) Implicit addressing → CLC, STD
		Any 3
		x
		2 marks
			6

3.	JA/JNBE JAE/JC/JNAE JBE/JNA JE/JZ JG/JNLE JCXZ JGE/JNL JO JNO JS JP JNP/JPO JP/JPE etc.	Any 3 x 2marks	6

4.	The address of ISR is called Interrupt Vector. It is in the form of CS:IP. Vector for any ISR has 4 bytes: 2 for CS and 2 for IP. 8086 has 256 interrupts. So 256×4 = 1024 bytes (1K) of memory are allocated to store the interrupt vectors. These 256 vectors are stored in a table called Interrupt Vector Table (IVT). In systems RAM, the memory locations with addresses 00000H to 003FCH is used for Interrupt Vector Table. 	Explm. 4 + Fig 2.	6
5.	(i) Mode_0 (Simple Input/Output) (ii) Mode-1 (Input/Output with Handshake) (iii) Mode-2 (Bi-directional I/O data Transfer) (iv) BSR mode (Bit Set/Reset mode)	Any 4 × 1½ marks	6
6.	* 32-bit microprocessor * 32-bit data bus * 32-bit address bus. * 4GB of Physical memory & 64TB of virtual memory * 32-bit general purpose registers. * Available as 132-pin PGA package. * Three memory addressing modes — Real Addressing Mode, Protected Virtual Addressing mode (PVAM) & Virtual 86 mode. * Available in 2 different versions: SX and DX	Any 4 × 1½ marks	6

7.	A multi-core processor is a single computing component with two or more independent actual central processing units called 'cores'. These units read and execute the programs. Multiple cores can run multiple instructions at the same time, increasing overall speed for programs. Manufacturers typically integrate the cores onto a single integrated circuit die known as 'chip multiprocessor (CMP), or onto multiple dies in a single chip package.	Defn. 3 + Expln. 3.	6
	Part-C Module-I		
III	 BIU - Bus Interface Unit EU - Execution Unit	Fig-10 + Expln. 5	15

IV a)



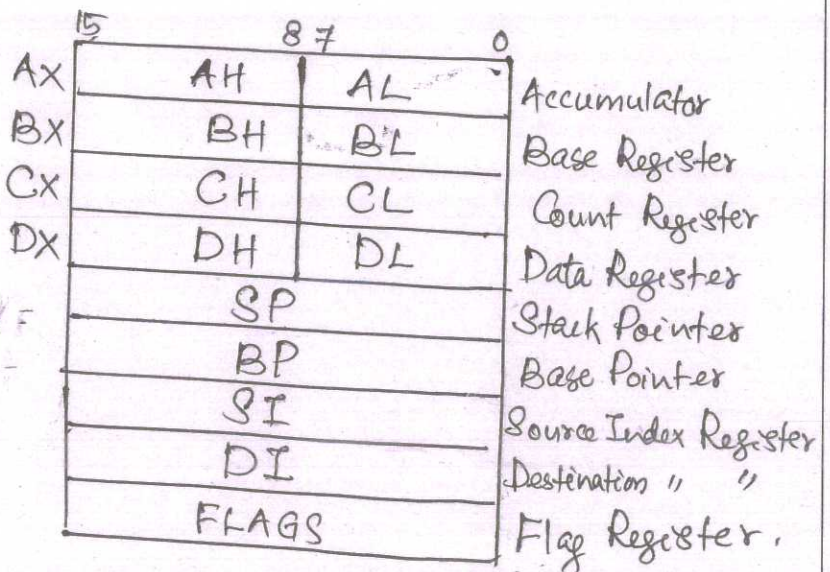


Fig 5 + Expln. 3

8

IV b)

* Allows memory capacity to be 1MB even though the addresses associated with the individual instructions are only 16 bits wide.
* Facilitates the use of separate memory areas for the program (code), its data and stack.
* Multitasking becomes easy.
* Permits a program and its data to be put into different areas of memory each time the program is executed

7

15

V a) Module-II

Data Transfer Instructions:

(i) MOV Dest, Source → Eg: MOV AL, BL
MOV CX, DX
MOV AH, [8050H]

(ii) PUSH Source → Eg: PUSH CX
PUSH [BX]

(iii) POP Dest. → Eg: POP DX
POP [SI]

(iv) IN acc, port → Eg: IN AL, 05H
IN AX, 08H

(v) OUT Port, acc → Eg: OUT [DX], AL
OUT 07H, AX

(vi) LEA Reg, Mem.

(vii) LDS Reg, Mem.

(viii) LEA Reg, Source.

(ix) LAHF

(x) SAHF

(xi) XCHG dest, source

(xii) XLAT

Any 4 x 2 marks = 8

V b)

```
DATA SEGMENT
    NUM1 DW 1284H
    NUM2 DW 5327H
    SUM DW ?
    CARRY D ?
DATA ENDS
ASSUME CS:CODE, DS:DATA
CODE SEGMENT
START: MOV AX, DATA
       MOV DS, AX
       MOV AX, NUM1
       MOV BX, NUM2
       MOV CL, CARRY
       ADD AX, BX
       JNC SKIP
       INC CL
SKIP:  MOV SUM, AX
       MOV CARRY, CL
       MOV AH, 4CH
       INT 21H
CODE ENDS
END START
```

7 marks

15

VI a)

```
DATA SEGMENT
    PBCD DB 45H
    BCD1 DB ?
    BCD2 DB ?
DATA ENDS
ASSUME CS:CODE, DS:DATA
CODE SEGMENT
    START: MOV AX, DATA
           MOV DS, AX
           MOV AL, PBCD
           MOV CL, 04H
           AND AL, 0F0H
           SHR AL, CL
           MOV BCD1, AL
           MOV AL, PBCD
           AND AL, 0FH
           MOV BCD2, AL
           MOV AH, 4CH
           INT 21H
CODE ENDS
END START
```

7 Marks

VI b)

Procedure	Macro
* It is a set of instructions in a given program that acts as a sub-program or sub-routine.	* Name given to a sequence of instruction lines in a program.
* Executes when it is called by the name. (CALL instruction)	* Executes the instructions in macro, when called by name.
* Machine codes for the set of instructions needs to be loaded into main memory only once.	* Needs to load the machine codes, each and every time when the macro is called.
* Uses less memory space.	* More memory space is needed.
* Uses CALL and RET instructions	* No need of CALL and RET instructions
* Involves the usage of stack	* No need of stack.

Module-III

VII a) Intel has dedicated certain interrupts for specific applications directly related to CPU operations. These are called pre-defined interrupts. Listing-5 + Explns. 3 = 8 Marks

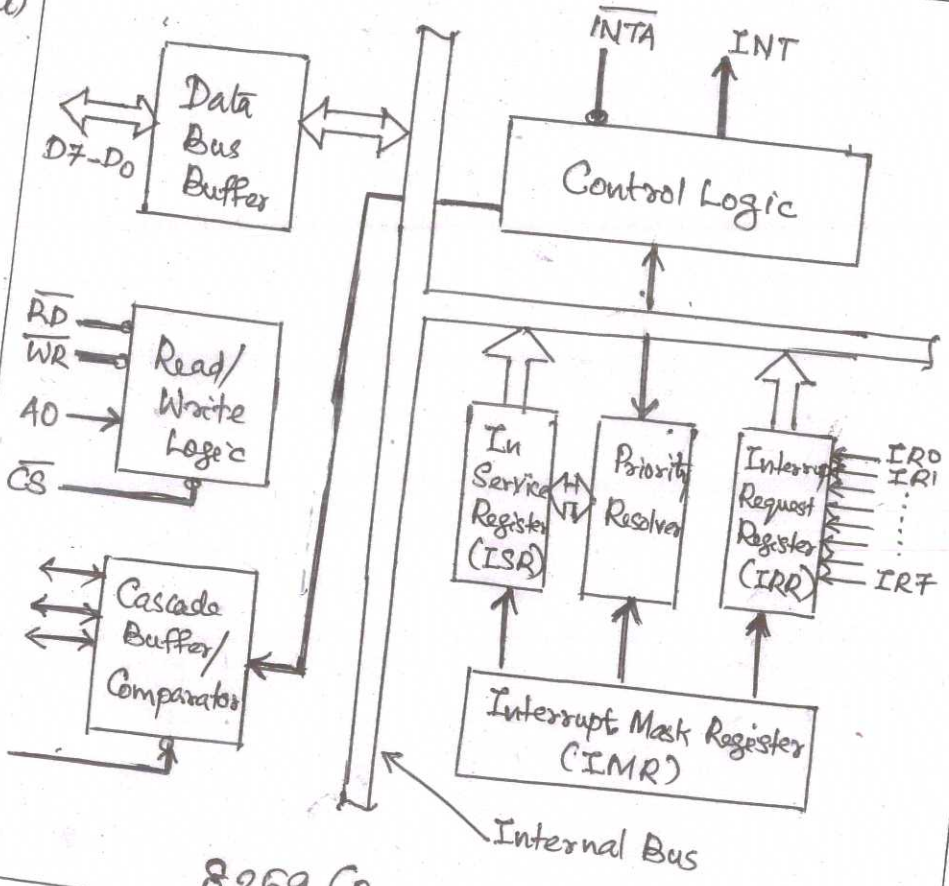
* Int 0 (Divide by Zero error)
* Int 1 (Single Stepping)
* Int 2 (Non Maskable Interrupt)
* Int 3 (Breakpoint Interrupt)
* Int 4 (Overflow Interrupt).

VII b) When two or more interrupts occur simultaneously, they are handled one by one on priority basis. The highest priority interrupt is serviced first and then one of the next higher priority and soon. The interrupt priorities of 8086 are given as below. 7 marks

Interrupts	Priority
Divide Error, Int n, INTO	Heghest
NMI	↓
INTR	↓
Single Step	Lowest.

15

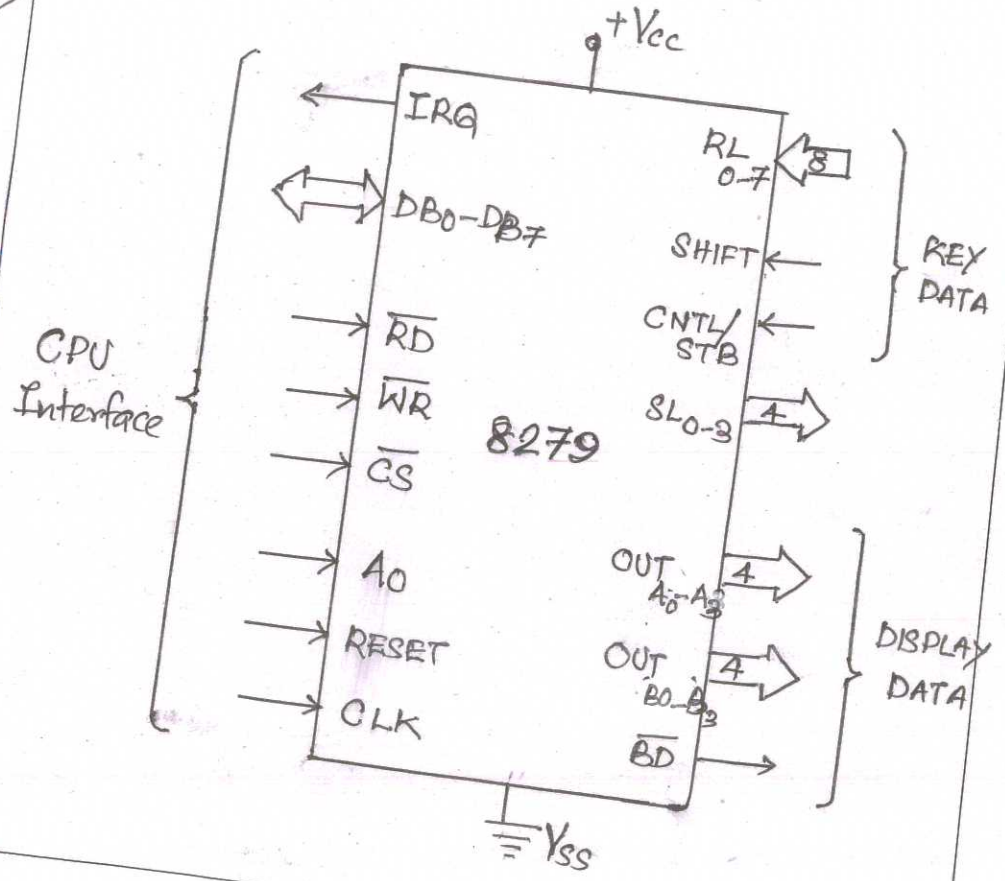
VIII a)



8259 (Programmable Interrupt Controller)

Fig 5 + Explⁿ. 3 = 8 marks

VIII b) 8279 - Pins & Signals



15

7 Marks

IX

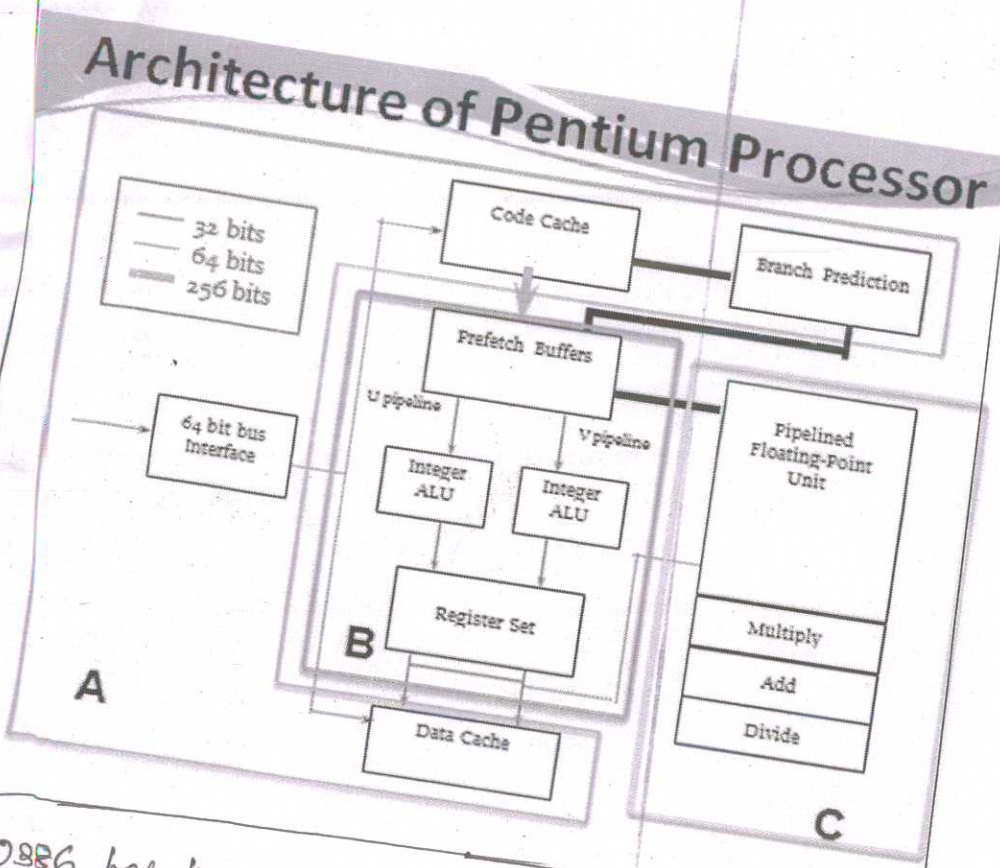


Fig 5 + Expln. 3 = 8 marks

IX b) 80386 has two memory addressing modes namely Real Addressing Mode & Protected Virtual Addressing Mode (PVAM).

80386 can be switched from Real address mode to PVAM by setting the PE (Protection Enable) bit in the Control Register 0 (CR0). In this mode, the processor can address 4GB of physical memory address space and 64 TB of virtual memory space.

In PVAM, each memory location is represented by a 48-bit virtual address. The 80386 converts this virtual address into a physical address differently depending upon whether the paging unit is enabled or disabled.

7 marks

15

X a) A superscalar machine executes multiple independent instructions in parallel, and thus enhances the processing speed.

Pentium processor is organized with two integer pipelines namely U-pipe and V-pipe with individual ALU for each pipe. While executing the current instruction, the processor checks the next two instructions.

If the execution of one instruction does not depend on the other, then the first instruction is issued to U-pipe and the second one to V-pipe, so that two instructions can be executed simultaneously.

This feature of Pentium to execute two instructions in parallel is called Superscalar architecture

8 marks

X b) MMX means MultiMedia Extension Technology.

- It is decined to accelerate multimedia and communication applications
- Exploits the parallelism inherent in many multimedia and communications algorithms.
- Single Instruction Multiple Data technique.
- Eight 64-bit wide MMX technology registers.
- Uses a number of new instructions.
- Four new data types.