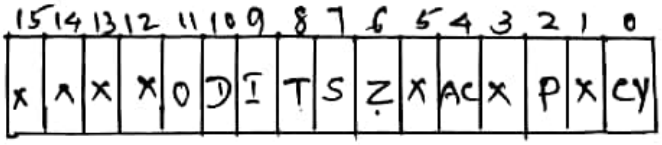
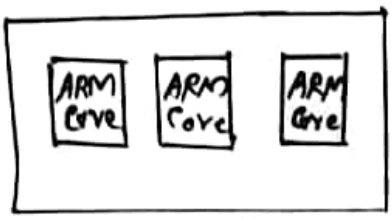
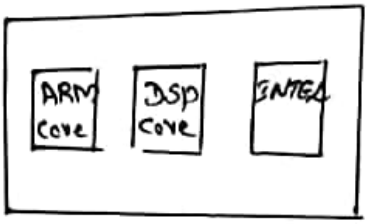
Scoring Indicators

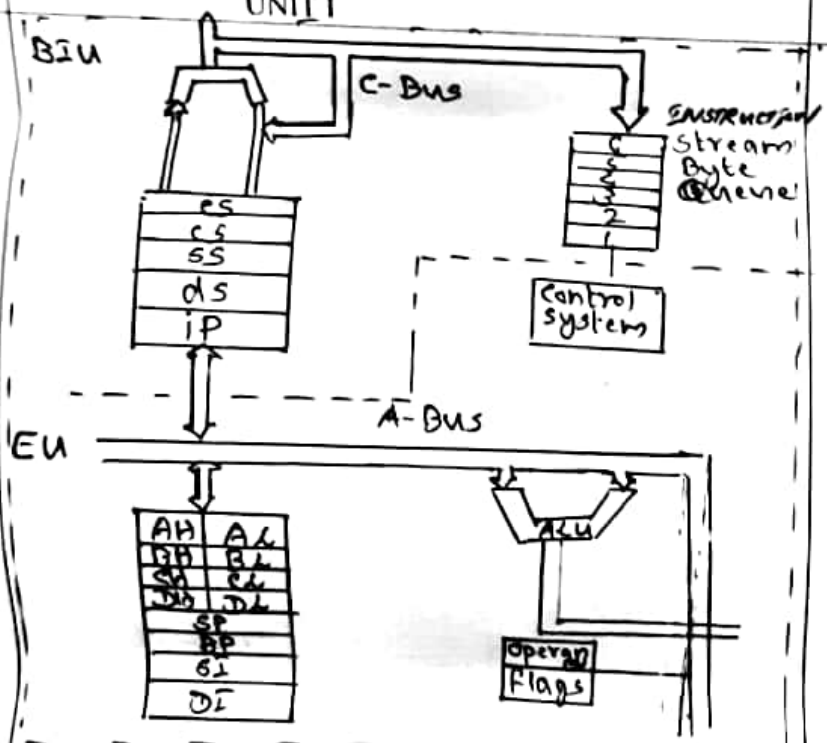
Course : ADVANCED MICROPROCESSORS **Code :** TED (15) 6041

Revision : 2015

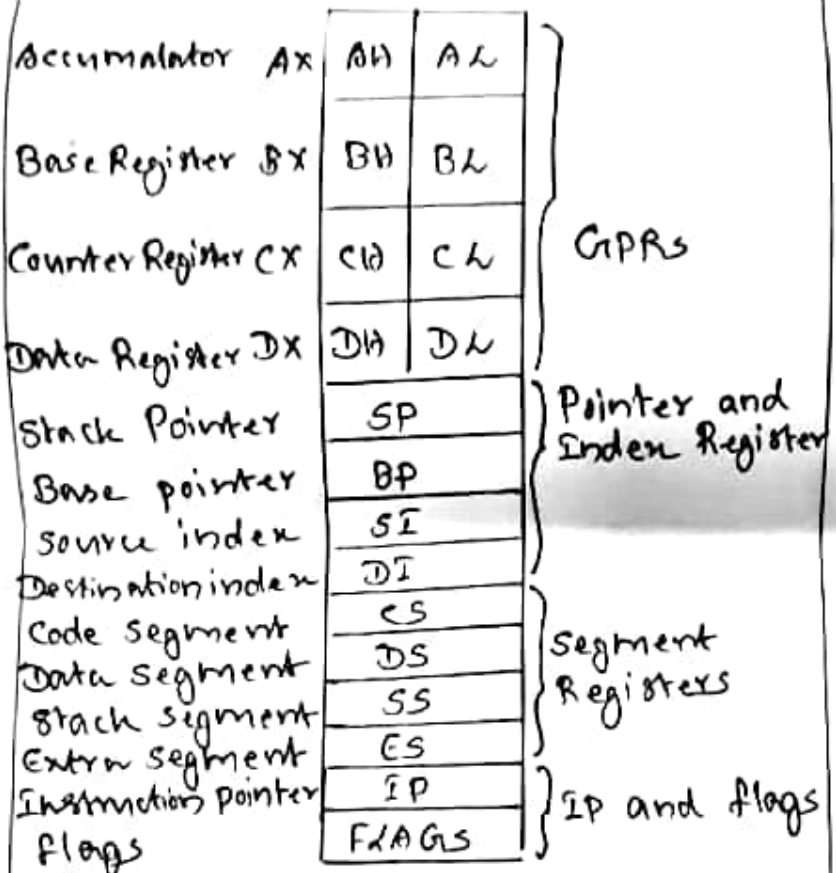
Version : A

Question No.		Scoring Indicators	Split Score
		PART A	
I.	1.	Address Latch Enable. For Demultiplexing Address bus and Data bus.	2
I.	2	Carry Flag is set if there is a carry after performing an arithmetic operation. Otherwise it is zero.ie, Reset	2
I.	3	Assembler converts Assembly Level Language into Machine Language.	2
I.	4	Core is an individual processor within a CPU.	2
I.	5	Protected Virtual Address Mode. By setting PE bit in the control register CRo	2
		PART B	
II.	1	 O- Overflow flag; set if overflow occurs D- Direction fag; used for string manipulation instructions. I- Interrupt flag; for enabling external maskable interrupt. T- Trap flag; for single step execution mode. S-Sign flag; Result of an arithmetic operation is positive then zero. Z- Zero flag; set if result is zero AC- Auxiliary Carry flag; set if there is a carry in BCD operation. P- Parity flag; set if lower byte of result contains even number of 1s. CY- carry flag; set if there is a carry out of the MSB in addition	6

II.	2	Homogeneous multicore processors include only identical cores.  Heterogeneous multicore processors have cores that are not identical.  	3+3
II.	3	Real Address Mode: when 80386 is resetted it enters into this mode.similar to 8086 but allows access to 32 bit registers,operand size is16 bits,paging is disabled,can access 1MB of physical memory. Virtual 8086 Mode: it performs all 8086 applications with all protected features of 80386.segment registers are used similar to real mode.20 bit physical address is obtained by shifting left 4 times the segment register and adding to offset.can access 1 MB physical memory. Paging is enabled.	3+3
II.	4	Superscalar Architecture Branch prediction Pipelined Floating point Unit 64 bit data bus Virtual mode extension Separate 8KB code and 8KB DataCache	6 (Any four)
II.	5	i3 CPUs have only two core. i3 operates at lower frequencies. i3 does not have Turbo Boost. Core i3 has smaller L3 cache i3 supports hyperthreading. i3 is used in entry level application field.	6 (Any four)

II.	6.	Data Transfer Instructions: MOV,XCHG,PUSH,POP,IN,OUT Arithmetic Instructions: ADD,ADC,SUB,SBB,INC,DEC,MUL,DIV,CMP	3+3 (Any 3 from each)
II.	7.	Instructions: assembly language consists of instructions. They are translated into machine codes.instructions produce executable codes. Directives: They are pseudo-instructions. They do not produce executable code.They direct the assembler to perform in certain ways.	3+3
		PART C	
		UNIT I	
III.	a.	 BIU: Bus Interface Unit; fetches instructions,reads data from memory or I/O ports and buffers in queue. EU: Execution unit; works parallel with BIU, fetch instruction from queue, decode and execute.It has 16 bit ALU for	Fig 6 Expl 4

		performing the arithmetic (addition, subtraction etc) and logical (OR,NOT etc)operations.	
III.	b	Arithmetic Left shift the given 16 bit address and add the offset to get the 20 bit physical address. eg:- Base Address = 2222 H offset = 0016 H Physical Address = 22220 H 0016 22236H	5
IV.	a.	1)General Purpose Registers: four 16 bit registers Accumalator AX- AH,AL Base Register BX- BH,BL Counter Register CX- CH,CL Data Register DX- DH,DL 2)Pointer and Index Registers SP- Stack Pointer BP- Base Pointer SI- Source Index DI- Destination Index 3) Segment Registers CS- Code segment; store instructions DS- Data segment; store program data, constants, variables SS- Stack Segment, for stack in a program ES: Extra Segment; store data strings for special instructions	fig 3 Expl 6

		4) Instruction Pointer and Flags IP: points to next instruction in the current code segment Flags: Checking various conditions  	
IV.	b.	HOLD: Used fir Direct Memory access.ie, when HOLD=1 indicates another master requesting bus access. HLDA: Hold Acknowledge, After receiving HOLD request processor issues HLDA signal. *READY*: Acknowledgement signal sent by peripheral when it is ready to transfer data.ie For communicating with slower peripherals.	6 (2 marks each)
		UNIT II	

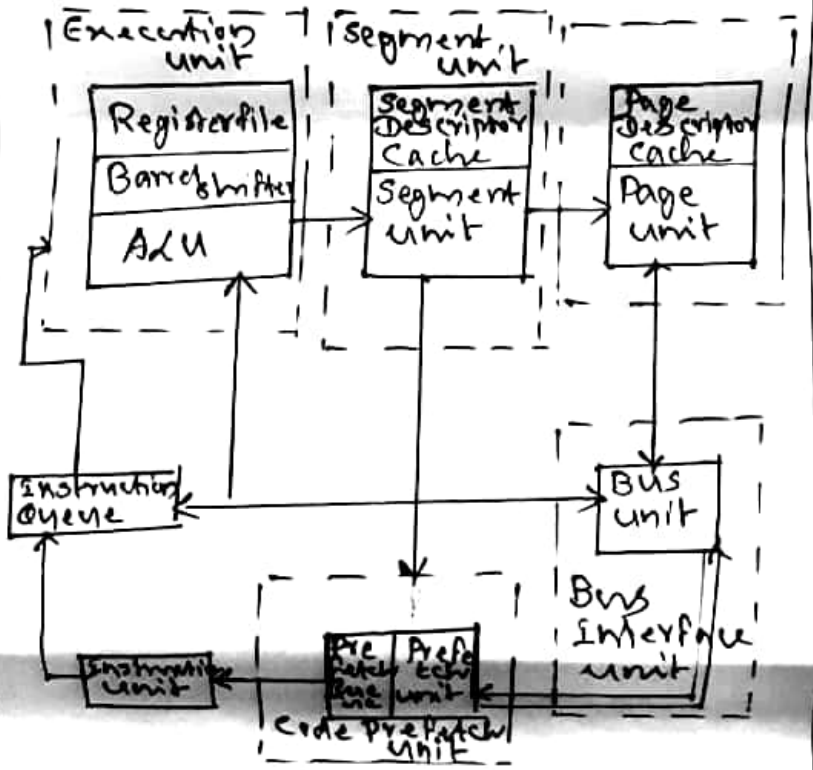
V.	a.	1) Type zero interrupt (Divide by Zero interrupt): When the quotient of division operation is too large to fit in the destination register.Eg: division by zero 2)Type 1 Interrupt(single step Interrupt): For debugging Assembly Language Program. Processor executes one instruction,then stops, contents of memory locations,registers are examined to see the result. 3)Type 2 Interrupt: NMI, Non Maskable Interrupt, used in emergency conditions.when power fails,used to save program and data. 4)Type 3 Interrupt (Break Point Interrupt): Break point is inserted in program for debugging.Upto the break point program is executed ISS stores content of registers on stack ,contents of registers displayed on CRT. 5)Type 4 Interrupt(Overflow Interrupt):If the signed result of two signed numbers is too large to fit in memory location overflow error occurs.INTO instruction is used immediately after arithmetic instruction.	10 (2 marks each)

V	b.	MOV AL,08H
		MOV BL,05H
		ADD AL,BL
		HLT
		Inputs : AL ← 08H
		BL ← 05H
		output : AL ← 0DH
			5

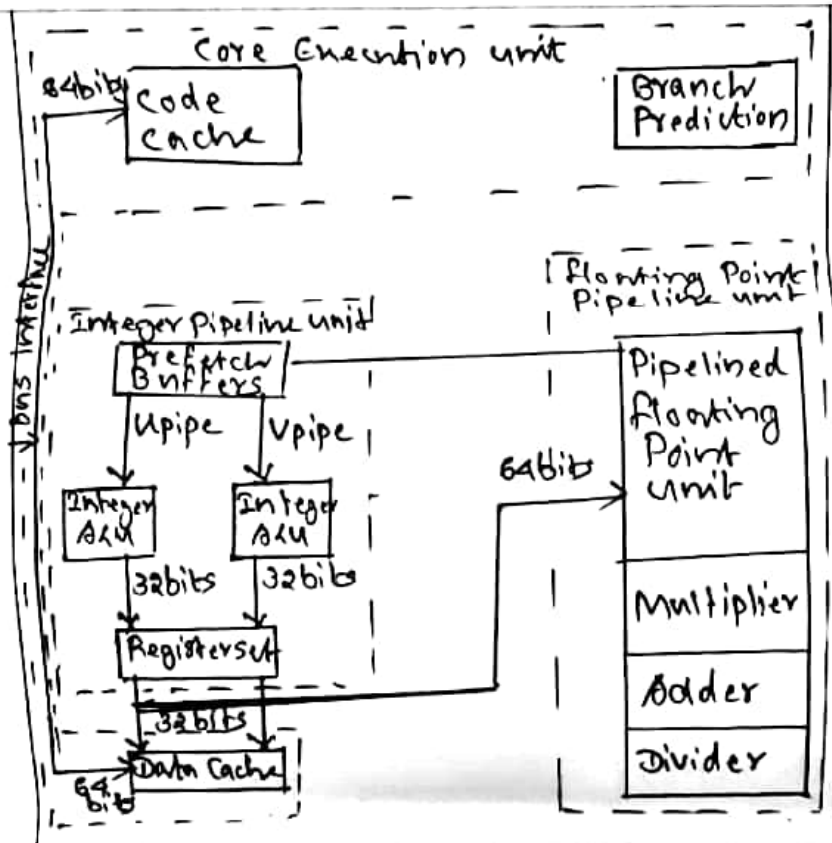
VI.	a.	1) Immediate Addressing Mode Eg: MOV AX, 0016H 2) Register Addressing Mode Eg: MOV AX, CX 3) Direct Addresssing Mode: Eg:MOV AX, [4000 H] 4)Register Indirect Addressing Mode Eg: MOV AX, [BX] 5)Based Addressing with Displacement Eg:MOV AX, 1234 H [BX] Effective address of source is obtained by adding the contents of BX and 16 bit Displacement 6)Indexed Addressing with displacement Eg: MOV AX, 1234 H [SI]	10 (2 marks each. any 5)

		Effective address is obtained by adding the content of index register and displacement. 7) I/O port addressing Port address is specified with fixed port address.	

VI	b.	MOV AL,08H
		MOV BL,05H
		MUL BL
		HLT
		Inputs AL ← 08H
		BL ← 05H
		output AX ← 0028H
			5

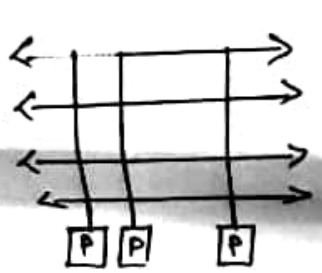
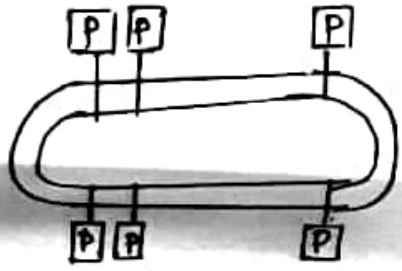
		UNIT III	
VII.	a.	 1)Bus Interface Unit:It interfaces with the memory and I/O. 80386 generates address, data and control signals. 2) Code Prefetch Unit: Fetches instruction from memory. Paging unit converts address generated by prefetch unit to physical address. 3)Instruction Decode unit: Translates instructions fro code	Fig 5 Expl 5

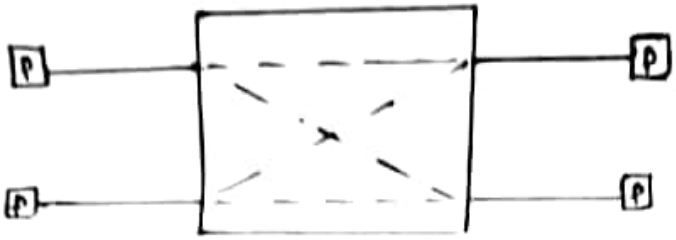
		prefetch unit into microcodes and stored in instruction queue. (FIFO) 4)Segmentation Unit:Produces a translated linear address which paging unit translates into physical address. 5)Paging Unit:Checks for paging violations before it sends a bus request. 6)Execution unit: operates on decoded instruction, performs steps needed to execute it. Control unit contains the microcodes and parallel hardware for multiply,divide and effective address calculation.	
VII.	b.	32 bit processor. 32 bit data bus and 32 bit internal registers 32 bit non multiplexed address bus. Break point registers. Contains 129 basic instructions. Provides multitasking support. Pipelined architecture.	5
VIII.	a.	1)Core Execution Unit: It contains code cache, data cache, branch prediction, separate 8 KB code cache, 8KB data cache. 2)Integer Pipe line unit: it has 5 stages. i)Prefetch: CPU fetches instructions from instruction cache and stores. ii)Instruction Decode: CPU decodes the instruction and generates a control word. iii)Address generation: CPU generates address for data memory references. iv) Execution: CPU either accesses the data cache for data operands or computes the result in ALU. v)Write Back: Depending on the execution result CPU updates the register's contents or status in the flag register. 3) Floating Point Pipeline unit: It consists of 8 stages, prefetch, instruction decode, address generation, operand fetch, first execute, second execute, write float and error reporting stages. 4) 64 bit bus interface: It is used to interface external I/O devices.	Fig 5 Expl 5



VIII.	b.	Superpipelining. Integrated Level 2 Cache. 32 bit optimization. Wider address bus Greater multiprocessing Out of order completion Superior branch Prediction Register renaming Speculative execution	5 (any five)

UNIT IV

IX	a.	Core i5: it has 4 cores, operate at higher frequency, it has Turbo Boost, Larger L3 cache, does not support hyperthreading, its application field is mainstream. Core i7: it has 4 cores, operate at higher frequency, it has Turbo Boost, Larger L3 cache, support hyperthreading, its application field is high end.	10 (5 marks for each)
IX	b.	HTTP: Hyper Threading Technology, developed by intel Corporation, enables processor to execute two threads or sets of instructions at the same time, like two separate processsors together. Can improve processing performance both in uniprocessor machine or for multiprocessor application. Threads can make GUI more responsive. It facilitatesthe overlap of I/O and computation.	5
X.	a.	1) Interconnects: With multiple cores and shared resources such as memory,buses,and I/O, the interconnection between cores is the big problem. Interconnection reduce latency, congestion and allow higher bandwidths. Early multicore processor used bus based interconnection, recently uses ring, mesh, cross bar topologies.  Bus Interconnect.  Ring Interconnect.	9 (3 marks each)



Cross Bar interconnect.

2)Caches and Cache Coherence: All multicore processors have a Level 1 cache as private resource for each core.some have Level 2 cache , Level 3 cache is shared. Due to distributed private cache, cache coherence is a problem. Once an intention of writing in a private cache is observed, the other caches either invalidate or update their private copies of this location.Thus coherence between the private caches of each core is ensured.

3) Programming Aspects: For using multocore processor in full potential application need to be written so that different parts of the program can be run concurrently on separate cores. Thus a multithreaded program is needed such that different cores can run different threads simultaneously.

X.	b.	1)Virtualization: allows system to work with more than one operating system. 2)Turbo Boost: It allows the processor core to run automatically and opportunistically at a higher clock frequency. 3)Hyperthreading: Enables the processor to execute two threads or sets of instructions at the same time. 4)Advanced vector extensions: It uses 256 bit vector data to perform operations of integer,floating pointetc	6 (Any three 2 marks each)