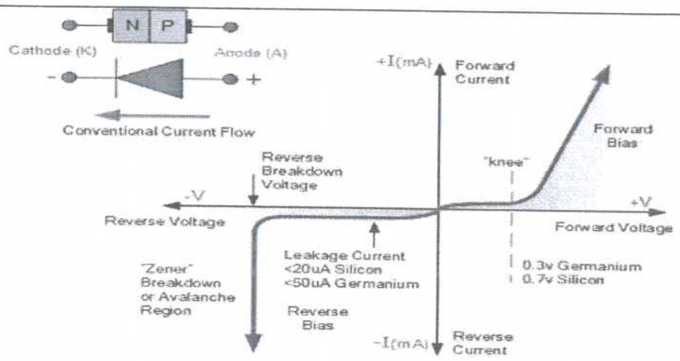
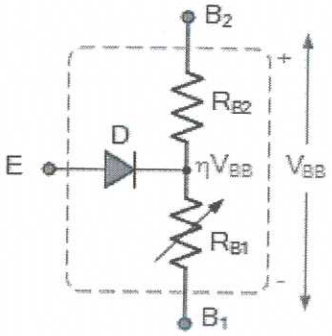
SET 1

Scoring Indicators

COURSE NAME: Basic Electronics

COURSE CODE: 2041

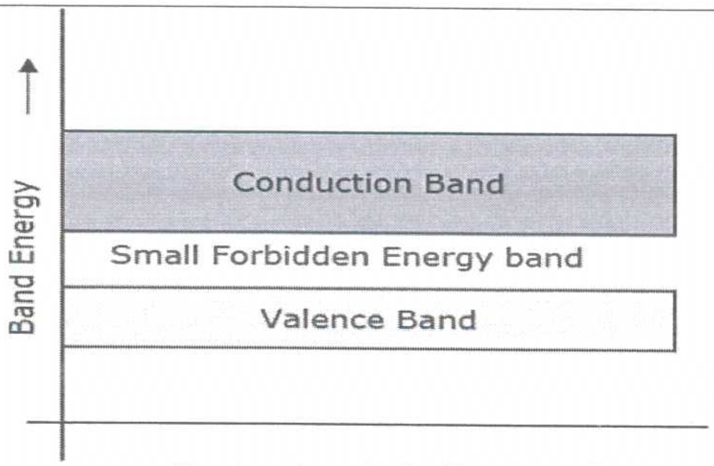
QID: 2106220059

Q. No.	Scoring Indicators	Split Score	Sub Total	Total Score
	PART A			**9**
I. 1	The process of adding impurities to a pure semiconductor in a controlled manner.	1	1	1
I. 2		1	1	1
I. 3	Active, Saturation, Cut-off, Inverted	0.5*2 = 1 (Any two)	1	1
I. 4	$\alpha = \frac{\beta}{1+\beta}$ or $\beta = \frac{\alpha}{1-\alpha}$	1	1	1
I. 5	NPN transistor	1	1	1
I. 6		1	1	1
I. 7	The ratio of the standoff voltage to the power supply voltage. Or The ratio of the R_{B1} (base resistance 1) and the interbase	1	1	1

	resistance (R_{BB}).			
I. 8	Clipping, Clamping	0.5*2 = 1	1	1
I. 9	Triangular wave	1	1	1
PART B				**24**
II. 01	1. Forward voltage drop, V_f • The voltage drop across the diode when it is in forward bias. • For silicon diodes $V_f = 0.7$ V and germanium diodes $V_f = 0.3$ V 2. Peak Inverse Voltage(PIV) • The maximum voltage that a p-n junction can withstand in reverse-biased condition. 3. Maximum Forward Current • The Maximum value of the forward current that a PN junction or diode can carry without damaging the device. 4. Reverse saturation current • Under reverse biased condition, the depletion width of diode increases and hence no diffusion current flows.But due to the flow of thermally generated charge carriers a small current flows through the diode called as reverse saturation current,I_{CO}. • I_{CO} increases with increase in temeperature. • Even when diode is open circuited, current exists in circuit because of I_{CO}. Hence it is also called as Leakage current. • For Si diode I_{CO} is in range of few nA and for Ge it is in range of few μA. 5. Power rating	3*1 = 3	3	3

	The maximum power that a PN junction or diode can dissipate without damaging the device itself. **(Any three)**			
II. 02	Drift Current • The current flow in the semiconductor, when the charge carriers in it moves under the influence of applied electric field is called as Drift current. • Once the voltage is applied to a semiconductor, then electrons move toward the positive terminal of a battery whereas the holes travel toward the negative terminal of a battery. • The direction of the drift current, as well as the applied electric field, will be the same. • Thermally generated minority carriers will give the drift current in PN junction.	1.5	3	3
	Diffusion current • The current flow in the semiconductor, when the charge carriers in it moves from a higher concentration region to a lower concentration region is called as Diffusion current. • The process of diffusion mainly occurs when a semiconductor is doped non-uniformly • The direction of diffusion current mainly depends on the charge within the concentrations of carrier • Majority carriers will give the diffusion current in PN junction.	1.5		
		1		
II. 03	The CE configuration provides both high current and voltage gain. The CC configuration has high current gain but voltage gain less than unity. The CB configuration has high voltage gain but current gain less than unity.	3		

	Power gain = Voltage gain*Current gain Thus CE configuration is best for amplification because of its high power gain (due to its both high voltage and current gain) and hence most widely used.		3	3
II. 04	1. Proper zero signal collector current: When no input signal is given; a DC current should flow in the collector terminal. The value of zero signal collector current should be at least equal to the maximum collector current due to the signal alone. 2. Minimum proper base-emitter voltage (V_{BE}) at any instant: The minimum base to emitter voltage V_{BE} should be greater than the cut-in voltage for the junction to be forward biased.For Si transistor it is 0.7V and for Ge transistor it is 0.3V 3. Minimum proper collector-emitter voltage (V_{CE}) at any instant: The collector emitter voltage V_{CE} should not fall below the cut-in voltage,(Knee Voltage). If V_{CE} is lesser than the knee voltage, the collector base junction will not be properly reverse biased. Then the collector cannot attract the electrons which are emitted by the emitter and they will flow towards base which increases the base current. Thus the value of β falls	3*1 = 3	3	3
II. 05	a) Drain to Source Voltage(V_{DS}) and Gate to Source Voltage(V_{GS}) b) When no voltage is applied to the device i.e. V_{DS} = 0 and V_{GS} = 0, the device will be idle and no current flows through it (I_{DS} = 0).	2 1	3	

II. 06	 Energy bands in Semiconductors	3	3	3
II. 07	Static forward resistance: The ratio of DC voltage applied across the diode to the DC current flowing through the diode. $R_f = \frac{VD}{ID}$ Dynamic forward resistance: The ratio of AC voltage applied across the diode to the AC current flowing through the diode. $r_f = \frac{\Delta VD}{\Delta ID}$	2*1.5 = 3	3	3
II. 08	TUF = 0.2865; ripple factor = 1.21; DC output voltage = $\frac{10}{\Pi}$	3*1 = 3	3	3
II. 09	The main source of the leakage current in a transistor is thermally generated minority carrier. When temperature increases minority carriers increases. When reverse bias is applied, thermally generated carriers began to flow resulting in leakage current. For every 10°C rise in temperature, leakage current doubles.	3	3	3

	Sl. No.	Emitter Junction	Collector Junction	Modes of Operation			
II. 10	1.	Forward biased	Reverse biased	Active	3*1 = 3	3	3
	2.	Forward biased	Forward biased	Saturation			
	3.	Reverse biased	Reverse biased	Cut-off			
	4.	Reverse biased	Forward biased	Inverted			

PART C	42

	Sl. No.	**P-type**	**N-type**			
III. 01	1.	Formed by adding trivalent impurity to pure semiconductor.	Formed by adding pentavalent impurity to pure semiconductor.	(3*2) +1 = 7 (Any four)	7	7
	2.	Impurity added creates vacancy of electrons (holes) called as Acceptor Atom.	Impurity added provides extra electrons and is known as Donor Atom.			
	3.	Holes are majority carriers.	Electrons are majority carriers.			
	4.	Electrons are minority carriers.	Holes are minority carriers.			
	5.	The acceptor energy level is close to the valence band and away from the conduction band.	The donor energy level is close to the conduction band and away from the valence band.			
	6.	Fermi level lies between acceptor energy level and the valence band.	Fermi level lies between donor energy level and the conduction band.			

III. 02	There are three biasing conditions for p-n junction diode based on the voltage applied:	1		

<table>
<tr>
<td></td>
<td>1. Zero bias
2. Forward bias
3. Reverse bias
1. <u>Zero bias:</u> Under no-biased condition(Zero bias), no external voltage is applied to the p-n junction diode. Hence no diffusion current flows through the diode, since the charge carriers do not have sufficient energy to overcome the barrier potential. But the minority charge carriers drift across the PN junction causing drift current which is in the range of nA.
2. <u>Forward bias:</u> A diode connected in a circuit is said to be forward biased, if its anode is connected to the positive terminal of the supply and cathode to the negative terminal of the supply.Under forward biased condition, diodes have more conduction and acts as closed switch. The width of the barrier decreases gradually
• 3. <u>Reverse bias:</u> A diode connected in a circuit is said to be reverse biased, if its anode is connected to the negative terminal of the supply and cathode to the positive terminal of the supply.Under reverse biased condition, diodes prevent conduction and acts as open switch.The width of depletion region increases gradually.</td>
<td>2
2
2</td>
<td>7</td>
<td>7</td>
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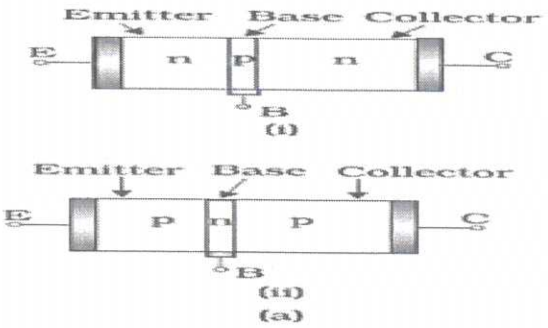
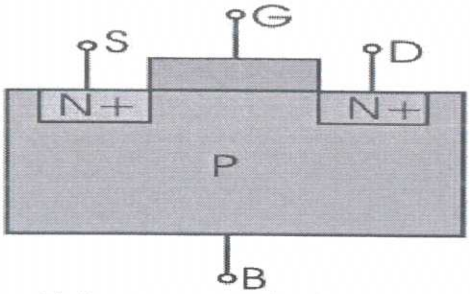
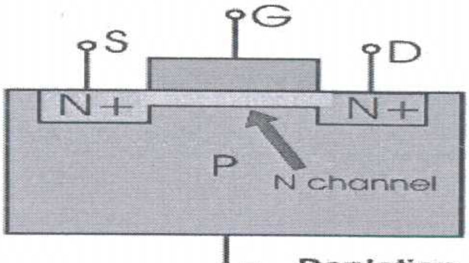
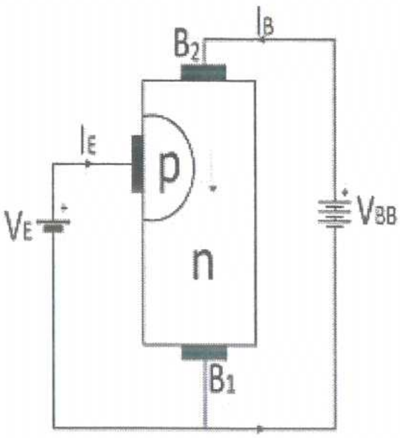
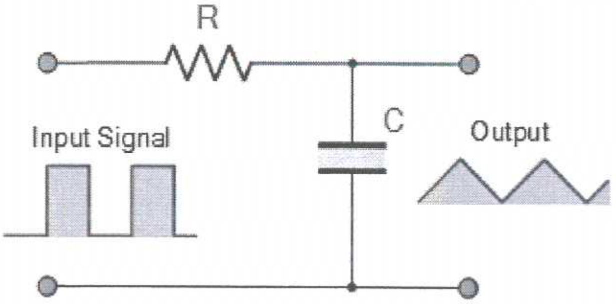
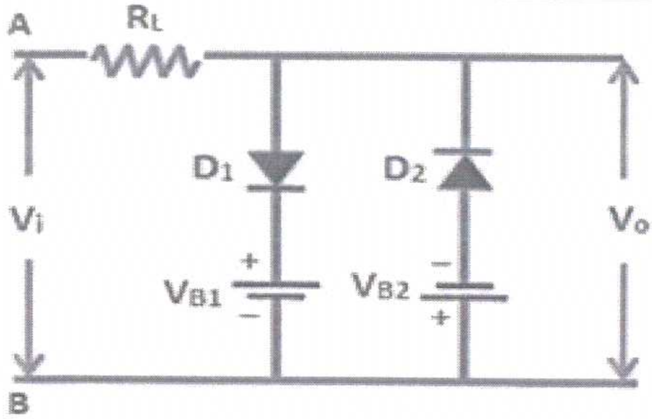
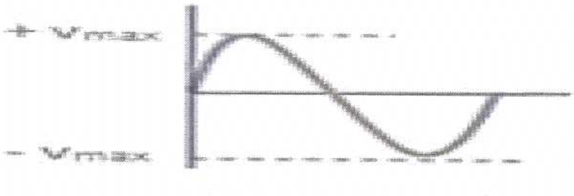
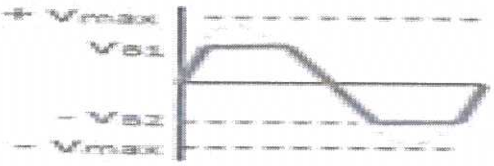
<tr>
<td>III. 03</td>
<td>
<table>
<tr><th>Sl. No.</th><th>Characteristic</th><th>Common Base</th><th>Common Emitter</th><th>Common Collector</th></tr>
<tr><td>1.</td><td>Input resistance</td><td>Low (100 Ω)</td><td>Low (750 Ω)</td><td>Very high (750 kΩ)</td></tr>
<tr><td>2.</td><td>Output resistance</td><td>Very high (450 kΩ)</td><td>High (45 kΩ)</td><td>low (50 Ω)</td></tr>
<tr><td>3.</td><td>Voltage gain</td><td>150</td><td>500</td><td>Less than</td></tr>
</table>
</td>
<td>7*1 = 7</td>
<td>7</td>
<td>7</td>
</tr>
</table>

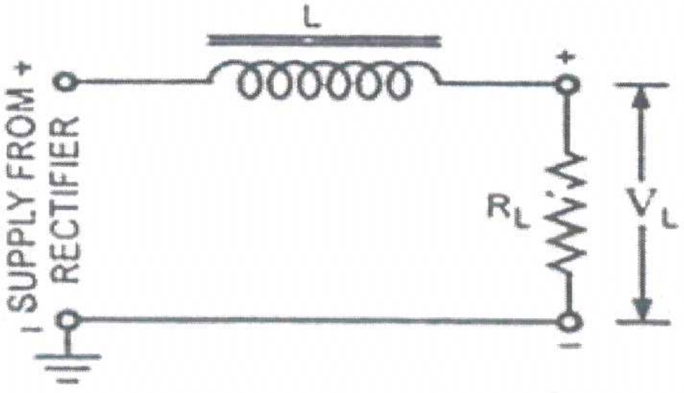
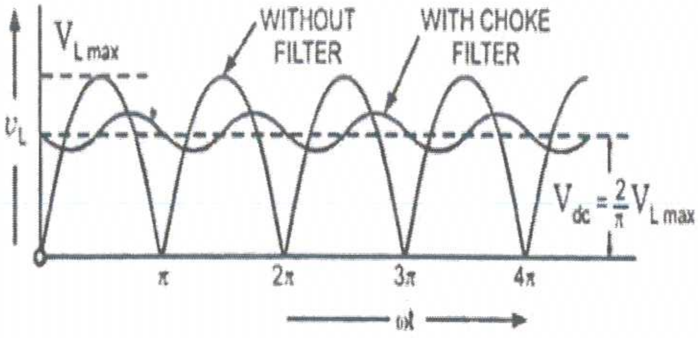
				1
4.	Current gain	Less than 1	Medium (β)	High
5.	Power gain	Low	Very high	Medium
6.	Phase shift	0	180	0
7.	Applications	High frequency	Audio frequency	Impedance matching

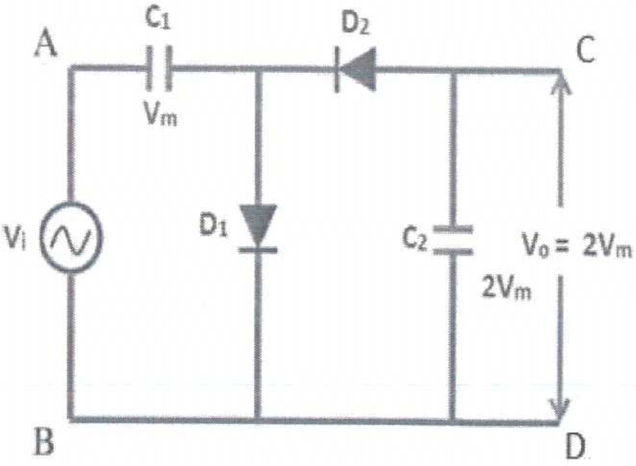
III. 04	A three terminal solid state device which is formed by connecting two diodes back to back. Hence it has got two PN junctions. Three terminals are drawn out of the three semiconductor materials present in it.Bipolar means two polarities(electrons and holes) are responsible for the current through the device. Hence the name Bipolar Junction Transistor (BJT) or simply junction transistors. The three regions of BJT: 1) Emitter: A moderate size and is heavily doped. As this emits majority carriers, it is called as an Emitter. 2) Base: Thin and lightly doped. Pass the majority carriers from the emitter to the collector. 3) Collector: Larger in size than emitter and base and is moderately doped. To collect the charge carriers from the emitter passed through the base. The two junctions of BJT: 1) Junction between emitter and base called as emitter-base junction or simply emitter junction and 2) Junction between collector and base called as collector-base junction or simply collector junction	1 1 1 1 1 2	7	7

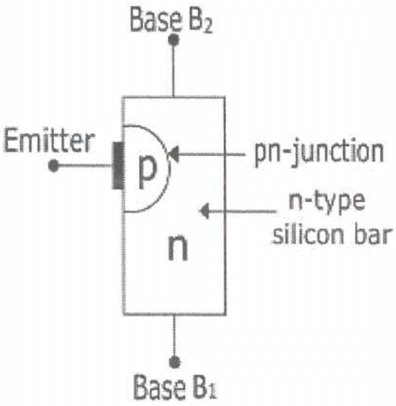
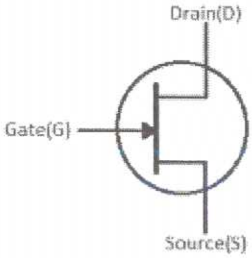
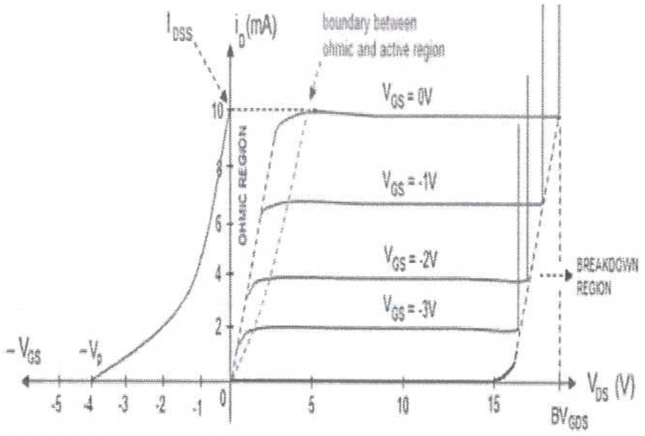
	 (i) (ii) (a)			
III. 05	A four-terminal device with source (S), drain (D) and gate Terminal (G) and body (B) terminals. The body is frequently connected to the source terminal, reducing the terminals to three. The charge carriers enter the channel at source and exit via the drain .It works by varying the width of a channel along which charge carriers flow (electrons or holes).. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide.  Enhancement Mode  Depletion Mode	3 4	7	7

III. 06	 When a positive voltage is applied at the emitter terminal, the pn-junction will remain reverse biased till the input voltage is less than V_1 (voltage between emitter and Base1). A soon as the input voltage at emitter exceeds V_1, the pn-junction becomes forward biased. Under this condition, holes are supplied from p-type region into the n-type bar. These holes are repelled by positive B_2 terminal and attracted towards the B_1 terminal. This increase in the number of holes in the emitter to B_1 region results in the decrease of resistance of this section of the bar. Because of this, the internal voltage drop from emitter to B_1 region is reduced, thus the emitter current (I_E) increases. As more holes are supplied, a condition of saturation is reached. At the point of saturation, the emitter current is limited by the emitter power supply. Now, the device is conducting, hence said to be in ON state.	4 3		7
III. 07	 It is a low pass filter. The time constant of the circuit should be very large. The output is taking across the capacitor. As the input square wave is applied, during the positive half cycle the voltage across capacitor increases from zero, to the maximum	4 (ckt:2 + Graph:2) 3		7

	(peak value of applied voltage). During the negative half cycle, the capacitor starts to discharge and comes to zero. This process repeats for the remaining cycles and a triangular wave is obtained.			
III. 08		3		
	1. Three input cases can be considered, because of two biased potentials(V_{B1} and $-V_{B2}$): I. $V_i > V_{B1}$ Diode,D_1 in on state. Diode,D_2 in off state. $V_o = V_{B1}$ II. $V_i < -V_{B2}$ Diode,D_2 in on state. Diode,D_1 in off state. $V_o = -V_{B2}$. III. $-V_{B2} < V_i < V_{B1}$ As $V_i > -V_{B2}$ Diode,D_2 in off state.As $V_i < V_{B1}$ Diode,D_1 in off state. $V_o = V_i$	2	7	7
	 Input waveform  Output waveform $V_{B1} = +2V$, $V_{B2} = -2V$	2		

III. 09	 The inductor offers high impedance to the ripples (ac components) and no impedance to the desired dc components. Thus the ripple components will be eliminated. When the rectifier output current increases above the average value, energy is stored in inductor in the form of a magnetic field. The energy is given up when the output current falls below the average value in order to balance the effect of the low value of DC.  	3 2 2	7	7
III. 10	During positive input half cycle, the top of a secondary winding of a transformer is positive, the P-terminal of diode D1 is positive while N-terminal is negative this makes the diode forward biased. On the contrary, the N-terminal of diode D2 is positive, and its P-terminal is negative which makes the diode D2 reversed biased. The capacitor C2 will remain uncharged. During the negative input half cycle the top of the secondary winding of the transformer is negative and bottom of the secondary winding of the transformer is positive, the diode D1 will be reversed biased and the diode D2 will be forward biased. Thus, the capacitor C1 will not get charged during negative half cycle while the	3		

	capacitor C2 will gets charged to its peak value. To determine the voltage across capacitor C2, apply Kirchhoff's law to the circuit starting from the secondary winding transformer's bottom point and moving in clockwise direction. $-V_m - V_{c1} - V_{c2} = 0$ Or $V_{c2} = V_m + V_{C1}$ $= V_m + V_m$ $= 2V_m$ Thus, the output voltage thus produced is double of the input AC voltage, and hence called as voltage doubler. A half-wave voltage doubler drives the voltage to the output during one half cycle (either positive or negative half cycle) of the input.  	4	7	7
III. 11	A three terminal semiconductor switching device. It consists of a bar of n-type silicon material with a non-rectifying contact at either end (base 1 and base 2), and with a rectifying contact (emitter) alloyed into the bar part way along its length, to form the only junction within the device (hence the name 'Unijunction'). Also known as Double Base Diode. The emitter junction is placed such that it is more close to terminal Base 2 than Base 1. The emitter is heavily doped while the n-region is lightly doped. Thus, the resistance between base terminals is very high when emitter terminal is open.	3 4		

			7	7
III. 12	 A)  B)	2 2.5*2 = 5 (Drain + Transfer)	7	7