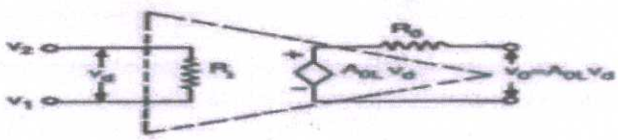
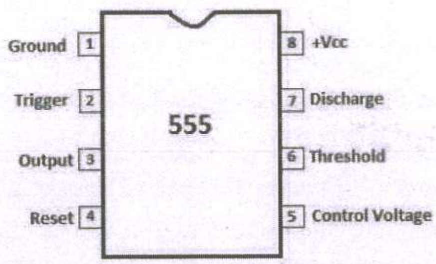
| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
|---|---|---|---|---|
| 1. |  | 1 | | 1 |
| 2. | Common mode rejection ratio of an op-amp is the relative sensitivity of an op-amp to a difference mode gain as compared to common mode gain.It is expressed in decibel<br>CMRR=Adm/Acm | 1 | | 1 |
| 3. | a. Metal can(TO)<br>b. DIP<br>c. Flatpack | Any (1) | | 1 |
| 4. | Log amplifier is a nonlinear op-amp circuit, in which the output voltage produced proportional to logarithm of input signal | 1 | | 1 |
| 5. | a. zero crossing detector<br>b. window detector<br>c. phase detector<br>d. timing marker signal generator | Any(2)<br>0.5*2 | | 1 |
| 6. | **Lock -in range**:- The range frequencies over which the PLL can maintain lock with incoming signal is called Lock -in range | 1 | | 1 |
| 7. |  | 1 | | 1 |

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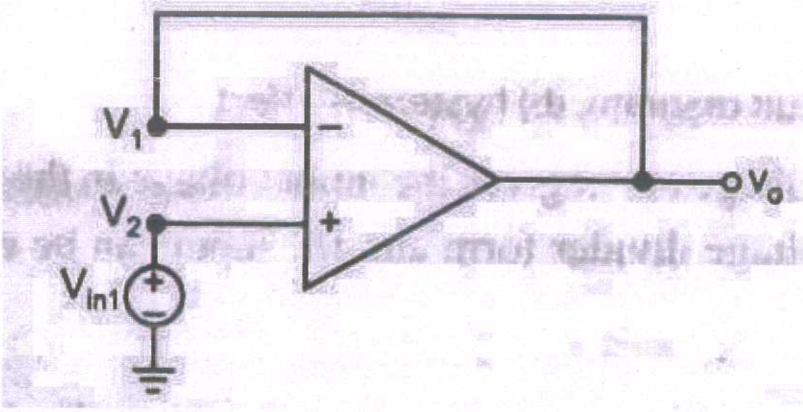
| 8.. | a. Fixed voltage regulators<br>b. Adjustable voltage regulators<br>c. Switching regulators | Any(2)<br>0.5*2 | 1 | 1 |
| 9. | Resolution:- The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to the number of bits. | 1 | | 1 |
| | **PART B** | | | |
| 1. | Voltage follower is a special case of the closed loop unity gain amplifier that produ output voltage equal to the input voltage in same phase. In the closed loop voltage follow can be derived with the help of the op-amps infinite input resistance and low output res characteristics, $R_{in} = \infty$ and $R_o = 0$ as $A_C = 1$.<br><br>The output terminal is c connected to the inverting input terminal without the feedback resistance. This means that the is independent of resistance. Therefore the output fed back to the input is equal to the invertin terminal, $V_o = V_1$. And the non-inverting terminal $V_2$ is connected directly to voltage source $V_i$ $V_2 = V_{in}$. The linear characteristic of ideal op-amp *i.e.,* the virtual short effect forces the diffe voltage equal to zero, $V_D = V_2 - V_1 = 0$ V, $V_1 = V_2$. From this, we can write that the output vol voltage follower,<br>$$V_o = V_{in} = V_1 = V_2.$$<br>Thus the closed loop gain is<br>$$A_C = \frac{V_o}{V_{in}} = 1$$ | Dia1<br>Exp2 | 1+2 | 3 |

| | | Split Up Score | Sub Total | Total |
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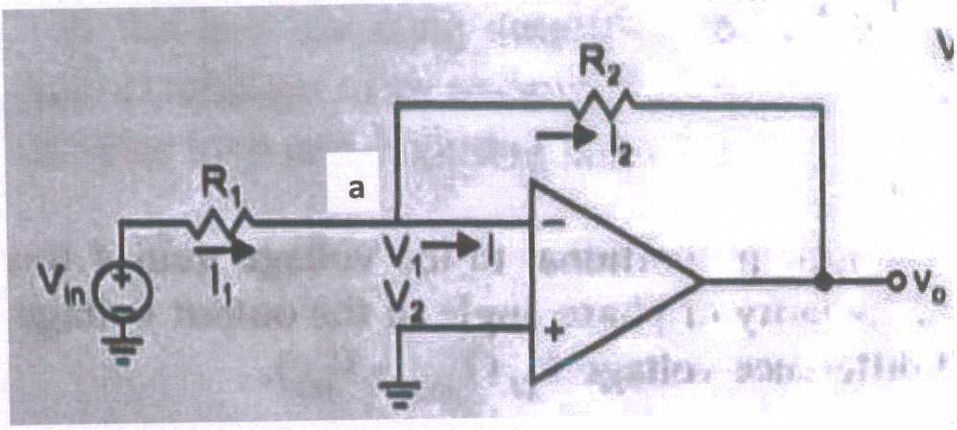
| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | | | |
| 2. | <br>-Inverting amplifier is one of the most widely used closed loop op-amp<br>-Inverting amplifier input voltage Vin drives the inverting terminal of an op-amp and the non-inverting connected to ground<br>-The output voltage vo is fed back to inverting input terminal though Rf-R1 network<br>-Assume ideal op-amp. As Vd=0, node 'a' is at ground potential and the current I1 through R1 is I1 = Vi/R1<br>-Also since op-amp draws no current, all the current flowing through R1 must flow through Rf. Hence the output voltage is<br>Vo = -I1 Rf = -(Vi/R1) Rf<br>therefore the gain of the closed loop inverting amplifier is Acl = Vo/Vi = -Rf/R1<br>-The –ve sign indicates a phase shift of 180° between Vi and Vo. | Ckt2<br>Exp1 | | 3 |
| 3. | $f_o = \frac{1}{2\pi RC}$<br>R=1.59KΩ<br>C=0.05μF<br>**Frequency =2KHz** | 1<br><br>2 | | 3 |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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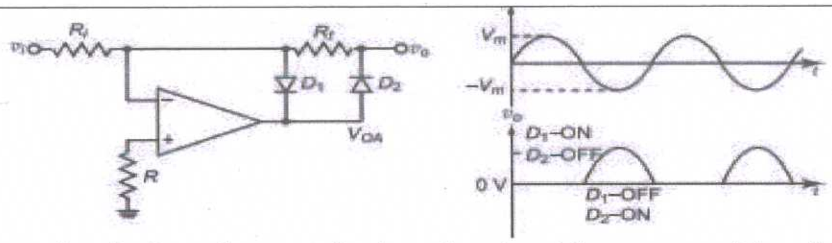
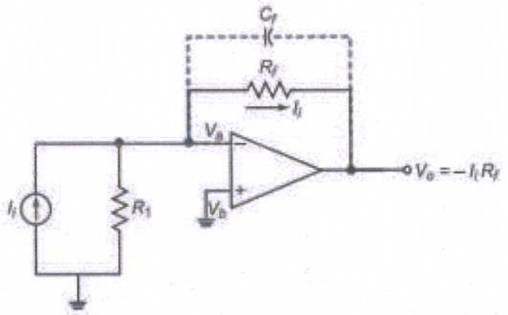
| 4. | <br>When vi > 0, the voltage at the inverting input becomes positive, forcing the output VOA to go negative. This results in forward biasing the diode D1 and the op-amp output drops only by ª 0.7 V below the inverting input voltage. Diode D2 becomes reverse-biased. The output voltage vo is zero since no current flows in the feedback circuit through Rf. Hence, the output vo is zero when the input is positive. When vi < 0, the op-amp output VOA becomes positive, forward biasing the diode D2 and reverse biasing the diode D1. The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when Rf = Ri.and output vo becomes positive | Ckt2<br>Exp1 | | 3 |
| 5. | <br>A current to voltage converter or an ideal current-controlled voltage source, also called transresistance amplifier is the one, whose<br>(i) output voltage is equal to a constant k times the magnitude of an independent input current Ii or in other words, Vo = kIi and<br>(ii) output voltage is independent of the load connected to it. The constant k has the unit of ohms. It is also called as current controlled voltage sources(CCVS) | Ckt2<br>Exp1 | | 3 |

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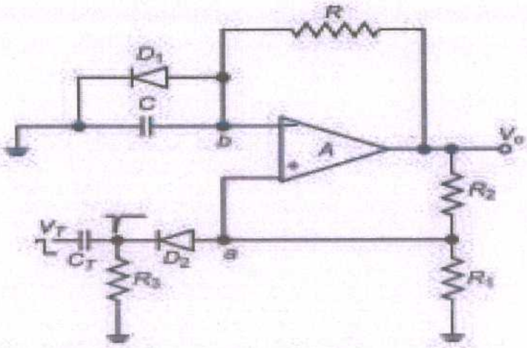
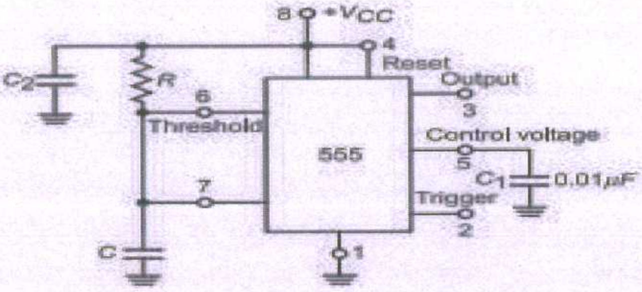
| | Since it is generally easier to measure voltages.current from the photo-devices can be converted to voltage by using this current to voltage converter Due to the virtual ground, Vb = Va = 0, the current through R1 is zero and Ii flows through the feedback resistor Rf . ThusVa=- I R f.In order to reduce the high frequency and possible oscillations, a capacitor Cf is connected across Rf | | | |
| 6. |  | 3 | | 3 |
| 7. |  | 3 | | 3 |

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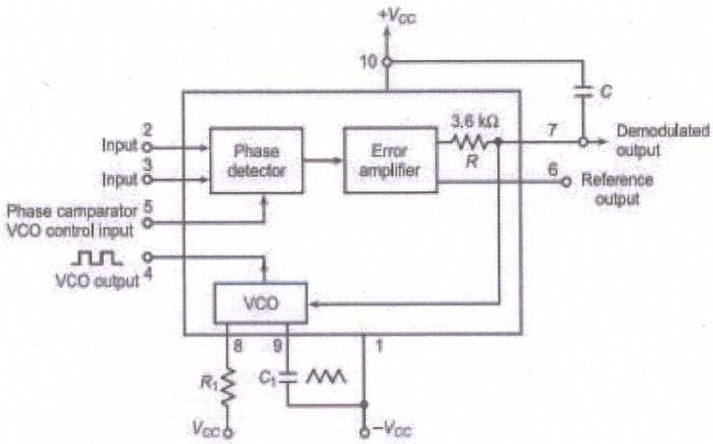
| 8. |  | 3 | | 3 |
| 9. | **Important features of IC 723**<br>External pass transistor is not necessary to produce the output current.<br>It allows the input voltage up to 40 V.<br>It provides the adjustable regulated output from 2V to 38V.<br>The output current can be increased up to 10A by using the external transistors.<br>It can be used as both linear and switching type regulator.<br>It provides the adjustable regulated voltage from 2 to 3V.<br>The maximum load current is 150mA.<br>It can be used for both positive and negative supply regulation.<br>The internal power dissipation is 800 mW.<br>It has a built-in short circuit protection.<br>The temperature drift is very low.<br>It has a high ripple rejection.<br>It has the linear or fold back current limiting facility.<br>It provides the guaranteed performance over the temperature range 0° to 70°C<br>It provides 0.01% line and 0.03% load regulation. | (0.5x 6pt) | | 3 |

<table>
<tr><td></td><td>SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits</td><td>Split Up Score</td><td>Sub Total</td><td>Total</td></tr>
<tr><td>10.<br><br><br><br><br><br><br>1</td><td><u>Monotonicity</u> :-A D/A converter is monotonic if its output value increases as the binary inputs are incremented from one value to the next<br><u>Linearity</u>:-Important measure of its accuracy and tells us how close the converter output is to ideal transfer characteristic<br><u>Settling time</u>:-The time required for the output of D/A converter to settle down to within±(1/2)LSB of the final value for a given digital input is known as settling time<br><u>Part C</u><br><br>i)Input offset voltage<br>ii )Input offset current<br>iii) Input bias current<br>iv)Input resistance<br>v)SVRR<br>vi)Slew rate<br>vii)CMRR<br>viii)Output resistance<br>ix) Gain band width product<br><br>Input offset voltage It is the voltage that must be supplied between the two input terminals of an op-amp for making the output zero. For 741C, the maximum value of input offset voltage is ±60 mV<br><br>Input offset current The algebraic difference between the two currents entering the inverting (–)input and non-inverting (+) input is referred to as the input offset current. For IC 741C, the maximum value of offset current is 200 nA.<br><br>The input bias current is the average of the currents that flow into the inverting and non-inverting input terminals of an op-amp. The input bias current affects all applications of op-amps<br><br>Input resistance:-It is the resistance across the two input terminals of op-amp under open loop condition<br><br>PSRR:-The internal circuitry of an op-amp is very sensitive to variations in supply voltages. Hence, the power supply used for the op-amp is preferred to have low noise and good regulation characteristics. This sensitivity is indicated by the maximum offset voltage versus supply voltage. The reciprocal of sensitivity is defined as the Power Supply Rejection Ratio (PSRR) or Supply Voltage Rejection Ratio (SVRR)</td><td>(1x3)<br><br><br><br><br><br>List1<br>+<br>Any<br>5x1</td><td></td><td>3</td></tr>
</table>

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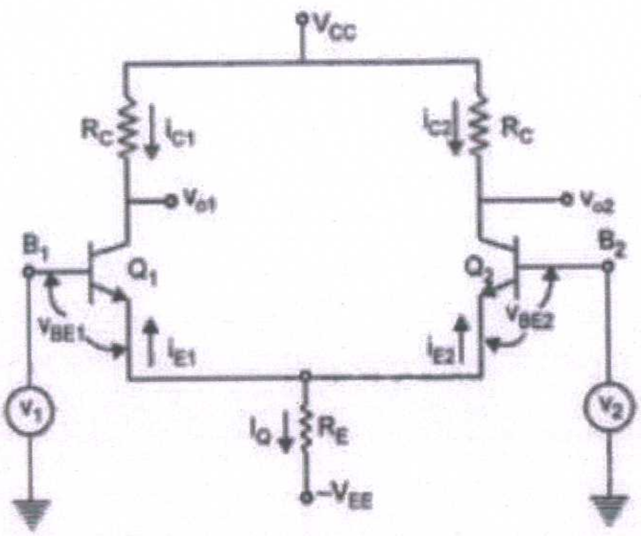
| | Slew rate :It is defined as the maximum rate of change of output voltage realised by a step input voltage, and it is usually specified in units of V/ms. The slew rate of the op-amp is related to its frequency response<br><br>CMRR The common-mode rejection ratio is defined as the rat of the differential gain Adm to the common-mode gain Acm.<br>$CMRR = \frac{A_{dm}}{A_{cm}}$<br><br>This represents the figure of merit for the differential amplifier and it is usually represented in decibels (dB).<br><br>Gain band width product:-due to parasitic junction capacitance and minority carrier charge storage voltage gain decrease at high frequency this aspect of op-amp is characterized by gain bandwidth product | | | |
| 2. | The differential is an amplifier that amplifies the difference between to voltages and rejects and common mode value of the voltages<br><br> | | | |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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| | The differential amplifier circuit configured in four different ways based on the input and output connection<br>a)Dual Input Balanced Output- In this configuration two inputs are given an output is taken from both the transistors.<br><br>b)Dual Input Unbalanced Output- The input is given to both the transistors but the output is taken from a single transistor.<br><br>c)Single Input Balanced Output- Here, by providing single input we take the output from two separate transistors.<br><br>d)Single Input Unbalance Output- It is a type of configuration in which a single input is given an output is taken from only a single transistor<br><br>The two separate transistors possess similar characteristics ideally. Common emitter resistor $R_E$, common positive supply $V_{CC}$ and common negative supply $V_{EE}$ is shared by both the transistors.<br>-When both B1and B are joined together and connected to common mode voltage as Transistor Q1and Q2are matched and due to symmetry of the circuit ,the current IQ divides equally through transistors Q1andQ2.<br>IE1=IE2=IQ/2<br>IC1=IC2=αf IQ/2<br>V01=Vcc- αf IQ/2RC=V02<br>The difference of voltage between the two collectors will be zero. The differential pair reject common mode signal. | Ckt4<br>3exp | | 7 |
| 3. | The basic comparator is used in open-loop mode. Since the open loop gain of the op-amp is very large, false triggering at the output can occur even due to a few tenths of millivolts peak of the input or less. When the input changes slowly as compared to the output, noise is coupled from the output of the comparator back to the input. The comparator circuit designed with a positive feedback to avoid such an unwanted triggering is called the Schmitt Trigger or the Regenerative Comparator | | | |

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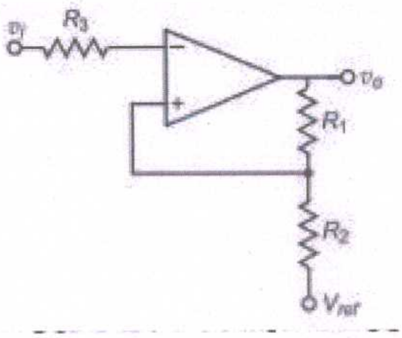
The regenerative comparator or the inverting Schmitt Trigger. It consists of an inverting comparator provided with positive feedback. The input voltage to be wave-shaped is applied to the (–) input terminal and the feedback voltage is applied to the (+) input terminal. The input voltage vi triggers the output vo every time it crosses certain voltage levels. These voltage levels are called Upper Threshold Voltage VUT and




The difference between the two threshold voltages VUT and VLT is called the hysteresis voltage, VH = VUT – VLT. The voltage span of hysteresis is set to be greater than the peak-to-peak noise voltage. Therefore, there will not be any incorrect output variations due to noise signals. The threshold voltage values can be obtained as follows. Suppose the output is at positive saturation with v o = +Vsat, then the voltage at (+) input terminal is given by The difference between the two threshold voltages VUT and VLT is called the hysteresis voltage,

VH = VUT – VLT.

The voltage span of hysteresis is set to be greater than the peak-to-peak noise voltage. Therefore, there will not be any incorrect output variations due to noise signals.

The threshold voltage values can be obtained as follows. Suppose the output is at positive saturation with v o = +Vsat, then the voltage at (+) input terminal is given by

$$V_{ref} + \frac{R_2}{R_1 + R_2}\left(V_{sat} - V_{ref}\right) = V_{UT}$$

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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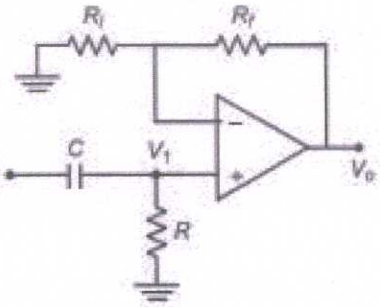
| | where VUT is the upper threshold voltage. The output voltage vo remains constant at +Vsat as long as vi is less than VUT. When vi is just slightly more positive than VUT, the output vo switches from +Vsat to –Vsat and remains at the same level, as long as vi is greater than VUT. When Vo = – Vsat, the voltage at the (+) input terminal is given by<br>$V_{ref} - \frac{R_2}{R_1+R_2}(V_{sat}+V_{ref}) = V_{LT}$<br>This voltage is identified as Lower Threshold Voltage VLT. The input voltage vi must be slightly more negative than VLT to switch vo from –Vsat to +Vsat | Ckt4<br>Exp3 | | 7 |
| 4.. | <br>Given $f_L = 2\ kHz$<br>Let $C = 0.01\ \mu F$<br>We know that $f_L = \frac{1}{2\pi RC}$<br>Therefore, $R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi(2\times10^3)\times10^{-8}} = 7.95\ k\Omega$<br>$A = 1 + \frac{R_f}{R_i} = 2$<br>Therefore, $R_f = R_i = 10\ k\Omega$ (say) | Ckt2<br>+<br>Pb5 | | 7 |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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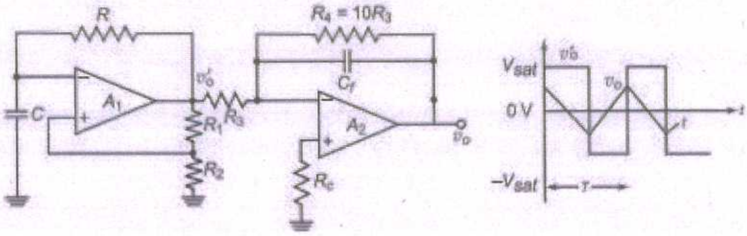
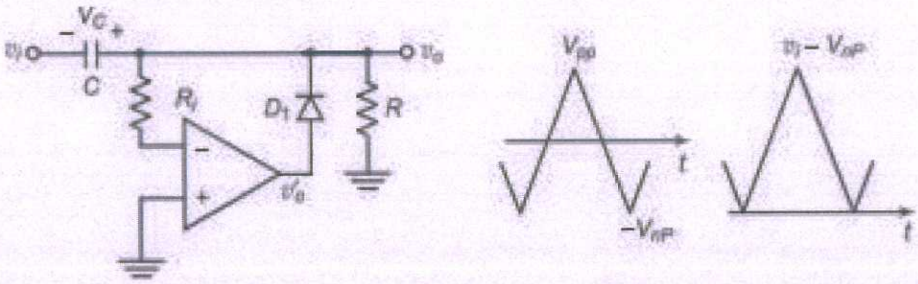
| 5. | <br>Let us assume that the voltage $v'_o$ is high at $+V_{sat}$. This forces a current of $+V_{sat}/R_3$ through capacitor $C_f$ of the integrator, producing a negative ramp at the output of the integrator. When $v'_o$ is low at voltage $-V_{sat}$, the output of integrator ramps up linearly. This cycle repeats itself and hence the frequency of the triangular wave is the same as that of the square-wave. Hence, the value of resistor $R$ connected in the square-wave generator part of the circuit determines the frequency of the triangular wave. The amplitude of the triangular wave decreases with an increase in frequency value. This is due to the fact that the capacitive reactance decreases at high frequencies and increases at low frequencies. | Ckt4<br>Wfm 1<br>Exp2 | | 7 |
| 6. | <br>A clamper circuit is used to add a fixed voltage level to the minimum or maximum value of an input signal. The output is clamped to a desired level by either shifting up or shifting down an input signal, depending on whether a positive or negative clamping action is required. A typical example of a clamper circuit is the dc restorer used in television circuit to restore the dc level for the video signal. This circuit is also called a dc inserted . | | | |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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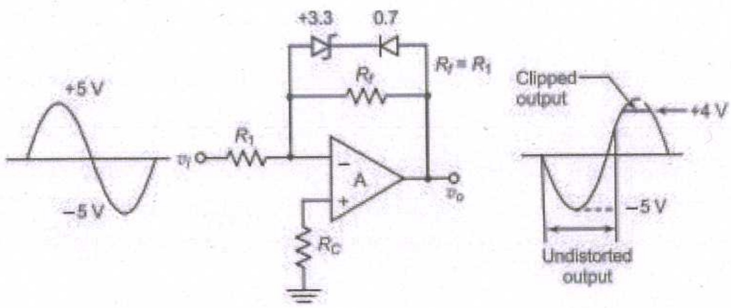
| | The positive clamping circuit. The input signal vi is applied at the negative input terminal through a capacitor C. During the negative half-cycle transition of the input voltage, the output of op-amp becomes positive. The diode D1 connected at the output of op-amp is forward-biased and this causes the capacitor to get charged. The charging continues until the inverting input terminal of the op-amp attains virtual ground condition. At that instant, the peak voltage VC across the capacitor becomes equal to the negative peak of input signal Vnp .VC = Vnp where V np is the negative peak amplitude of input signal. When the input voltage goes positive, diode D1 becomes reverse-biased. The capacitor retains the previous voltage VC. The output voltage vo is then given by v o = vi + VC = vi + Vnp.The voltage vi is hence shifted by the voltage across capacitor.<br>Clipper<br>A clipper, also called an amplitude limiter, consists of an inverting amplifier circuit with a backto-back Zener diode and a signal diode connected in the feedback loop<br>The gain of the circuit is determined by the ratio of resistors R f./R1. The signal to be clipped is applied to the inverting input of the op-amp. The output vo follows the input vi with 180° phase difference, if the Zener diode and signal diode do not exist in the feedback path.<br><br> | 3.5+<br>3.5 | | 7 |

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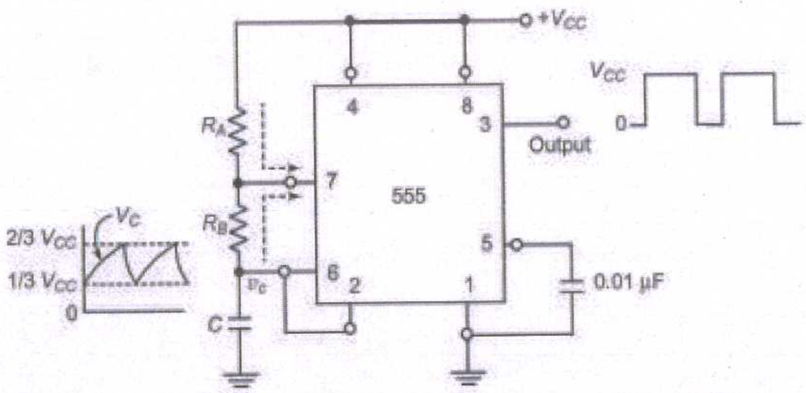
| | Let us assume that a ±5 V peak sine wave input signal vi is applied, the breakdown voltage of Zener diode is 3.3V and the cut-in voltage of diode is 0.7 V. Then, for an output voltage of VZ + VD (3.3 V + 0.7 V = 4 V), the Zener diode avalanches. The output signal is clipped or limited to this voltage, until the transition at the input signal makes the output to fall below 4V. When the input voltage is less than 4V, the circuit acts just like an inverting amplifier with a gain of Rf /R1 during the remaining duration of the cycle. Then the diodes do not affect the inverting amplifier operation. This is due to the fact that, when the output voltage becomes negative, the semiconductor diode gets reverse biased and makes the Zener diode path open and inactive | | | |
| 7. | <br>When the power supply VCC is connected to the circuit, the capacitor C charges towards VCC. The charging rate is determined by the time constant (RA + RB)C. During this period, the output (pin 3) is) is high, since R = 0, S = 1 and thus Q = 0 | | | |

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When the capacitor voltage reaches and rises just above (2/3)VCC, the upper comparator triggers, and resets the flip-flop (FF). This makes internal discharge transistor Q1 ON, resulting in the capacitor C discharging towards ground through the resistance RB and Q1. The time constant for discharging is RBC. Since current can also flow through RA into Q1, the resistance RA and RB are to be made large enough to limit this current. A maximum current of 0.2A can be allowed to flow through the ON transistor Q1.When the timing capacitor C discharges, as it reaches and goes just less than (1/3)VCC, the lower comparator gets triggered. This sets the flip-flop making Q = 0. This results in unclamping the external timing capacitor by switching Q1 OFF. This cycle of charging to (2/3)VCC, and discharging to (1/3) VCC repeats. timing sequence and capacitor voltage waveform during the astable operation. The output (pin 3) is high during the internal charging of the capacitor from (1/3)VCC to (2/3) VCC.

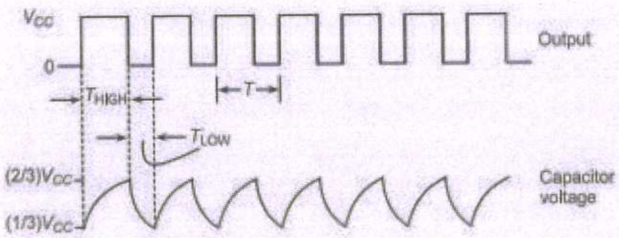
During discharging period -Td= 0.693 RC

During charging period-Ton= 0.693(RA + RB)C

T = Td + Ton

T = 0.693(RA + 2RB)C

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

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| Ckt3<br>Exp3<br>Wfm<br>1 | | 7 |

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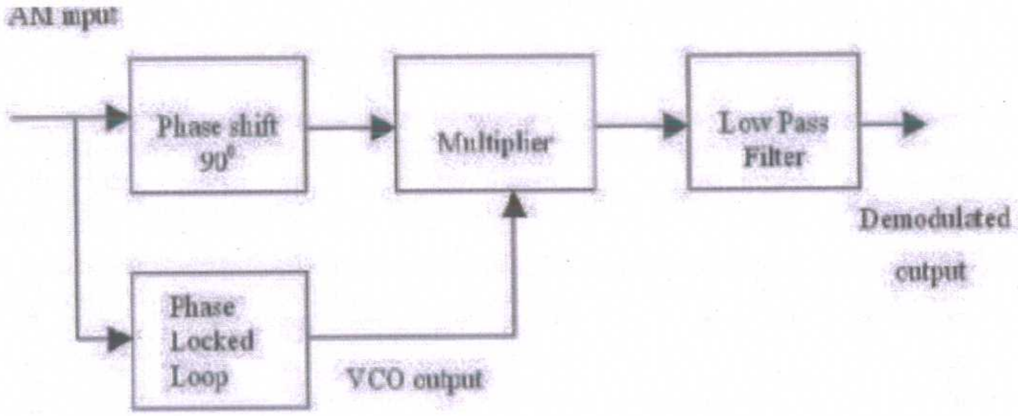
| 8. | | | | |

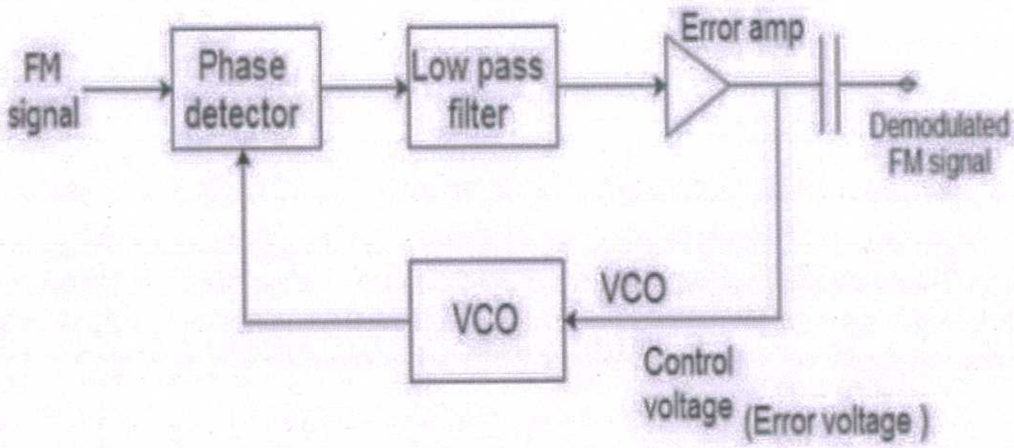



-AM signal is applied to PLL;It produce a carrier output with a same frequency by locked to the carrier frequency of the incoming.

-A PLL always provides an output with 90°phase of an incoming signal

-Multiplier accepts two signals and produce its output contain sum and difference signals to the LPF

-After filtering low pass filter leaves the demodulated signal to the output terminal of AMdetector



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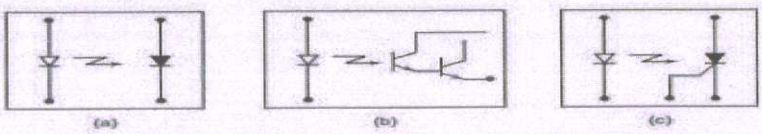
|---|---|---|---|---|
| | -An FM signal is applied as a one input to the phase detector other input is output of VCO<br>-VCO provides 90⁰ phase difference for its input<br>-Phase detector utilizes two input with same frequency and 90⁰ phase difference .It responds zero error voltage to the output terminal that is the loop locked in an equilibrium state. From this output low pass filter produce fm detector output is equael to zero<br>-When the phase detector inputs are having phase and frequency difference ,it develop An error voltage as an output voltage | 3.5+3.5 | | 7 |
| 9. | -An opto-coupler is a solid state component in which the light emitter, the light path and the light detector are all enclosed within the component and cannot be changed from outside. As the opto-coupler provides electrical isolation between two circuits, it is also called an opto-isolator<br>- An opto-coupler, also called an opto-electronic coupler, generally consists of an infrared LED and a photo-detector such as PIN photo diode for fast switching, photo transistor Darlington pair, or photo-SCR combined in a single package. Optoisolators transduce input voltage to a proportional light intensity by using LEDs. The light is transduced back to output voltage using light sensitive devices. GaAs LEDs are used to provide spectral matching with the silicon sensors.<br>The schematic diagrams of the opto-couplers using a photodiode, photo Darlington pair and photo-SCR<br><br><br>*Schematic representation of opto-couplers using (a) Photodiode, (b) Photo-Darlington pair, and (c) Photo-SCR* | | | |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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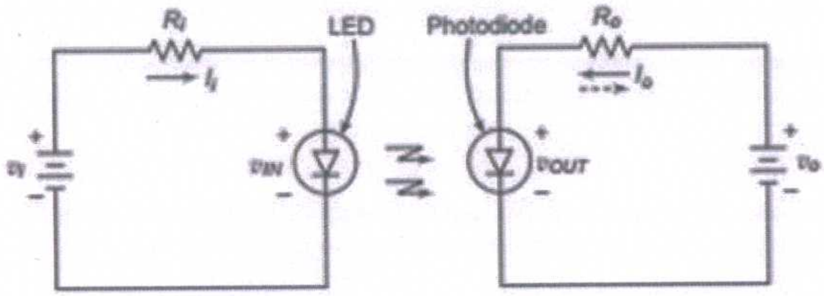
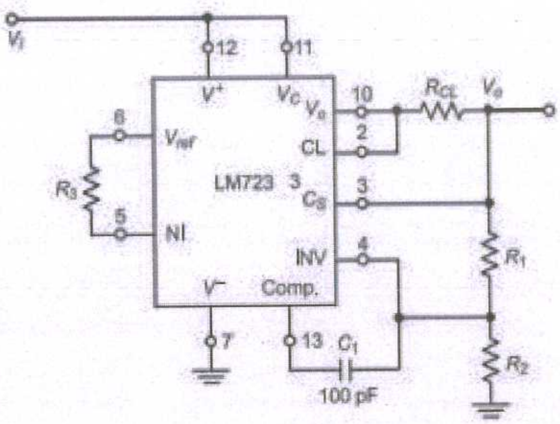
| | <br> | Ckt4<br>+3 | | 7 |
| | -The basic arrangement for the use of an opto-coupler the source vi and series resistor Ri determines the forward current Ii through the LED.<br>-The light emitted from the LED depends on the signal vi.This light incident on the photo diode generates a reverse current in the output circuit through the resistor Ro<br>-The drop across the resistor Ro is proportional to the input voltage ,and it varies proportionately with change in input signal source. | | | |
| 10. | <br> | | | |

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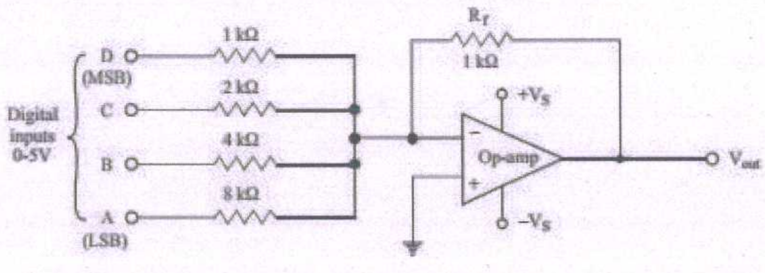
| | -The IC 723 can be used for designing a high voltage regulator for output voltages ranging from 7 V to 37 V.<br>-The non-inverting input (NI) terminal is directly connected to Vref through R3.<br>-The inverting input (INV) terminal is connected to the junction of resistors R1 and R2 connected with the output Vo.<br>-The resistor R3 is selected to be equal to R1 \|\| R2. Then the error amplifier acts as a non inverting amplifier with a voltage gain.<br>$A_V = 1 + \frac{R_1}{R_2}$.<br>The output voltage is given by<br>$V_o = V_{ref}\left(1+\frac{R_1}{R_2}\right) = 7.15\left(1+\frac{R_1}{R_2}\right)$ | Ckt4<br>exp3 | | 7 |
| 11. | Binary weighted DAC<br>In this method, the circuit contains one resistor or current source for each bit of the D/A converter connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less.<br> | | | |

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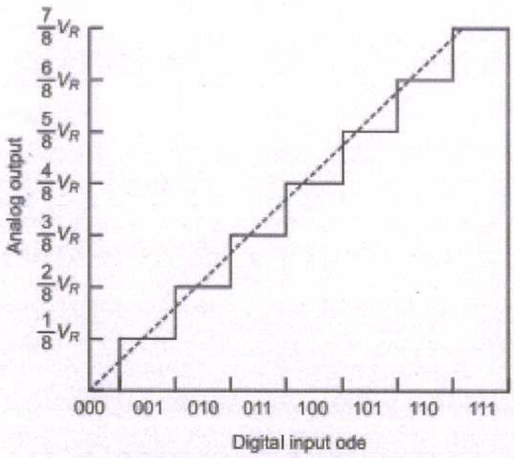
| | 4-bit D/A converter using binary weighted conversion technique. As seen from this figure, the circuit makes use of an op-amp in the inverting amplifier configuration. It has 4 resistors with one of their ends connected to four inputs A, B, C and D and there other ends connected together to the inverting input. The op-amp acts as a summing amplifier which produces the weighted sum of its input voltages. the summing amplifier multiplies each input voltage by the ratio of Rf/Rin<br>The summing amplifier output may be expressed as<br>$V_{out} = -\left(V_D + \frac{1}{2}V_C + \frac{1}{4}V_B + \frac{1}{8}V_A\right)$<br>The negative sign is there because of the 180°-phase shift introduced by op-amp being used in the inverting amplifier configuration.<br><br><br>Graphical representation | Ckt4<br>+<br>Exp3 | | 7 |

| | SCHEME OF EVALUATION<br>(Scoring Indicator)<br>Revision:2021 Course code:4043<br>Course :Linear Integrated Circuits | Split Up Score | Sub Total | Total |
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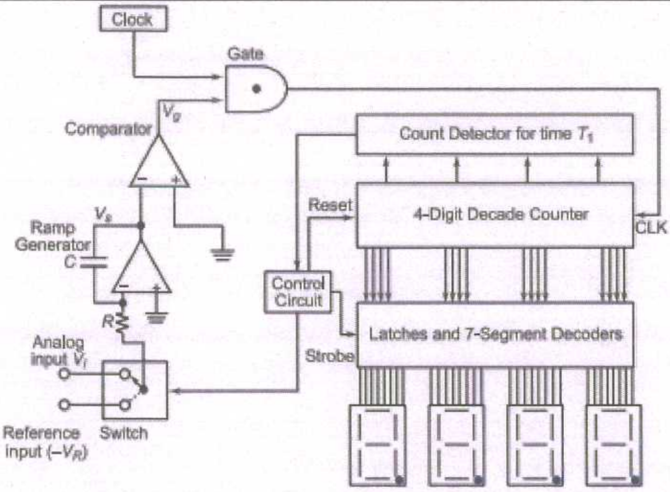
| 12. | <br>In dual slope type A/D converter, the integrator generates two different ramps, one with the unknown analog input voltage Vi as the input, and another with a known reference voltage (–VR) as the input. Hence, it is called dual slope type A/D converter<br>The operation of dual slope type A/D converter is explained as follows. Assume that the 4-digit decade counter is initially reset to 0000, the ramp output Vs is reset to 0V, analog input voltage is positive, and the input to the ramp generator or integrator is switched to the unknown analog input voltage. Since the positive analog input voltage is connected to the inverting input of the integrator, the integrator output Vs is a negative ramp while the comparator output Vg is positive, and the CLK is passed through the AND gate. This results in counting-up of the 4-digit decade counter | 4ckt<br>3exp | | 7 |

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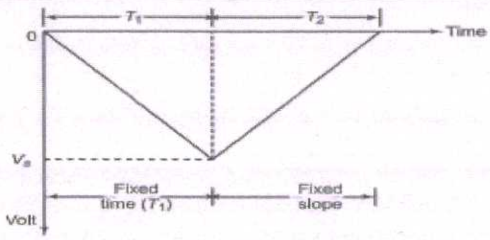


The negative ramp will proceed for a fixed time period $T_1$, which is determined by a count detector for the time period $T_1$. At the end of fixed time period $T_1$, the ramp voltage is given by

$$-V_s = \frac{V_i}{RC} \times T_1$$

When the counter reaches the fixed count at time period T1, the count detector gives a signal to the control circuit which in turn resets the counter to 0 and switches the integrator input to a negative reference voltage (–VR). Now, the ramp generator begins at –Vs and increases upward until it reaches 0 V. During this time, the counter gets advanced. When Vs reaches 0 V, the comparator output will become 0 and the CLK is inhibited from passing through the AND gate. Now, the conversion cycle is said to be completed and the positive ramp voltage is given by

$$V_s = -\left(\frac{-V_R}{RC} \times T_2\right)$$

where VR and RC are constants and the time period T2 is variable.

Since the ramp generator voltage starts at 0 V, decreasing down to –Vs and then increasing up to 0 V, the amplitude of negative and positive ramp voltages