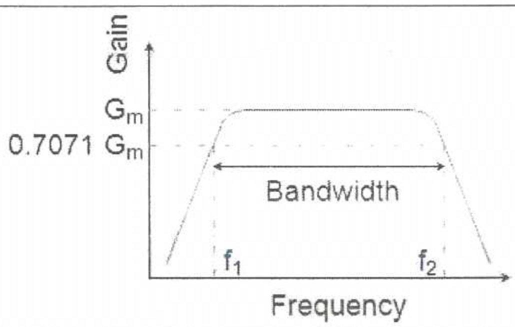
175 14/11/23

11 Nov-23

Scoring Indicators

COURSE NAME :ELECTRONIC CIRCUITS

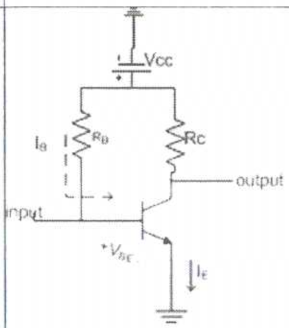
COURSE CODE :3043 **QID :2110220222**

Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			**9**
I. 1	The operating point of a device, also known as a bias point, quiescent point or Q-point, is the steady-state DC voltage or current at a specified terminal of an active device such as a transistor with no input signal applied.	1	1	
I. 2	Ic/Ib	1	1	
I. 3	The quality factor of a resonant circuit describes the quality or performance of the resonant circuit.	1	1	
I. 4	50-70%	1	1	
I. 5	$Af = A/1 + A\beta$ $Af = A/1 - A\beta$	1	1	
I. 6	$f_o = \frac{1}{2\pi(\sqrt{6})CR}$	1	1	
I. 7	musical instruments, voice synthesis, and GPS units,	1	1	
I. 8	T = 0.693 (RA + 2 RB) C.	1	1	
I. 9	two	1	1	
	PART B			24
II. 1		3	3	
II. 2	The important features of Emitter Follower are –	Any 3	3	

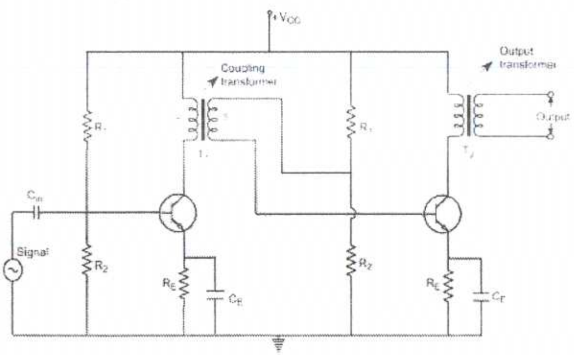
<table>
<tr><td></td><td>

- It has high input impedance
- It has low output impedance
- It is ideal circuit for impedance matching
- Gain unity

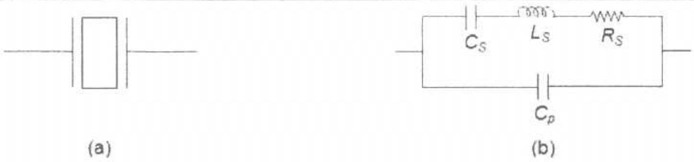
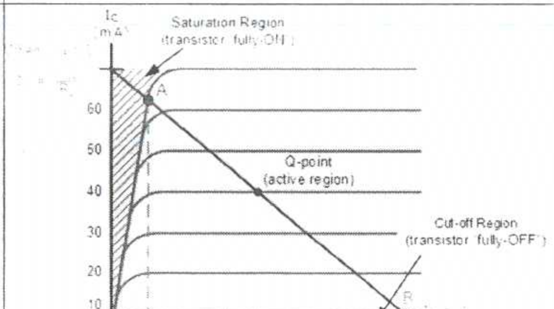
All these ideal features allow many applications for the emitter follower circuit. This is a current amplifier circuit that has no voltage gain.</td><td></td><td></td><td></td></tr>
<tr><td>II. 3</td><td>

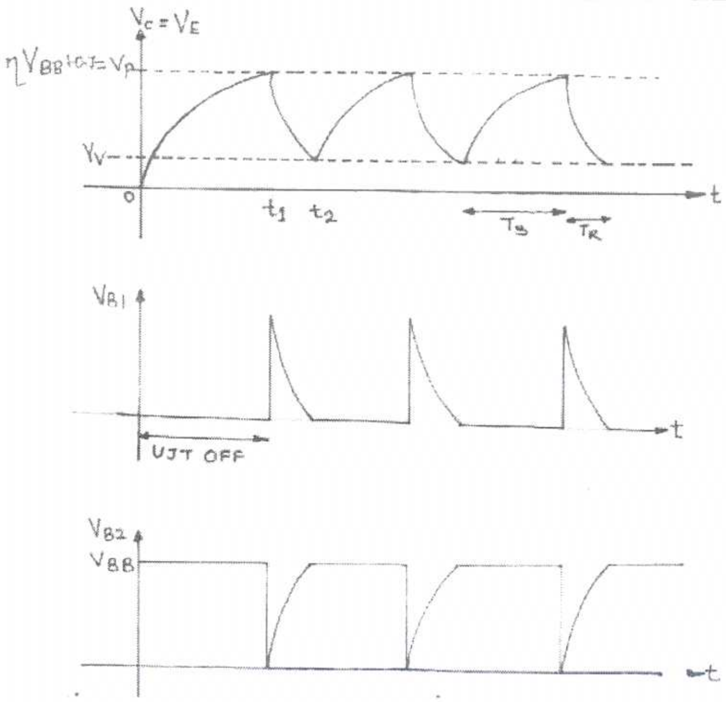


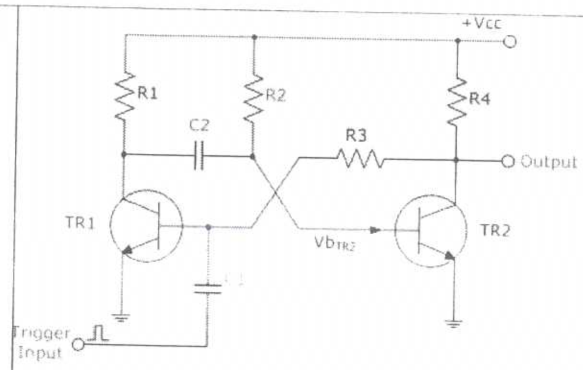
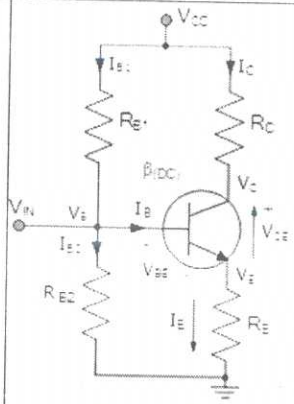
It consists of a dc voltage Vcc for biasing and base resistor R_B. Together they provide a 'fixed' base current(I_B). (For a given circuit, values of Vcc and R_B are constant, so they provide a fixed current).</td><td>2+1Exp</td><td>3</td><td></td></tr>
<tr><td>II. 4</td><td>Resonant Frequecy/band width =100</td><td>3</td><td>3</td><td></td></tr>
<tr><td>II. 5</td><td>

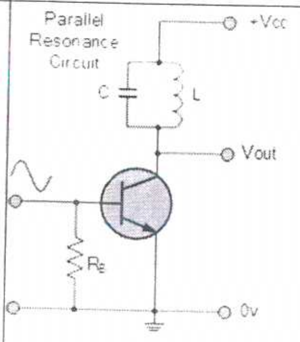


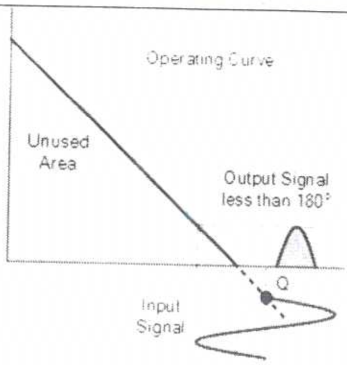
</td><td>3</td><td>3</td><td></td></tr>
<tr><td>II. 6</td><td>The UTP and LTP in Schmitt trigger are nothing but UTP stands for upper trigger point, whereas LTP stands for the lower trigger point. Hysteresis can be defined as when the input is higher than a certain chosen threshold (UTP), the output is low. When the input is below a threshold (LTP), the output is high; when the input is between the two, the output retains its</td><td>3</td><td>3</td><td></td></tr>
</table>

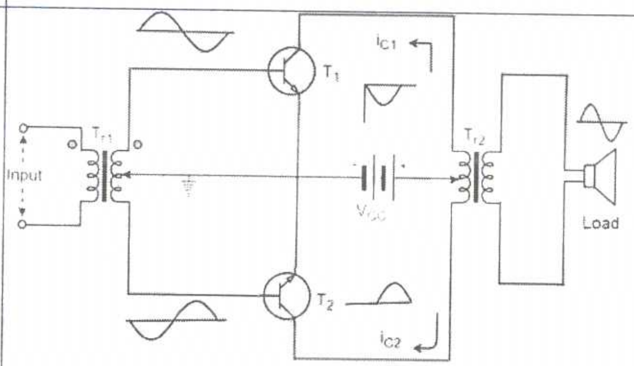
	current value. This dual threshold action is called hysteresis			
II. 7	 **Figure 1 (a) Quartz Crystal (b) Equivalent Electric Circuit** The principle of crystal oscillators depends upon the Piezo electric effect. Series Resonant Frequency, fs which occurs when the series capacitance CS resonates with the series inductance LS. At this stage, the crystal impedance will be the least and hence the amount of feedback will be the largest. $f_s = \frac{1}{2\pi\sqrt{L_s C_s}}$ Parallel Resonant frequency, fp which is exhibited when the reactance of the LSCS leg equals the reactance of the parallel capacitor Cp i.e. LS and CS resonate with Cp. At this instant, the crystal impedance will be the highest and thus the feedback will be the least. $f_p = \frac{1}{2\pi\sqrt{L_S \frac{C_P C_S}{C_P + C_S}}}$	1+2	3	
II. 8	 As a transistor switch, it operates in two regions and those are Saturation Region (fully-ON) and the Cut-off Region (fully-OFF).	2+1 Exp	3	

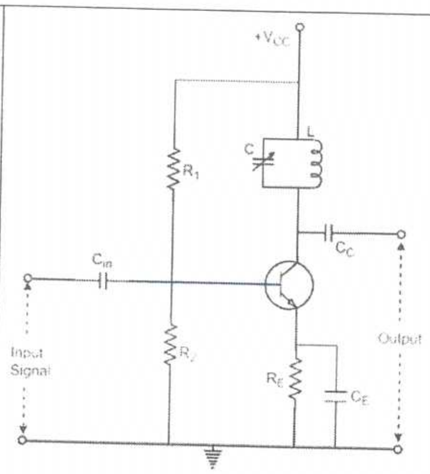
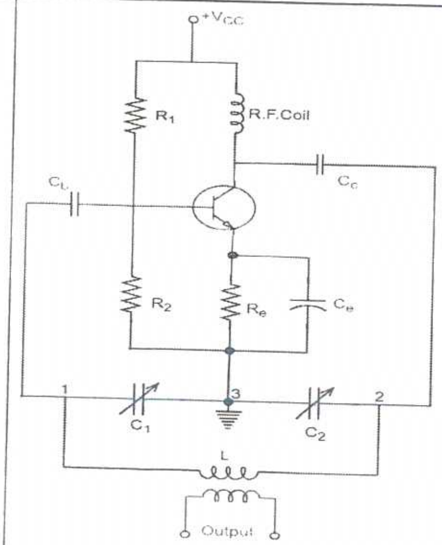
II.9		3	3	

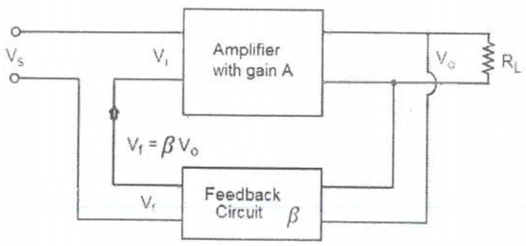
<table>
<tr><td>II.10</td><td>
</td><td></td><td>3</td><td></td></tr>
<tr><td></td><td>PART C</td><td></td><td></td><td>42</td></tr>
<tr><td>III. 1</td><td>

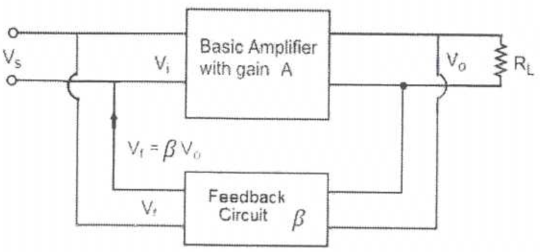
$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$
$V_E = I_E R_E = V_B - V_{BE}$
$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$
$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right) V_{CC}$
$I_{B2} = \frac{V_B}{R_{B2}}$
$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$
$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}}$ $\quad I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta)R_E}$
$I_C = \beta_{(DC)} I_B$
$I_E = I_C + I_B = \frac{V_E}{R_E}$</td><td>4+3</td><td>7</td><td>7</td></tr>
<tr><td>III. 2</td><td><table>
<tr><th>S.No</th><th>Particular</th><th>RC Coupling</th><th>Transformer Coupling</th><th>Direct Coupling</th></tr>
<tr><td>1</td><td>Frequency response</td><td>Excellent in audio frequency range</td><td>Poor</td><td>Best</td></tr>
<tr><td>2</td><td>Cost</td><td>Less</td><td>More</td><td>Least</td></tr>
<tr><td>3</td><td>Space and Weight</td><td>Less</td><td>More</td><td>Least</td></tr>
<tr><td>4</td><td>Impedance matching</td><td>Not good</td><td>Excellent</td><td>Good</td></tr>
<tr><td>5</td><td>Use</td><td>For voltage amplification</td><td>For Power amplification</td><td>For amplifying extremely low frequencies</td></tr>
</table></td><td></td><td>7</td><td>7</td></tr>
<tr><td>III. 3</td><td>


</td><td>4+3Exp</td><td>7</td><td>7</td></tr>
</table>

	The Class C Amplifier design has the greatest efficiency but the poorest linearity. The class C amplifier is heavily biased so that the output current is zero for more than one half of an input sinusoidal signal cycle with the transistor idling at its cut-off point. In other words, the conduction angle for the transistor is significantly less than 180 degrees, and is generally around the 90 degrees area. While this form of transistor biasing gives a much improved efficiency of around 80% to the amplifier, it introduces a very heavy distortion of the output signa.			
III. 4	Resonant Frequency, $F_R = 1/2\pi\sqrt{LC}$ 1.3MHz	3+4	7	7
III. 5	 When no signal is applied at the input, the transistors T1 and T2 are in cut off condition and hence no collector currents flow. As no current is drawn from VCC, no power is wasted. When input signal is given, it is applied to the input transformer Tr1 which splits the signal into two signals that are 180° out of phase with each other. These two signals are given to the two identical transistors T1 and T2. For the positive half cycle, the base of the transistor T1 becomes positive and collector current flows. At the same time, the transistor T2 has negative half cycle, which throws the transistor T2 into cutoff condition and hence no collector current flows.	4+3Exp	7	7

III. 6	 The high frequency signal that has to be amplified is applied at the input of the amplifier. The resonant frequency of the parallel tuned circuit is made equal to the frequency of the signal applied by altering the capacitance value of the capacitor C, in the tuned circuit. At this stage, the tuned circuit offers high impedance to the signal frequency, which helps to offer high output across the tuned circuit. As high impedance is offered only for the tuned frequency, all the other frequencies which get lower impedance are rejected by the tuned circuit. Hence the tuned amplifier selects and amplifies the desired frequency signal.	4+3Exp	7	7
III. 7	 	4+3Exp	7	7

<table>
<tr><td></td><td>When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across C1 which are applied to the base emitter junction and appear in the amplified form in the collector circuit and supply losses to the tank circuit.
If terminal 1 is at positive potential with respect to terminal 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at that instant because terminal 3 is grounded. Therefore, points 1 and 2 are out of phase by 180°.
As the CE configured transistor provides 180o phase shift, it makes 360° phase shift between the input and output voltages. Hence, feedback is properly phased to produce continuous Undamped oscillations. When the loop gain |βA| of the amplifier is greater than one, oscillations are sustained in the circuit.</td><td></td><td></td><td></td></tr>
<tr><td>III. 8</td><td>

Voltage Series


Voltage Shunt</td><td>3.5+3.5</td><td>7</td><td>7</td></tr>
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<table>
<tr>
<td>III. 9</td>
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<table>
<tr><th>Parameters</th><th>Positive Feedback</th><th>Negative Feedback</th></tr>
<tr><td>Input and output noise voltage</td><td>Increases due to feedback</td><td>Decreases due to feedback</td></tr>
<tr><td>Feedback signal and input signal phase condition</td><td>In phase</td><td>Out of phase</td></tr>
<tr><td>Gain</td><td>Increases</td><td>Decreases</td></tr>
<tr><td>Stability</td><td>Poor</td><td>Good</td></tr>
<tr><td>Applications</td><td>Oscillators</td><td>Amplifiers</td></tr>
</table>
</td>
<td>7</td>
<td>7</td>
<td>7</td>
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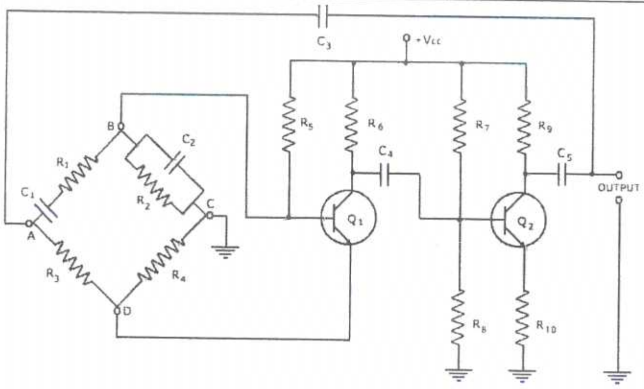
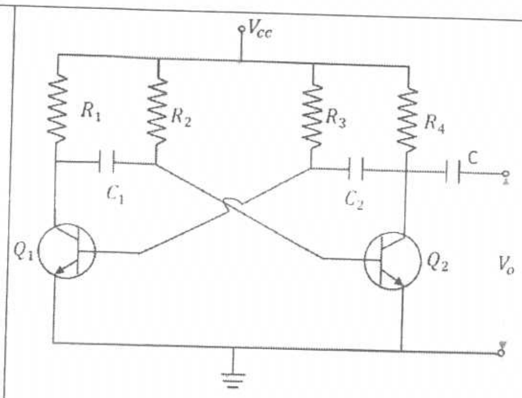
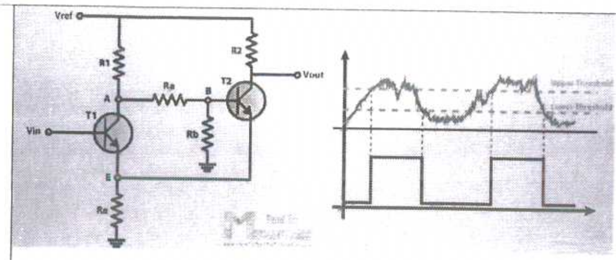
<tr>
<td>III. 10</td>
<td>


$f = \frac{1}{2\pi CR}$

. The base current is applied to the collector terminal of the first transistor and the phase shift is about the 180°. The output of the first transistor is given to the base terminal of the second transistor Q2 with the help of the capacitor C4.

The output signal is connected to the phase with the help of the first transistor to the base terminal. The input point of the bridge circuit is from the point A to point C the feedback of this circuit is the output signal at the second transistor. The feedback signal is given to the resistor R4 which gives the negative feedback. In this same way the feedback signal is given to the base bias resistor R4 and it produces the positive feedback signal.
</td>
<td>4+3Exp</td>
<td>7</td>
<td>7</td>
</tr>
</table>

III. 11	 When Vcc is applied, one of the two transistors say Q1 has its collector current increase and thus conducts. The collector of Q1 is applied to the base of Q2 through C1. This connection lets the increased negative voltage at the collector of Q1 to get applied at the base of Q2 and its collector current decreases. This continuous action makes the collector current of Q2 to decrease further. This current when applied to the base of Q1 makes it more negative and with the cumulative actions Q1 gets into saturation and Q2 to cut off. Thus the output voltage of Q1 will be VCE (sat) and Q2 will be equal to VCC. The capacitor C1 charges through R1 and when the voltage across C1 reaches 0.7v, this is enough to turn the transistor Q2 to saturation. As this voltage is applied to the base of Q2, it gets into saturation, decreasing its collector current. This reduction of voltage at point B is applied to the base of transistor Q1 through C2 which makes the Q1 reverse bias. A series of these actions turn the transistor Q1 to cut off and transistor Q2 to saturation. Now point A has the potential VCC. The capacitor C2 charges through R2. The voltage across this capacitor C2 when gets to 0.7v, turns on the transistor Q1 to saturation.	4+3Exp	7	7

III. 12	 Schmitt trigger can be defined as it is a regenerative comparator. It employs positive feedback and converts sinusoidal input into a square wave output. The output of Schmitt Trigger swings at upper and lower threshold voltages, which are the reference voltages of the input waveform. It is a bi-stable circuit in which the output swings between two steady-state voltage levels (High and Low) when the input reaches certain designed threshold voltage levels. UTP stands for upper trigger point, whereas LTP stands for the lower trigger point. Hysteresis can be defined as when the input is higher than a certain chosen threshold (UTP), the output is low. When the input is below a threshold (LTP), the output is high; when the input is between the two, the output retains its current value. This dual threshold action is called hysteresis.	4+3Exp	7	7