മീറ്റിംഗ് മിനിട്സ് (24/01/24)

സമയം.11.00

3044(21)

വേദി: ജോയിൻറ് കൺട്രോളറുടെ ചേമ്പർ

പങ്കെടുത്തവർ

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8 ശ്രീ.ഷറഫുദീൻ.എ,സിസ്റ്റം അനലിസ്റ്റ്

1.Decision taken by the JCTE office on 23/01/24, based on the complaints received from students from various Polytechnic colleges in connection with the Diploma Examination November 2023 and the recommendations of expert committee from different departments.

OUT OF SYLLABUS QUESTION GUIDELINES

R.21	5043D	Part.B Question -8	3 mark
		Part C Question V	7 mark
R.21	3042	Part.C Question No.IV	4 mark
		Part C Question VII	2 mark
		Part C Question X	2 mark
R.21	3051	Part.C Question VI	7 mark
R.21	5021	Part B Question 9	3 mark

R.21	3055	Question III	25 marks
R.21	3044	Part.B Question 8	3 mark
R.21	3033	Part C Question 13	7 mark
R.15	5182	part B question II	Students who have drawn the site plan in the 1:200, 1:400 and 1:800 scales can be considered eligible for getting the marks they deserve .

The above mentioned questions are out of syllabus as recommended by the expert committee. Hence, following guidelines shall be used to calculate the mark/grade of the students who had tried to attend the above specific questions.

a) Calculate the percentage of marks obtained by the student considering the total marks excluding the marks of out of syllabus questions.

b) Then, the proportionate marks of out of syllabus questions shall be calculated based on the above obtained percentage.

c) Marks obtained in the above cases shall be added to get actual marks admissible to the student.

2. 25.01.2024 -ന് ആരംഭിക്കുന്ന ഡിപ്ലോമ പരീക്ഷ മൂല്യനിർണ്ണ ക്യാമ്പിൻറ പ്രവർത്തനം സംബന്ധിച്ച് കമ്മിറ്റി ചർച്ച ചെയ്യുകയും ക്യാമ്പ് ആഫീസർമാർക്ക് നിർദ്ദേശങ്ങൾ നൽകുന്നതിന് സർക്കുലർ അയയ്ക്കുവാൻ D2 സെക്ഷൻ സീനിയർ ക്ലർക്ക് ശ്രീ.അനൂപിനെ ചുമതലപ്പെടുത്തുകയും ചെയ്തു.

3. ക്യാമ്പുകളുടെ സുഗമമായ നടത്തിപ്പിനായി വിവിധ മൂല്യനിർണ്ണയ ക്യാമ്പുകൾ സന്ദർശിക്കുവാൻ JCTE, DCTE, ACTE, TECHNICAL OFFICER എന്നിവരെ നിയോഗിക്കുവാൻ തീരുമാനിച്ചു.

4.SBTE സോഫ്റ്റവെയറിൻറ സെക്യൂരിറ്റി ആഡിറ്റ് ചെയ്യുന്നതിന് JCTE ആഫീസിൽ ലഭിച്ചിട്ടുള്ള പ്രപ്പോസലുകൾ പരിശോധിച്ച് തീരുമാനം എടുക്കുന്നതിന് NIC യ്ക്ക് കത്ത് അയ്ക്കുവാൻ തീരുമാനിച്ചു.

CONTROLLER OF TECHNICAL EXAMINATIONS * TRIVANDRUM * Govt. Of Kerala Dept. Of Techl Edn.

ജോയിൻറ് കൺട്രോളർ

200 16/11/23

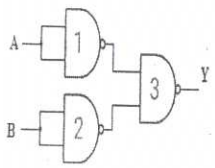
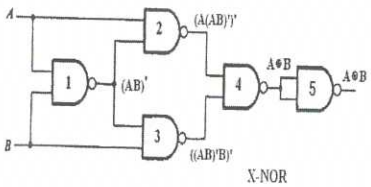
11

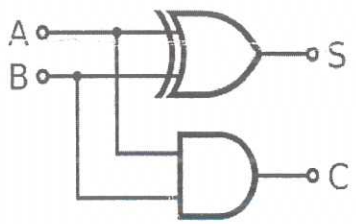
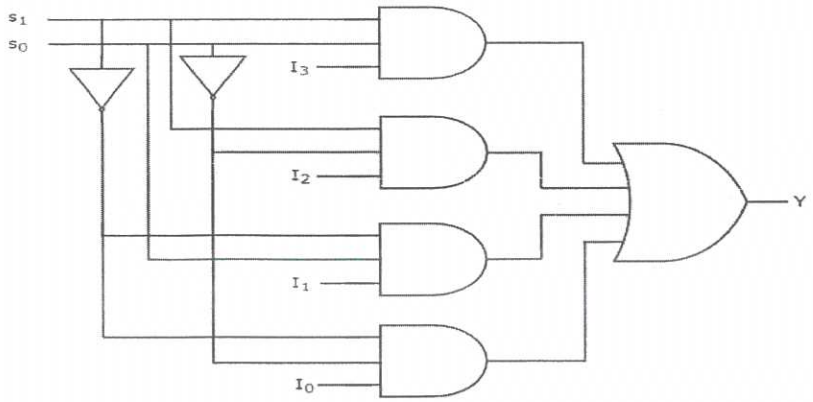
Nov. 23

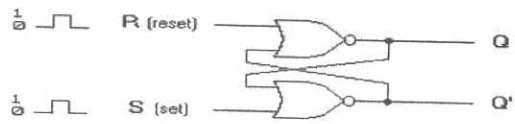
Scoring Indicators

COURSE NAME : DIGITAL ELECTRONICS

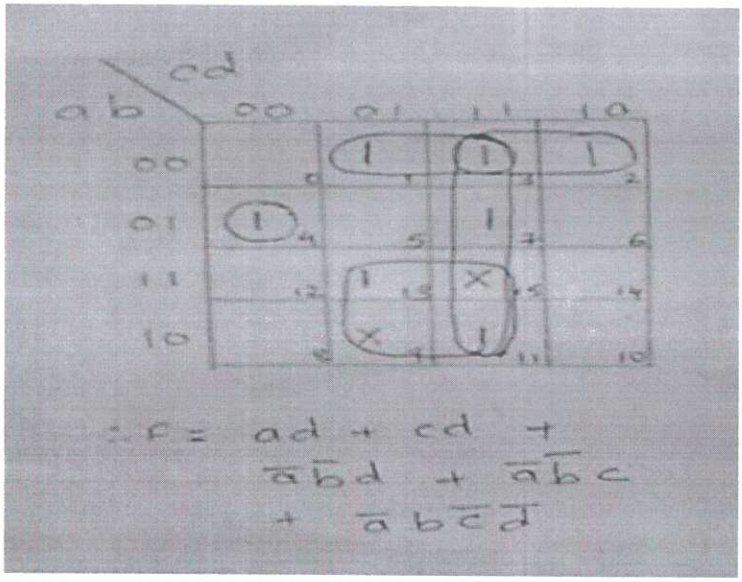
COURSE CODE : TED(21)3044 QID : 2110220235

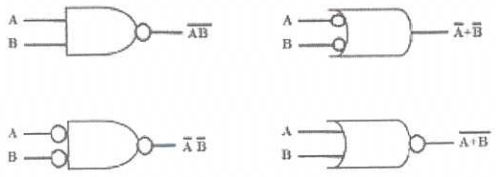
Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			**9**
I.1	c) Either 0 or 1		1	
I.2	A) MSB		1	
I.3	Emitter-coupled logic		1	
I.4	3		1	
I.5	T flip-flop		1	
I.6	Parallel in/Parallel out		1	
I.7	D Flip Flop		1	
I.8	5		1	
I.9	High		1	
	PART B			**24**
II.1	237.4_{16}		3	
II.2	1100012 (Hind-Find 2's compliment of 1011112,then add with 1100000_2 - ignore the carry)		3	
II.3	(c) OR gate: $Y = A + B$  NAND Gates as EX-NOR Gate  X-NOR	1.5 1.5	3	
II.4	TTL : *TTL stands for Transistor-Transistor Logic. The name is derived from the use of two Bipolar Junction Transistors.	1x3	3	

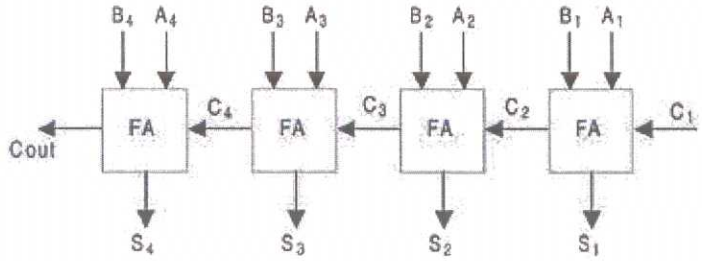
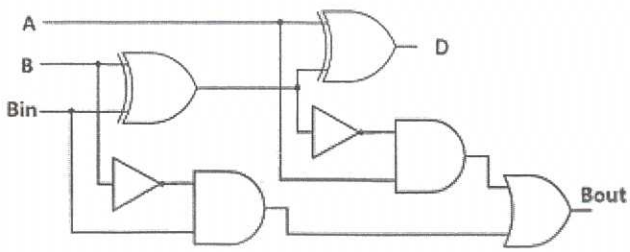
	*The density of logic gates is less in TTL as compared to CMOS. *TTL circuits consumes more power compared to CMOS circuits at rest. CMOS: *CMOS stands for Complementary Metal Oxide Semiconductor. * The primary advantage of CMOS chips to TTL chips is in the greater density of logic gates within the same material. *CMOS circuits comsumes less power at rest. *CMOS technology and its circuit are more economical. *CMOS circuits have better noise immunity than TTL circuits.			
II.5	 **Inputs** / **Outputs** A | B | Sum | Carry 0 | 0 | 0 | 0 0 | 1 | 1 | 0 1 | 0 | 1 | 0 1 | 1 | 0 | 1	1.5 1.5	3	
II.6			3	

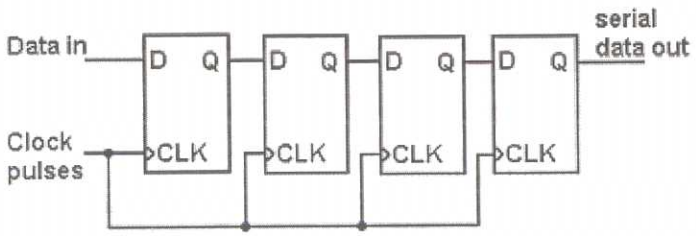
II.7	Combinational Circuit *In this output depends only upon present input. *Speed is fast. *It is designed easy. *There is no feedback between input and output. Sequential Circuit *In this output depends upon present as well as past input. *Speed is slow. *Its design is tough as compared to combinational circuits. *There exists a feedback path between input and output.	1x3	3	
II.8	It has two inputs, one is called "SET" which will set the device (output = 1) and is labelled S and another is known as "RESET" which will reset the device (output = 0) labelled as R. The RS stands for SET/RESET.The flip-flop is reset back to its original state with the help of RESET input and the output is Q that will be either at logic level "1" or logic"0". It depends upon the set/reset condition of the flip-flop. Flip flop word means that it can be "FLIPPED" into one logic state or "FLOPPED" back into another.  (a) Logic diagram S R | Q Q' 1 0 | 1 0 0 0 | 1 0 (after S=1, R=0) 0 1 | 0 1 0 0 | 0 1 (after S=0, R=1) 1 1 | 0 0 (b) Truth table Basic flip-flop circuit with NOR gates	Dia-1 TT-1 Exp-1	3	

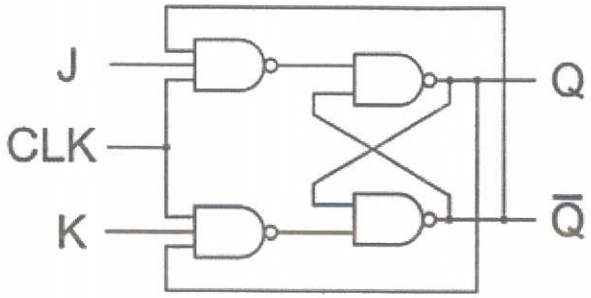
II.9	Synchronous Counter *In synchronous counter, all flip flops are triggered with same clock simultaneously. *Synchronous Counter is faster than asynchronous counter in operation. *In synchronous counter, propagation delay is less. *Synchronous Counter will operate in any desired count sequence. Asynchronous Counter *In asynchronous counter, different flip flops are triggered with different clock ,not simultaneously. *Asynchronous Counter isslower than synchronous counter in operation. *In Asynchronous counter, propagation delay is more. *Asynchronous Counter will operate in fixed count sequence.	1x3	3	
II.10	Flash memory, also known as flash storage, is a type of nonvolatile memory that erases data in units called blocks and rewrites data at the byte level. Flash memory is widely used for storage and data transfer in consumer devices, enterprise systems and industrial applications. Cache memory is an extremely fast memory type that acts as a buffer between RAM and the CPU. It holds frequently requested data and instructions so that they are immediately available to the CPU when needed. Cache memory is used to reduce the average time to access data from the Main memory.		3	

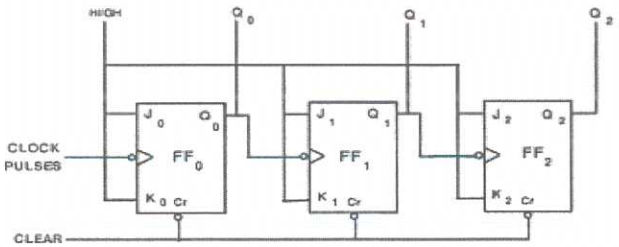
	PART C			42
III.1		K-map-4 equ-3	7	
III.2	(i) 21.625_{10} (ii) 1000110100012 (iii) 1010001101012 (iv) 1011001.1012	2X3 1X 1	7	
III.3	The excess-3 code is also treated as XS-3 code. The excess-3 code is a non-weighted and self-complementary BCD code used to represent the decimal numbers. This code has a biased representation.We can easily get an excess-3 code of a decimal number by simply adding 3 to each decimal digit. And then we write the 4-bit binary number for each digit of the decimal number. BCD-Binary-coded decimal is a system of writing numerals that assigns a four-digit binary code to each digit 0 through 9 in a decimal (base 10) number. Simply put, binary-coded decimal is a way to convert decimal numbers into their binary equivalents. However, binary-coded decimal is not the same as simple binary representation.	3.5x2	7	

III.4	 | A | B | A.B | $\overline{A.B}$ | $\overline{A}$ | $\overline{B}$ | $\overline{A}+\overline{B}$ | |---|---|---|---|---|---|---| | 0 | 0 | 0 | 1 | 1 | 1 | 1 | | 0 | 1 | 0 | 1 | 1 | 0 | 1 | | 1 | 0 | 0 | 1 | 0 | 1 | 1 | | 1 | 1 | 1 | 0 | 0 | 0 | 0 |	3.5x2	7	
III.5	(i) Fan-in is the number of inputs that a logic gate can take, fan-out implies the maximum number of logic gates that can be drive by the output of a logic gate of the same family. (ii) Propagation delay, or gate delay, is the essential performance metric, and it is defined as the length of time starting from when the input to a logic gate becomes stable and valid, to the time that the output of that logic gate is stable and valid. (iii) Power dissipation is the supplied power required to operate the desired logic function. This parameter does not include the power delivered from another gate. (iv) The noise margin, NMH = |VOH min – VIH min|, for logical high is the range of tolerance for which a logical high signal can still be received correctly.		7	
III.6	Two binary numbers each of n bits can be added by means of a full adder circuit. two 4-bit binary numbers B4 B3 B2 B1 and A4 A3 A2 A1 are to be added with a carry input C 1. This can be done by cascading four full adder circuit.	Dia-3 TT-2 Exp-2	7	

	The least significant bits A1, B1, and C1 are added to the produce sum output S 1 and carry output C 2. Carry output C2 is then added to the next significant bits A2 and B2 producing sum output S 2 and carry output C 3. C 3 is then added to A 3 and B 3 and so on. Thus finally producing the four-bit sum output S 4S 3S 2S 1and final carry output Cout. Such type of four-bit binary adder is commercially available in an IC package.  			
III.7	The full subtractor is used to subtract three 1-bit numbers A, B, and C, which are minuend, subtrahend, and borrow, respectively. The full subtractor has three input states and two output states i.e., diff and borrow.  	Dia-3 TT-2 Exp- 2	7	

	<table><tr><th colspan="3">Inputs</th><th colspan="2">Outputs</th></tr><tr><th>A</th><th>B</th><th>$Borrow_{in}$</th><th>Diff</th><th>Borrow</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>			
III.8			7	
III.9	In SR flip flop, both the inputs 'S' and 'R' are replaced by two inputs J and K. It means the J and K input equates to S and R, respectively. The two 2-input AND gates are replaced by two 3-input NAND gates. The third input of each gate is connected to the outputs at Q and Q'. The cross-coupling of the SR flip-flop permits the previous invalid condition of (S = "1", R = "1") to be used to produce the "toggle action" as the two inputs are now interlocked. If the circuit is "set", the J input is interrupted from the "0" position of Q' through the lower NAND gate. If the circuit is "RESET", K input is interrupted from 0 positions of Q through the upper NAND gate. Since Q and Q' are always different, we can use them to control the input. When both inputs 'J' and 'K' are set to 1, the JK toggles the flip flop as per the given truth table.	Dia-3 TT-2 Exp-2	7	

	 Same as for SR Latch / Toggle action — Clock: Clk; Input: J, K; Output: Q, Q'; Description X 0 0 1 0 — Memory no change X 0 0 0 1 ↓ 0 1 1 0 — Reset Q>>0 X 0 1 0 1 ↓ 1 0 0 1 — Set Q>>1 X 1 0 1 0 ↓ 1 1 0 1 — Toggle ↓ 1 1 1 0			
III.10	A register can be defined as when a set of FFs can be connected within the series, the definition of the shift register is when the stored data can be moved in the registers. It is a sequential circuit, mainly used to store the data, & moves it to the output on each CLK (clock) cycle. Types of shift registers are 1.Serial in Serial out (SISO) Shift Register: The Serial in Serial out (SISO) logic circuit is shown above. This circuit can be built with four D-Flip Flops in serially. Once these Flip flops connected with each other then the equal CLK signal is given to every flip flop. 2.Serial in parallel out (SIPO) Shift Register :This shift register allows serial input and generates a parallel output, so this is known as serial in parallel out (SIPO) shift register. 3.Parallel in Serial out (PISO) Shift Register:This shift register allows parallel input and generates a serial output, so this is known as Parallel in Serial out (PISO) Shift Register	Defi.-2 Types 2 Exp-3	7	

	4.Parallel in Parallel out (PIPO) Shift Register :The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register.			
III.11	<table><tr><th colspan="4">COUNT-UP Mode</th></tr><tr><th>States</th><th>Q_C</th><th>Q_B</th><th>Q_A</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>2</td><td>0</td><td>1</td><td>0</td></tr><tr><td>3</td><td>0</td><td>1</td><td>1</td></tr><tr><td>4</td><td>1</td><td>0</td><td>0</td></tr><tr><td>5</td><td>1</td><td>0</td><td>1</td></tr><tr><td>6</td><td>1</td><td>1</td><td>0</td></tr><tr><td>7</td><td>1</td><td>1</td><td>1</td></tr></table> In the 3-bit ripple counter, three flip-flops are used in the circuit. As here 'n' value is three, the counter can count up to $2^3 = 8$ values .i.e. 000,001,010,011,100,101,110,111. 	Dia-5 Exp-2	7	
III.12	An Asynchronous counter can have 2n-1 possible counting states e.g. MOD-16 for a 4-bit counter, (0-15) making it ideal for use in Frequency Division applications. But it is also possible to use the basic asynchronous counter configuration to construct special counters with counting states less than their maximum output number. For example, modulo or MOD counters. This is achieved by forcing the counter to reset itself to zero at a pre-determined value producing a type of asynchronous counter that has truncated sequences	Dia-5 Exp-2	7	

QD	QC	QB	QA	Reset logic
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0