42
8/11/23

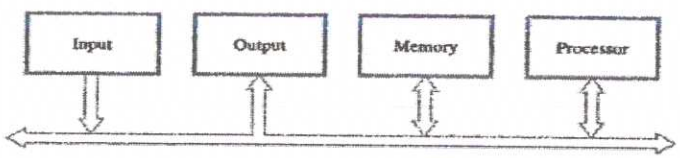
13 Nov-23

SET 2

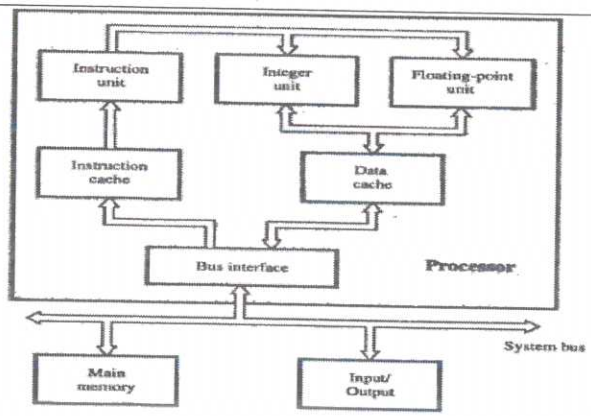
Scoring Indicators

COURSE NAME: COMPUTER ORGANIZATION
COURSE CODE:3131

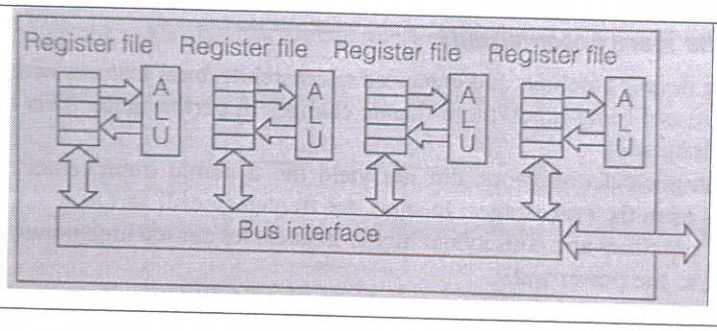
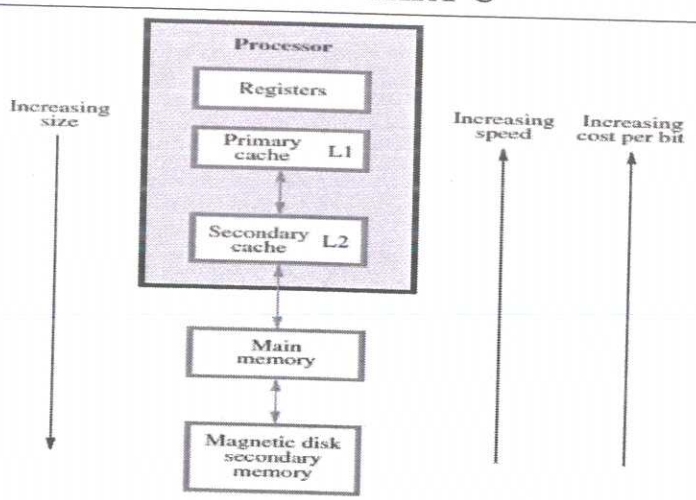
QID: 2110220197

Q. No.	Scoring Indicators	Split Score	Sub Total	Total Score
	PART A			**9**
I. 1	Input unit, Output unit, Memory unit, Arithmetic & Logic unit and Control unit.	1	1	1
I. 2	Seek Time is defined as the time required by the read/write head to move from one track to another.	1	1	1
I. 3	Raster scan is a technique used to construct alphanumeric text and graphical pictures. In raster scan, the electron beam is swept across the screen, one row at a time from top to bottom and the beam intensity is turned on and off to create a pattern of illuminated spots.	1	1	1
I. 4	Universal Serial Bus	1	1	1
I. 5	Fetch Phase and Execution Phase	0.5x2=1	1	1
I. 6	• Program Counter (PC) • Memory Address Register (MAR) • Memory Data Register (MDR) • Instruction register (IR)	0.5*2 =1 (Any 2)	1	1
I. 7	A program counter is a register in the CPU containing the address of the next instruction to be executed.	1	1	1
I. 8	8 Bits	1	1	1
I. 9	**SI** – Source Index and **DI** – Destination index register	0.5x2=1	1	1
	PART B			**24**
II. 01	A group of lines that serves as a connecting path for several devices is called a bus. 	Def. Bus 1		

	In addition to the lines that carry the data, the bus must have lines for address and control purposes. Since all units are connected to a single bus, only two units can actively use the bus at any given time. Bus control lines are used to arbitrate multiple requests for use of bus. The main advantage of single bus structure is its low cost and flexibility for attaching I/O devices.	0.5x4=2 Any 4 points	3	3
II. 02	***STATIC MEMORIES*** • Capable of retaining their state as long as power is applied. • SRAMs are volatile memories. • Very low power consumption. • Static RAMs can be accessed very quickly. ***DYNAMIC RAMS*** • Information is stored in a cell is in the form of a charge on a capacitor. • Contents must be periodically refreshed to retain the information stored. • Less expensive and higher density RAMs can be implemented with simpler cells.	1.5x2=3 Any 3 Points from each	3	3
II. 03	The program controlled I/O is the simplest type of I/O technique for the exchanges of data or any types of communication between the processor and the I/O devices. If the processor issues a command to the I/O module, then it must wait until the I/O operation is completed. Ie Program-Controlled I/O repeatedly checks (polls) the status flag of the device to achieve the required synchronization between the processor and I/O device. **Disadvantage - Busy waiting.**	3	3	3

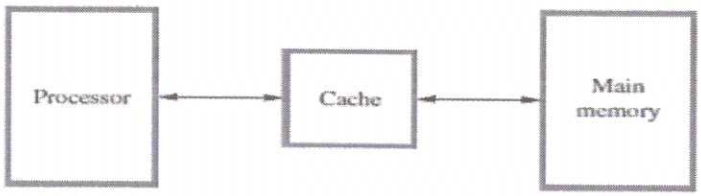
II. 04		3	3	3
II. 05	Two control signals are used to place the contents of the register on the bus or to load the data on the bus into the register 1. Enable the output of register R1 by setting R1out to 1. This places the contents of R1 on the processor bus. 2. Enable the input of register R2 by setting R2in to 1.This loads data from processor bus to register R2.	1.5x2=3	3	3
II. 06	To execute an instruction, the processor has to perform the following steps: 1. **Fetch** the contents of the memory location (instruction to be executed) pointed to by the PC and loaded into the IR. ***IR←[[PC]]*** 2. Increment the PC to point to the next instruction or operand. ***PC←[PC] + 4*** 3. Read the operands and load them into a processor register 4. Carry out the operation specified by the instruction in the IR. 5. Store data from a processor register into a given memory location. For Example, Consider the instruction Add (R3),R1. Executing this instruction requires the following actions: 1) Fetch the instruction. 2) Fetch the first operand. 3) Perform the addition.	3	3	3

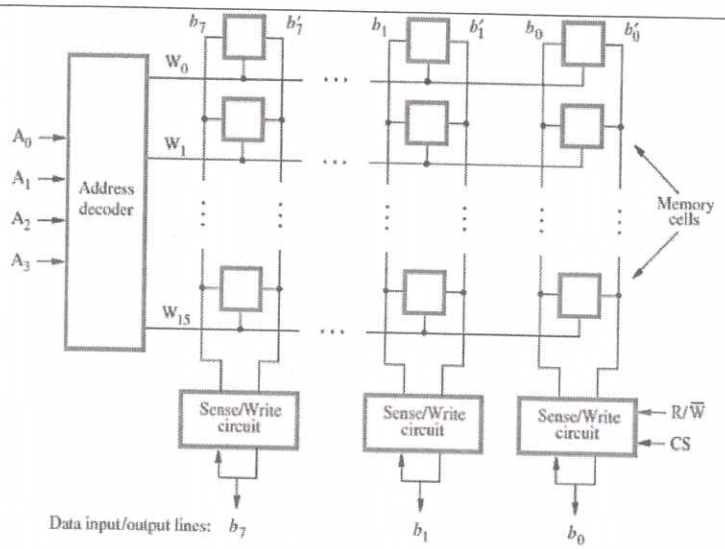
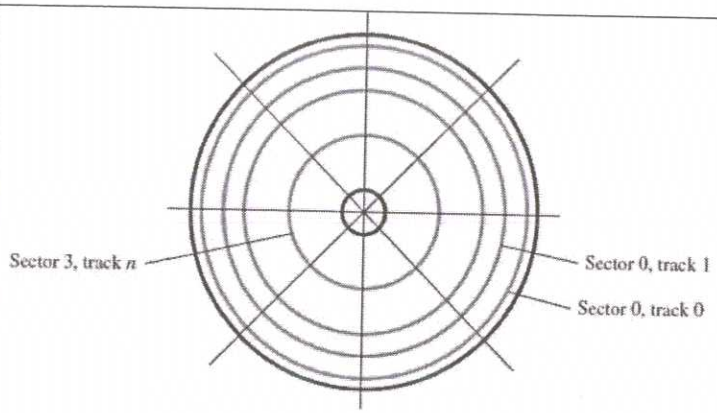
	4) Load the result into R1.			
II. 07	• **Control Word** (CW) is a word whose individual bits represent various control-signals such as Add, PCin etc. • A sequence of CWs corresponding to control-sequence of a machine instruction constitutes the **micro routine.** • The micro routines for all instructions in the instruction-set of a computer are stored in a special memory called the **Control Store** (CS). Control-unit generates control-signals for any instruction by sequentially reading CWs of corresponding micro routine from control store.	1x3=3	3	3
II. 08	The 8086 architecture uses the concept of segmented memory, the 1-megabyte memory is divided into 16 logical segments of size 64 Kbytes of memory. • **Code segment register (CS):** is used for addressing code segment where the executable program is stored. • **Data segment register (DS):** points to the data segment of the memory where the data is stored. • **Extra Segment Register (ES):** which is another data segment in the memory. • **Stack Segment Register (SS):** is used for addressing stack segment of the memory used to store stack data.	0.75x4=3	3	3
II. 09	A multi-core processor is an integrated circuit with two or more processor cores attached to it for faster simultaneous processing of several tasks, reduced power consumption, and for greater performance. The performance enhancement is obtained using parallelization.	3	3	3

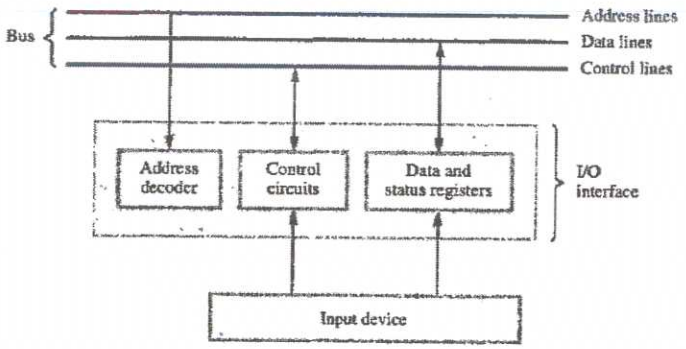
<table>
<tr><td></td><td> 
</td><td></td><td></td><td></td></tr>
<tr><td>II. 10</td><td>• Pentium has superscalar pipelined architecture which means, CPU can execute two (or more) instructions per cycle.
• Execution unit with two integer pipeline (U-pipe and V-pipe).
• Pipelined floating point unit.
• Separate 8K code cache and 8K data cache
• Branch prediction logic
• 64 bit data bus and 32 bit address bus etc.</td><td>1x3=3 (Expln. of any 3)</td><td>3</td><td>3</td></tr>
<tr><td colspan="4">PART C</td><td>42</td></tr>
<tr><td>III. 01</td><td> 

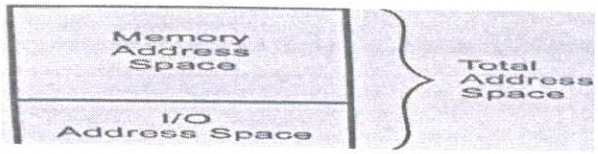
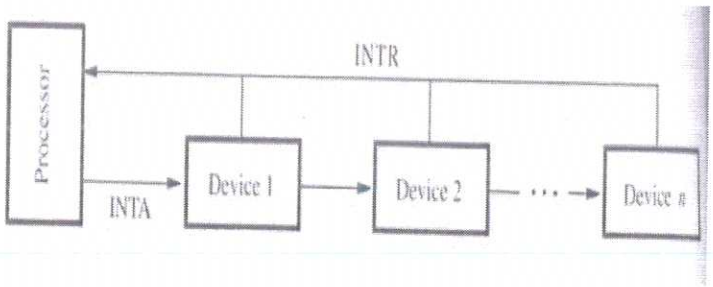
<table>
<tr><th>Memory</th><th>Speed</th><th>Size</th><th>Cost</th></tr>
<tr><td>Registers</td><td>Very high</td><td>Lower</td><td>Very Lower</td></tr>
<tr><td>Primary cache</td><td>High</td><td>Lower</td><td>Low</td></tr>
<tr><td>Secondary cache</td><td>Low</td><td>Low</td><td>Low</td></tr>
<tr><td>Main memory</td><td>Lower than Seconadry cache</td><td>High</td><td>High</td></tr>
<tr><td>Secondary Memory</td><td>Very low</td><td>Very High</td><td>Very High</td></tr>
</table></td><td>Figure 2.5

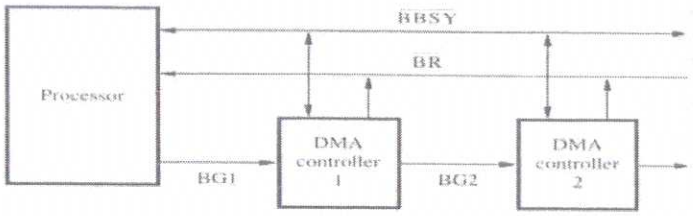
Compare Speed Size Cost 1.5x3 =4.5</td><td>7</td><td>7</td></tr>
</table>

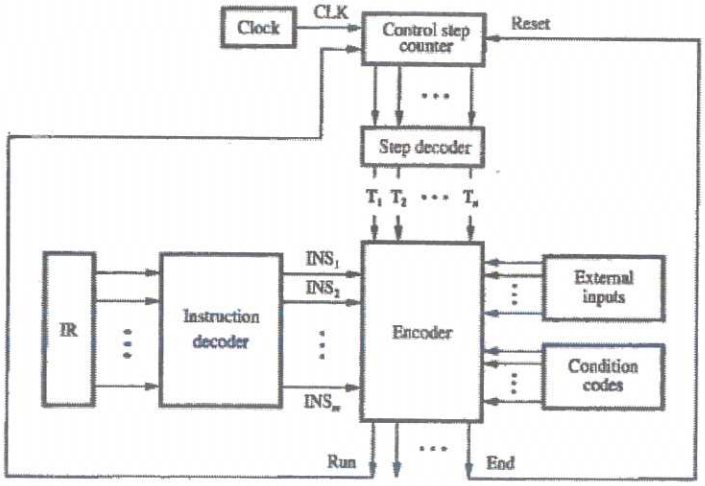
III. 02	The cache is a small and very fast memory, interposed between the processor and the main memory. Its purpose is to make the main memory much faster than it actually is. The effectiveness is based on the **property locality of reference**. The point is that many instructions in localized areas of the program are executed repeatedly during some time period. This behaviour manifests itself in two ways: **temporal and spatial**. The first means that a recently executed instruction is likely to be executed again very soon. The spatial aspect means that instructions close to a recently executed instruction are also likely to be executed soon.  ***Cache Hits :*** The processor issues Read and Write requests using addresses that refer to locations in the memory. The cache control circuitry determines whether the requested word is currently exists in the cache or not. If it does, the Read or Write operation is performed on the appropriate cache location. ***Cache Misses:*** If the word is not available in the cache constitutes a **cache miss**. Then it will copy block of words containing the requested word from the main memory into the cache and then transfer the requested word to the processor. ***Cache Replacement:*** When the cache is full and a memory word which is not in the cache is referenced, the cache control Hardware must decide which block should be removed to create the space for the new block.	Figure & Expln. 4 1x3=3	7	7

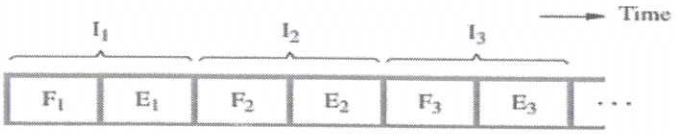
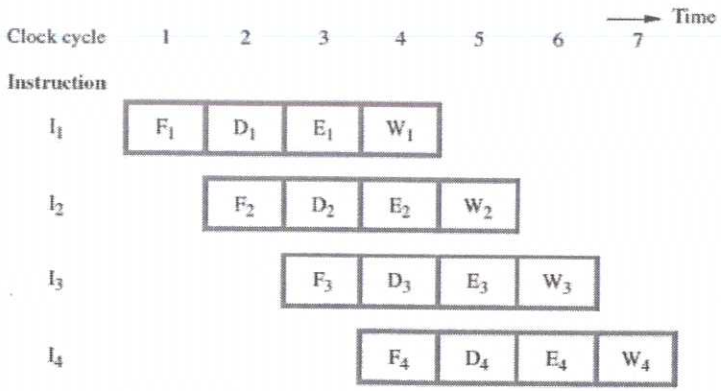
III. 03	 A cell is capable of storing one bit of information. Memory chips are organized as array of cells. Each row of cells constitutes a memory word, and all cells in a row are connected to a common word line, which is driven by the address decoder on the chip. The cells in each column are connected to a Sense/Write circuit by two bit lines, and the Sense/Write circuits are connected to the data input/output lines of the chip. During a **Read operation**, these circuits' sense, or read, the information stored in the cells selected by a word line and place this information on the output data lines. During a **Write operation**, the Sense/Write circuits receive input data and store them in the cells of the selected word.	Defn. 1 Figure 4 Expln. 2	7	7
III. 04	 The storage medium in a magnetic-disk system consists of one or more disk platters mounted on a common spindle. A thin magnetic film is deposited on each platter, usually on	3 Figure		

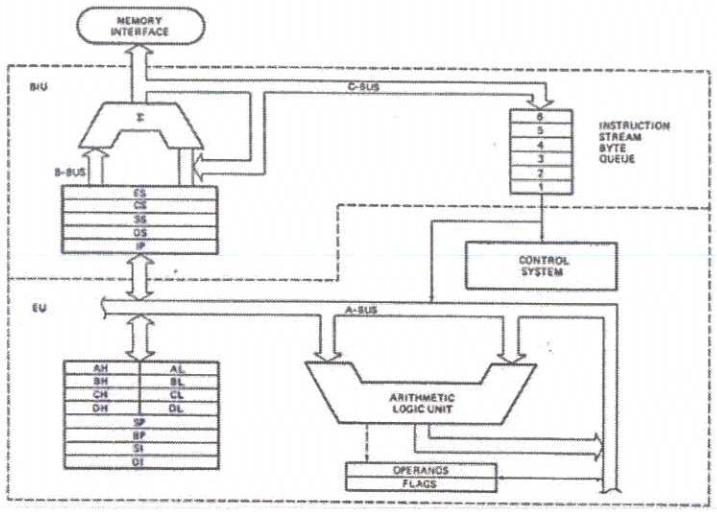
	both sides. The assembly is placed in a drive that causes it to rotate at a constant speed. The magnetized surfaces move in close proximity to read/write heads for reading and writing data. **Organization of Data on a Disk** : Each surface is divided into concentric **tracks,** and each track is divided into **sectors**. Each **sector may contain 512 or more bytes.** There is a small inter-sector gap that enables the disk control circuitry to distinguish easily between two consecutive sectors. The set of corresponding tracks on all surfaces of a stack of disks forms a logical **cylinder**. ***Accessing of Data on a Disk*** *:* Data bits are stored serially on each track. Data are accessed by specifying the **surface number, the Track number, and the sector number**. Read and Write operations always start at sector boundaries. All tracks of a cylinder can be accessed without moving the read/write heads.	2 2	7	7
III. 05	Interfacing circuitry of I/O devices is shown below. The address decoder enables the device to recognize its address when this address appears in the address line. The data register holds the data being transferred to or from the processor. The status register contains status information of the operation.  ***Memory Mapped I/O*** In this technique, I/O devices and Memory share the same address space. The total memory address space is partitioned and part of this space is devoted to I/O addressing. So machine instruction that can access memory can also be used	Expln 2 Figure 2 3	7	7

	to transfer data to or from an I/O device.  			
III. 06	A number of devices which are connected to the processor through a common interrupt line INTR and several devices may request interrupts at exactly the same time. Then, it must be possible to break the tie and select one of the requests for service, after that next ones can be serviced. **Device identification : Polling** - When a device raises an interrupt request, it sets IRQ bit to 1 in status register. The simplest way to identify the interrupting device is to poll all I/O devices in the system. The first device encountered with its IRQ bit set to 1 is the device that should be serviced. This scheme is very easy to implement, but the main disadvantage is the time spent interrogating the IRQ bits of devices that may not be requesting any service.  **Vectored Interrupts:** Here the device requesting an interrupt can be identified by the special code sent by the device to the processor through the interconnection network. The processor's circuits determine the memory address (interrupt vectors, stored interrupt-vector table) of the required interrupt-service routine from this code and immediately start executing the corresponding interrupt-service routine which may be located anywhere in the memory. When an interrupt occurs, the information provided by the	Any one Method 7	7	7

	device is used as a pointer into the interrupt-vector table, and the address in the corresponding interrupt vector is automatically loaded into the program counter.			
III. 07	DMA is an approach to transfer blocks of data directly between the main memory and I/O devices without continuous intervention by the processor. The unit that controls DMA transfers is referred to as a DMA controller. When two or more devices attempts to use the bus, the bus arbiter circuit will resolve the conflict.  **Cycle Stealing and Burst Modes:** DMA controllers can operate in a cycle stealing mode in which they take over the bus for each byte of data to be transferred and then return control to the CPU. In burst mode a block of data is transferred before returning bus control to the CPU.	DMA 3 2x2=4	7	7
III. 08	The acronym SCSI stands for **Small Computer System Interface**. The SCSI bus is used to connect a variety of devices to a computer. • SCSI is widely used in workstations, servers, and mainframes, particularly well-suited for disk drives. • SCSI helps transfer data between computers and laptops and peripheral devices. • SCSI has its own controller for troubleshooting and less dependency on other devices for proper performance. • Data exchanges occur through a single cable, thus streamlining the connection. • SCSI equipment is highly accessible, making it easy to replace and upgrade older SCSI components. • Current SCSI technologies can transfer up to 640 megabytes per second.	1 1.5x4=6 Any 4 features	7	7

	• The advantage of SCSI is that you can add a scanner and several other drives such as CD-Rs, DVD-RAM, Zip drives as well as hard drives, to one SCSI cable chain. • SCSI is useful in network servers, where several hard drives can be easily set up as a RAID configuration.			
III. 09	To execute instructions, the processor must have to generate control signals.  Control-signals are generated by using logic circuits such as gates, flip-flops, decoders etc. Decoder / Encoder generates required control-outputs depending on state of all its inputs. Instruction decoder decodes the instruction loaded in the IR, based on that one of the output-lines INS1 through INSm is set to 1, and all other lines are set to 0.Step-Decoder provides a separate signal line for each step in the control sequence. Encoder gets the input from instruction decoder, step decoder, external inputs and condition codes. It uses all these inputs to generate individual control-signals. After execution of each instruction, end signal is generated which resets step counter. Sequence of operations carried out by this machine is determined by wiring of logic circuits, hence the name "hardwired". ***Advantage:*** **Can operate at high speed.**	3 Figure 4 Expln	7	7

III. 10	Pipelining is a process of executing instructions concurrently. Let Fi and Ei refer to the fetch and execute steps for instruction Ii. Execution of a program consists of a sequence of fetch and execute steps, as shown below,  (a) Sequential execution This fetching and executing phases can be operated in an overlapped way. That is when the execution unit is executing the current instruction, the fetch unit can fetch the next instruction. This is basic idea of instruction pipelining. The processing of an instruction can be divided four steps, • **F- Fetch**: read the instruction from the memory. • **D- Decode**: decode the instruction and fetch the source operand(s). • **E- Execute**: perform the operation specified by the instruction. • **W- Write**: store the result in the destination location.  ***Pipeline Performance*** The performance increase is proportional to the number of pipeline stages. In this example (Two stage), in each clock cycle, one instruction is completed execution, which means	Defn. 2 5	7	7

	the rate of instruction processing is four times that of sequential operation.			
III. 11	There are 6 different flags in 8086 which are set or reset based on the result of 8-bit or 16-bit operations. 1. **Sign Flag (S)** - if the MSB is 1, then it indicates that the number is negative. And this flag is set to 1. 2. **Zero Flag (Z)** - If the result is zero, then Z flag will be set. 3. **Auxiliary Cary Flag (AC)** – if carry after the lower half and sends it to upper half, the AC will be 1. 4. **Parity Flag (P)** – it will be set to 1, when result has even number of 1s. 5. **Carry Flag (CY) – if the** operation is generating a carry, this flag is set to 1. 6. **Overflow Flag (O) - it** is set to 1 when the result of a signed operation is too large to fit.	List the names 1 1x6=6 Expln.	7	7
III. 12		7	7	7
