



No: D1/288/2024 CTE

Office of the  
Controller of Technical Examinations  
Kaimanam, Thiruvananthapuram - 695040  
email: jctexam@gmail.com  
Telephone No.0471-2775401  
Dated: 15-06-2024

**CIRCULAR**

Sub:- Technical Education – Examination Wing - April 2024 Diploma Examination -  
Out of syllabus questions - Decision taken - Regarding.

Ref :- Complaints received from students of various colleges.

Camp Officers of all the Centralised Valuation Camps of April 2024 Diploma Examination are informed that, the following guidelines should be followed for distribution of marks in connection with out of syllabus questions, of below mentioned codes, in the case of students who tried to attend the said questions.

- |              |                      |        |
|--------------|----------------------|--------|
| 1) R21 4041  | Part C<br>Qn No: III | 7 Mark |
| 2) R 21 4021 | Part A<br>Qn No: 9   | 1 Mark |
|              | Part B<br>Qn No: 9   | 3 Mark |
|              | Part C<br>Qn No: XIV | 7 Mark |

**Guidelines:**

- Calculate the percentage of marks obtained by the student considering the total marks excluding the marks of out of syllabus questions (If he had attended that option).
- Then the proportionate marks of out of syllabus questions shall be calculated based on the above obtained percentage.
- Marks obtained in the above cases shall be added to get the actual marks admissible to the student.

TECHNICAL EXAMINATIONS

To:

- Camp Officers of Centralised Valuation Camps.
- Stock file & Office copy.



JOINT CONTROLLER

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## BLUE PRINT

## Mark Distribution

Module	Hr/ Module	$(h_i / \sum H_i) * 123$	TYPE OF QUESTIONS							
			PART A		PART B		PART C		TOTAL	
			No of Questions	Marks	No of Questions	Marks	No of Questions	Marks	No of Questions	Marks
I	12	25.44	2	2	3	9	2	14	7	25
II	17	36.05	3	3	2	6	4	28	9	37
III	14	29.689	3	3	4	12	2	14	9	29
IV	15	31.81	1	1	1	3	4	28	6	32
<b>Total</b>	<b>58</b>	<b>122.989</b>	<b>9</b>	<b>9</b>	<b>10</b>	<b>30</b>	<b>12</b>	<b>84</b>	<b>31</b>	<b>123</b>

## Cognitive Level Wise Question Analysis

## Mark Distribution

Cognitive Level	%Marks	Marks	TYPE OF QUESTIONS							
			PART A		PART B		PART C		TOTAL	
			No of Questions	Marks	No of Questions	Marks	No of Questions	Marks	No of Questions	Marks
R	9.75%		5	5	2	6	1	7	8	18
U	78.86%		4	4	8	24	9	63	21	91
A	11.38%						2	14	2	14
<b>Total</b>	<b>100</b>		<b>9</b>	<b>9</b>	<b>10</b>	<b>30</b>	<b>12</b>	<b>84</b>	<b>31</b>	<b>123</b>


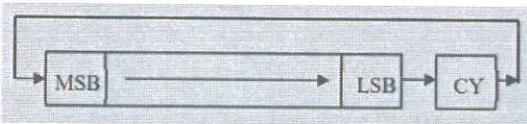
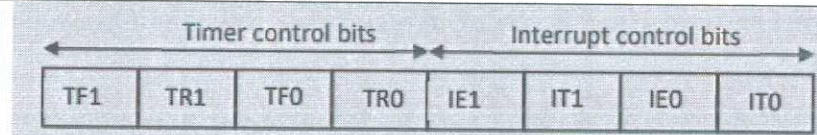
### Scoring Indicators

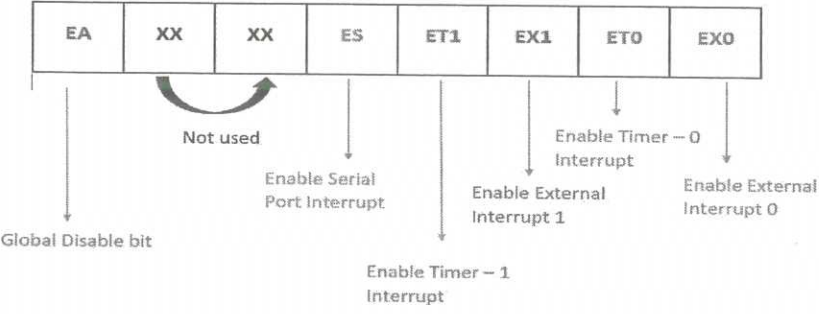

#### COURSE MICROCONTROLLER AND APPLICATIONS

COURSE CODE: 4041 QID: 2103230128

Q No	Scoring Indicators	Split score	Sub Total	Total score
<b>PART A</b>				<b>9</b>
I.1	To latch the address from the address bus onto the external latch		1	
I.2	Address bus-16 bits.		1	
I.3	FF		1	
I.4	Stack is a data structure implemented in the RAM area and is used to store address and data when the microcontroller branches to subroutine		1	
I.5	DJNZ- Decrement and Jump if Not Zero		1	
I.6	Serial communication interrupt - RI/TI Timer 0 overflow interrupt - TF0 Timer 1 overflow interrupt - TF1 External hardware interrupt - INT0 External hardware interrupt - INT1	Any two	1	
I.7	Mode-2		1	
I.8	To program the start bit, stop bit, and data bits of framing		1	
I.9	Stepper motor		1	
<b>PART B</b>				<b>24</b>
II.1	1. 8 bit microcontroller 2. 128 byte internal RAM (Data Memory ) 3. 4KB internal ROM (Program Memory ) 4. 4 register banks 5. 40 pin IC in DIP 6. +5v supply 7. Clock rating is 12Mhz 8. 8-bit bidirectional data bus	Any six points	3	3

	<p>9. 16-bit unidirectional address bus</p> <p>10. 32 general purpose registers each of 8-bit</p> <p>11. 4 no of 8 bit parallel ports</p> <p>12. Two 16-bit Timers.</p> <p>13. 16-bit program counter and data pointer</p>																		
II.2	<p>PORT P3 (Pins 10 to 17):</p> <p>In addition to acting as a normal I/O port,</p> <ul style="list-style-type: none"> <li>• P3.0 can be used for serial receive input pin(RXD)</li> </ul> <p>P3.1 can be used for serial transmit output pin(TXD) in a serial port</p> <p>P3.2 and P3.3 can be used as external interrupt pins(INT0' and INT1')</p> <p>P3.4 and P3.5 are used for external counter input pins(T0 and T1)</p> <p>P3.6 and P3.7 can be used as external data memory write and read control signal pins(WR'and RD')read and write pins for memory access.</p>	3	3	3															
II.3	<p>Using the bits RS1(PSW.4) and RS0(PSW.3) the register banks can select.</p> <table border="1"> <thead> <tr> <th>RS1</th> <th>RS0</th> <th>register bank</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>bank0</td> </tr> <tr> <td>0</td> <td>1</td> <td>bank1</td> </tr> <tr> <td>1</td> <td>0</td> <td>bank2</td> </tr> <tr> <td>1</td> <td>1</td> <td>bank3</td> </tr> </tbody> </table>	RS1	RS0	register bank	0	0	bank0	0	1	bank1	1	0	bank2	1	1	bank3	3	3	3
RS1	RS0	register bank																	
0	0	bank0																	
0	1	bank1																	
1	0	bank2																	
1	1	bank3																	
II.4	<ul style="list-style-type: none"> <li>• A subroutine is always executed with the CALL instruction</li> <li>• When the CALL instruction is executed the PC register contains the address of the next instruction to be executed (this is known as the return address)</li> <li>• The PC is saved onto the stack low byte first – The PC is then loaded with the address of the subroutine</li> <li>• The subroutine is then executed</li> <li>• The last line of a subroutine is always the RET instruction</li> <li>• The RET instruction will cause the return address to be popped off the stack and loaded into the PC – The instruction at the return</li> </ul>	3	3																

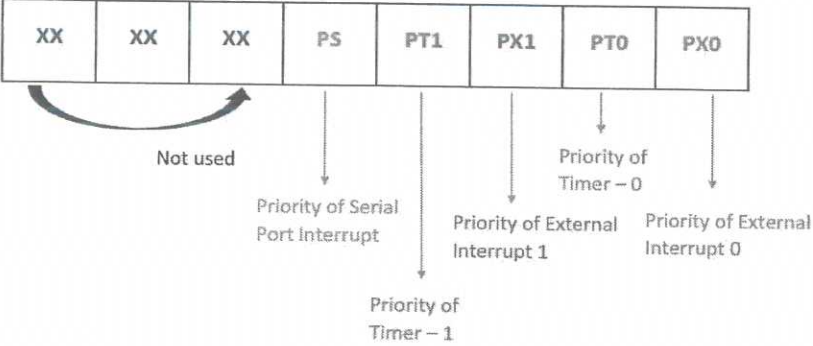
	address is then executed			
II.5	<p>RR: The rotate right (RR) instruction rotates the content of accumulator right by one bit position. All bits, starting with MSB, are shifted right with the LSB fed back to the MSB. The format of the instruction is as follows</p>  <p>RRC: The instruction rotate right through carry (RRC) is similar to RR with the exception that the carry flag (CY) behaves as an extension to the least significant side of the accumulator. The bits from MSB towards the LSB are shifted to the right by one bit position. The LSB gets shifted to CY while the CY is rotated back to the MSB of A. The format of the instruction is as follows</p> 	1/2	3	3
II.6	 <p>TFx: Timer x overflow flag, TRx: Timer x run control  IEx: External interrupt x edge flag, ITx: External interrupt x control  x = 0, 1</p>	3	3	3
II.7	<ul style="list-style-type: none"> <li>• A baud rate is the number of signal changes that occur per second in a communication channel.</li> <li>• It represents the speed at which data is transmitted over a serial link.</li> <li>• In 8051, the baud rate is set by the SMOD (Serial Mode) and TH1 (Timer 1 High byte) registers, and is calculated using the following formula:  <math display="block">\text{Baud Rate} = F_{\text{osc}} / (\text{SMOD} * 32 * (256 - \text{TH1}))</math> </li> </ul> <p>Where Fosc is the frequency of the oscillator used to drive the microcontroller.</p>	Any point	3	3
II.8	The enable/disable status of the 8051 interrupt is controlled by the setting of the Interrupt Enable (IE) register.		3	

		3		
II.9	 <p>1. <b>SMOD</b> -Serial Communication Baud Rate Modify Bit</p> <p>2. <b>GF1</b> -- General Purpose User Flag (Bit 1)-- To indicate the status of various events.</p> <p>3. <b>GF0</b> -General Purpose User Flag (Bit 0)-- To indicate the status of events.</p> <p>4. <b>PD</b> ----Power Down Bit---To enter Power Down Mode, set to 1.</p> <p>5. <b>IDL</b> ----Idle Mode Bit----To enter Idle Down Mode, set to 1.</p>	1  2	3	
II.10			3	
<b>PART C</b>				42

III.		7	7	7
VI	<p>Data Memory is used for temporarily storing data and intermediate results created and used during the operation of the microcontroller. 8051 has 128 byte data memory (RAM).with address space - 00H to 7FH.</p> <p>128 bytes Internal RAM is divided in several blocks.</p> <ol style="list-style-type: none"> <li>1. Register Banks (00H to 1FH):</li> <li>2. Bit-Addressable RAM (20H to 2FH):</li> <li>3. General Purpose RAM (30H to 7FH):</li> </ol> <p><u>Register Banks (00H to 1FH):</u></p> <p>The first block consists of 4 banks each including 8 registers denoted by R0-R7. These are the lowest 32 bytes of RAM space . Each bank consists of registers R0, R1, R2, R3, R4, R5, R6 and R7. At a time, only one bank of registers is active that can be used by the instruction being executed.</p> <p><u>Bit-Addressable RAM (20H to 2FH):</u></p> <p>The next memory block (address 20h- 2Fh) is bit- addressable, which means that each bit has its own address (0-7Fh). Since there are 16 such registers, this block contains in total of 128 bits with separate addresses. These 16 memory</p>	4	7	7

	<p>locations of which individual bits can be referred to by the bit-manipulating instructions. Such instructions can set/clear a bit, complement it or check the value.</p> <p><u>General Purpose RAM (30H to 7FH):</u></p> <p>These 80 bytes of RAM locations could be used as general-purpose storage space by the programs and addressable as byte.</p> <p><u>Additional RAM:</u> beyond 7FH (and till 0FFH), some RAM addresses are defined to correspond to some special function registers.</p> <p>The diagram shows a memory map from 00H to 7FH. It is divided into several sections: <ul style="list-style-type: none"> <li>00H to 07H: Register Bank-0 (R0 to R7)</li> <li>08H to 0FH: Register Bank-1 (R8 to RF)</li> <li>10H to 1FH: Register Bank-2 (R10 to RF)</li> <li>18H to 1FH: Register Bank-3 (R18 to RF)</li> <li>20H to 2FH: Bit Address Area (16 bytes)</li> <li>30H to 7FH: General Purpose Area (48 bytes)</li> </ul> Annotations indicate: <ul style="list-style-type: none"> <li>80 bytes for the General Purpose Area (30H-7FH).</li> <li>16 bytes for the Bit Address Area (20H-2FH).</li> <li>32 bytes = 8 x 4 bytes for the Register Banks (00H-1FH).</li> <li>No. of Bits = 16 x 8 = 128, Bit address 00H - 7FH.</li> </ul> </p>	3		
V.	<p>An Addressing Mode is a way to locate a target Data, which is also called as Operand. The 8051 Family of Microcontrollers allows five types of Addressing Modes for addressing the Operands. The addressing modes available with the 8051 are as follows.</p> <ul style="list-style-type: none"> <li>• Immediate addressing</li> <li>• Register addressing</li> <li>• Direct addressing</li> <li>• Register indirect addressing</li> <li>• Bit direct addressing</li> </ul>	5	Explanation of any one	7
VI	<p><b>Conditional Branching :</b> These instructions modify the PC value with the jump target if the specified condition is met. All conditional branches are</p>	1		



	<p>default interrupt priority is changed by programming the Interrupt Priority (IP) Special Function register. To change a higher priority to any of the interrupts, change the corresponding bit in the IP register high.</p> 	4	7	
X	<p>Steps to program in mode 2</p> <p>To generate a time delay using the timer's mode 2, take the following steps.</p> <ul style="list-style-type: none"> <li>• Load the TMOD value register indicating which timer (Timer 0 or Timer 1) is to be used, and select the timer mode (mode 2).</li> <li>• Load the TH registers with the initial count value.</li> <li>• Start the timer.</li> <li>• Keep monitoring the timer flag (TF) with the "JNB TFx, target" instruction to see whether it is raised. Get out of the loop when TF goes high.</li> <li>• Clear the TF flag.</li> <li>• .Go back to Step 4, since mode 2 is auto-reload.</li> </ul>	7	7	7

<p>XI</p>		<p>7</p>	<p>7</p>	<p>7</p>
<p>XII</p>	<p>Interfacing of ADC 0804 to 8051 Microcontroller :</p> <p>ADC 0804 is a single channel analog to digital converter i.e., it can take only one analog signal. ADC 0804 has 8 bit resolution. For an ADC with resolution of 8 bits, the step size is 19.53mV (5V/255). The time taken by the ADC to convert analog data into digital form depends on the frequency of clock source. To use the internal clock a capacitor and resistor are used as shown in the circuit. The input to the ADC is given from a regulated power supply and a 10K Potentiometer. The 8051 Microcontroller is used to provide the control signals to the ADC. CS(chip select) pin of ADC is directly connected to ground. The pin P1.1, P1.0 and P1.2 are connected to the pin WR, RD and INTR of the ADC respectively. When the input voltage from the preset is varied the output of ADC varies also varies.</p>	<p>3</p>	<p>7</p>	

		4		
XIII	<p>Keyboard is an Input peripheral device to give data to 8051. It consists of push button switches. When a key pressed in a keyboard, the push button switch will send a specific code to 8051 and hence 8051 can identify which key is pressed. Each time a key is pressed a code is generated and transmitted. There is only 1 code associated with a key. Each switch makes electrical contact when pressed. At the lowest level keyboard are organized in a matrix of rows and columns. The CPU access both rows and columns through ports, therefore through the 8 bit ports of 8051 an 8x8 matrix of keys can be connected to a controller. The figure below shows a 4x4 keyboard connected to 2 ports. The rows are connected to a Output port and the columns are connected to an Input port. If no key is pressed the voltage of columns will not change, since they are all connected to high Vcc. If all the rows are grounded and a key is pressed one of the columns will have 0 since the key provides a path to ground. It is the function of 8051 to scan the keyboard continuously to detect and identify the key pressed.</p>	3	7	7

		4		
XIV	<p>P1.0 to P1.7 pins of the microcontroller is connected to the DB0 to DB7 pins of the module respectively and through this route the data goes to the LCD module. P3.3, P3.4 and P3.5 are connected to the E, RW, RS pins of the microcontroller and through this route the control signals are transferred to the LCD module. Resistor R1 limits the current through the back light LED and so do the back light intensity. POT is used for adjusting the contrast of the display. Other important pins RS, R/W and E are connected via the port bits P3.2, P3.1 and P3.0, respectively. The program works by checking the busy flag, DB7 pin status, before issuing a command or data to the LCD.</p>	3	7	7
		4		