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April - 24

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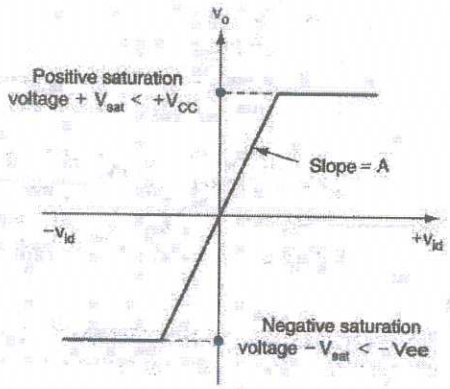
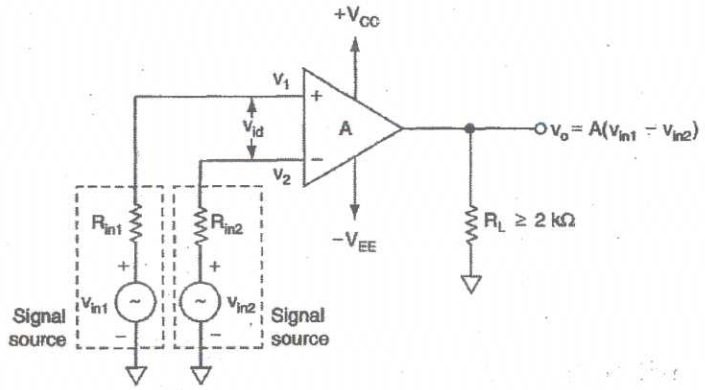
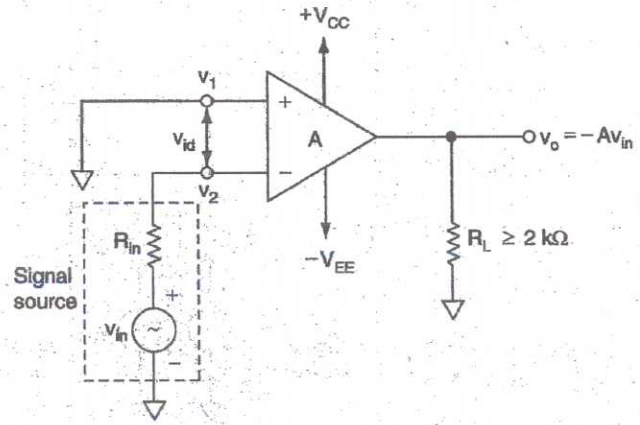
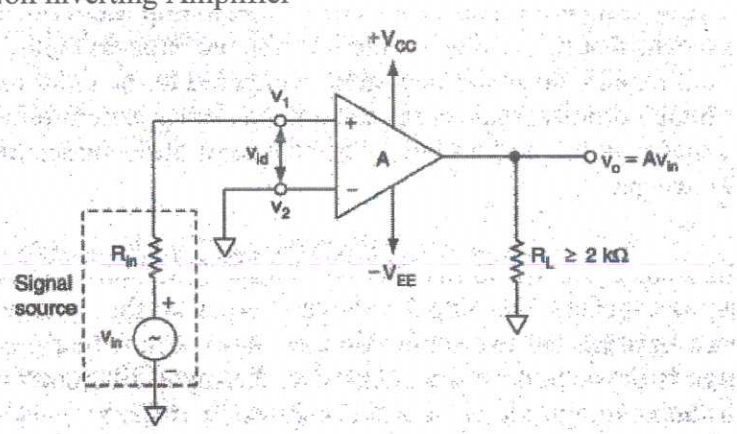
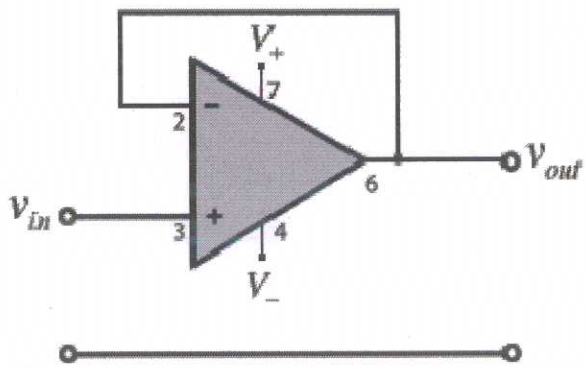
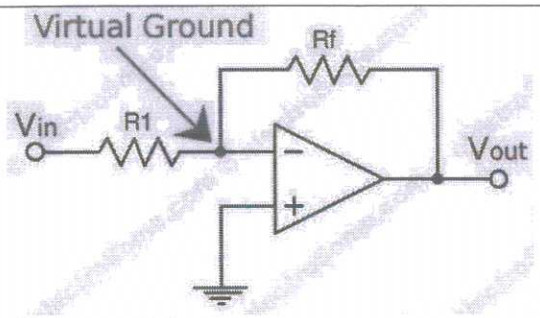
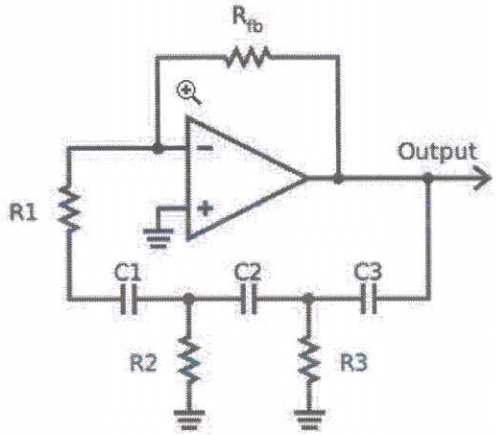
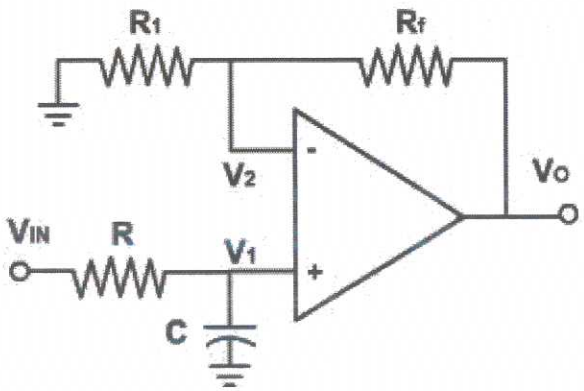
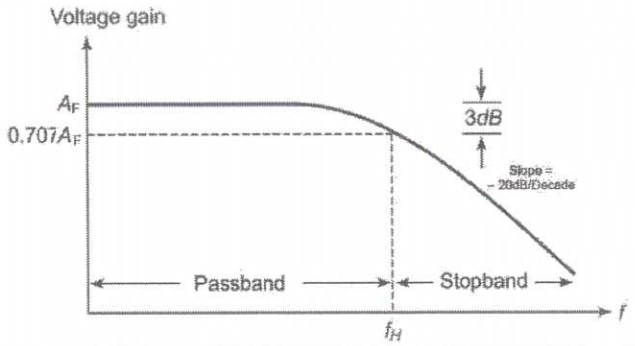
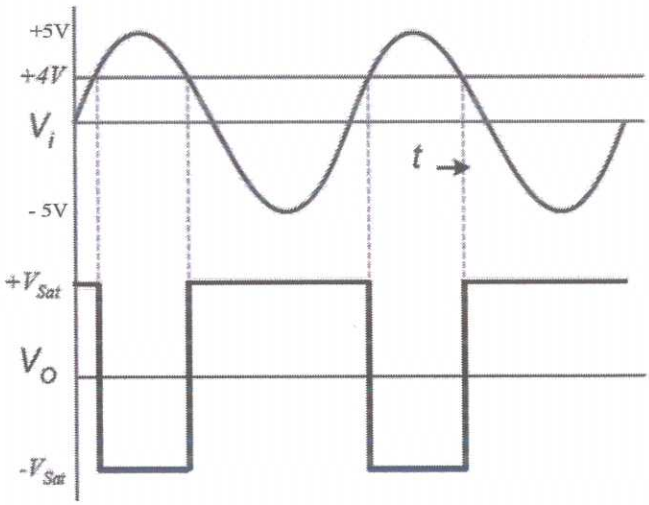
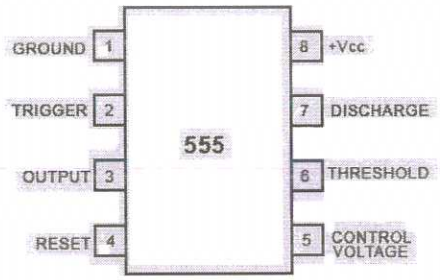
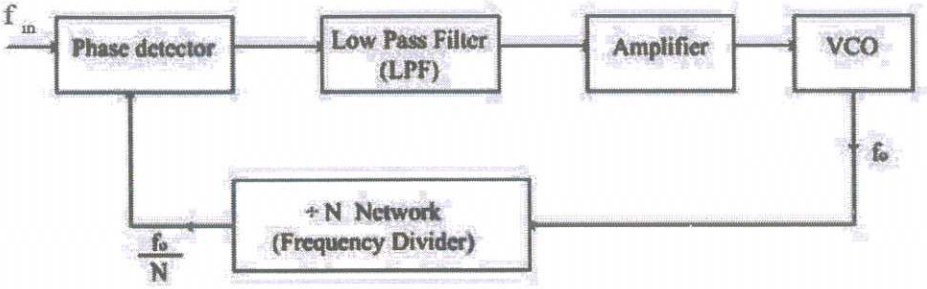
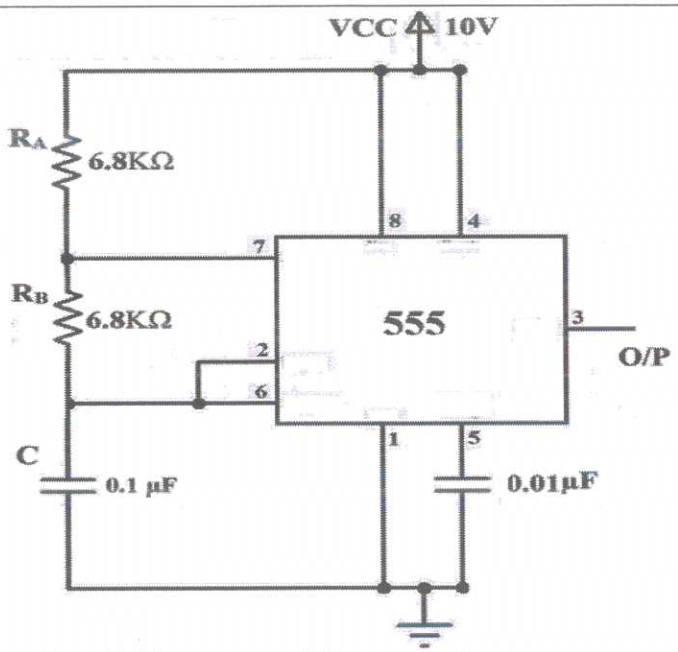
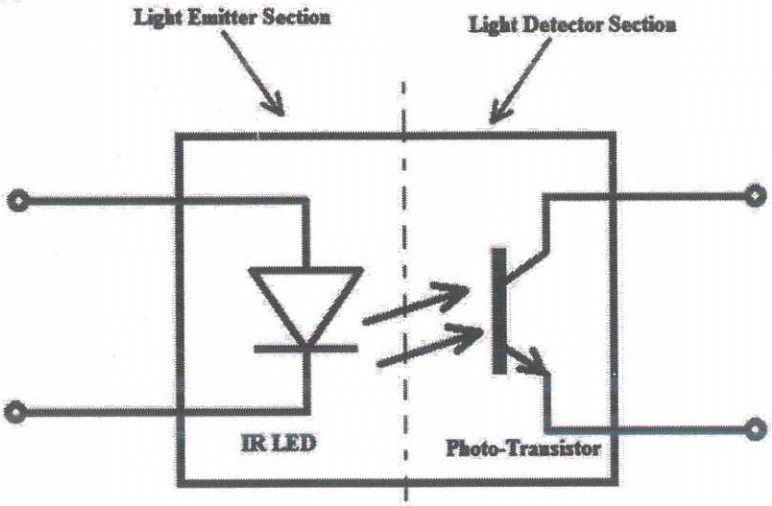
SCORING INDICATORS

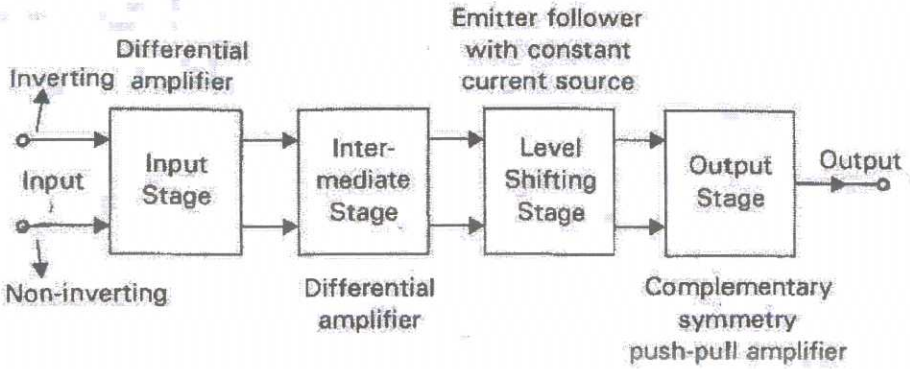
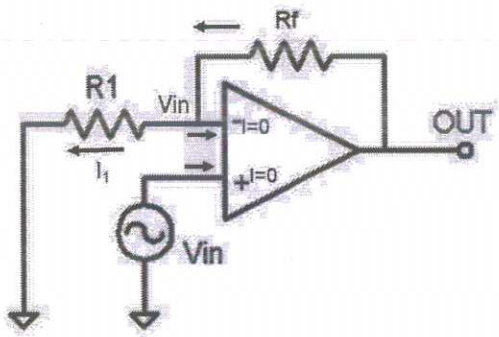
	Course Code: 4043 Revision : 2021 Course Title : LINEAR INTEGRATED CIRCUITS QID : 2103230121	SET 1		
Qn. No.	**Scoring Indicator**	**Split score**	**Sub Total**	**Total Score**
	PART A			9
I.1	Voltage that is applied between the two input terminals of the op-amp to null the output	1	1	1
I.2		1	1	1
I.3	It is basically a voltage comparator whose output changes when the input signal crosses the zero volt reference voltage level	1	1	1
I.4	- Designed to shift the input waveform either above or below a DC reference level without altering the shape of the waveform - Function as a level shifter	1	1	1
I.5	[Any one of the following] - sine wave to square wave converter - remove noise from signals used in digital circuits (signal conditioning) - convert slow edges to fast edges - to debounce a switch	1	1	1
I.6	T= Ton+ Toff = 0.693 (R_A+2R_B)C for AMV T=1.1RC for MMV	0.5 0.5	1	1
I.7	- PLL is a feedback control system that automatically adjusts the frequency and phase of a locally generated signal to match the frequency and phase of an input signal. OR - Regeneration of carrier signal	1	1	1
I.8	IC voltage regulators provide a constant DC output voltage that is independent of the input voltage, output load current, and temperature	1	1	1
I.9	DAC converts a digital signal into a corresponding analog voltage or current.	1	1	1

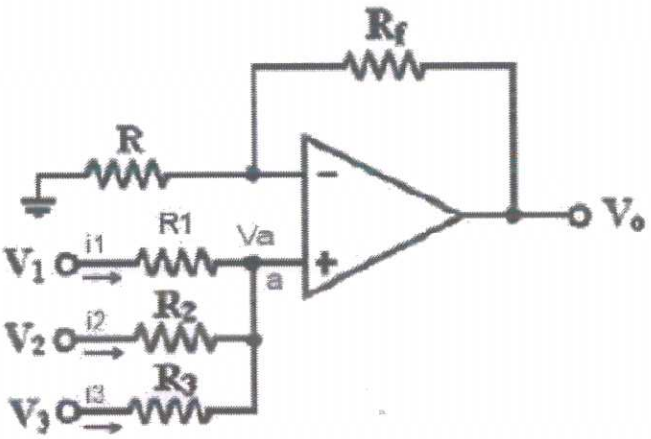
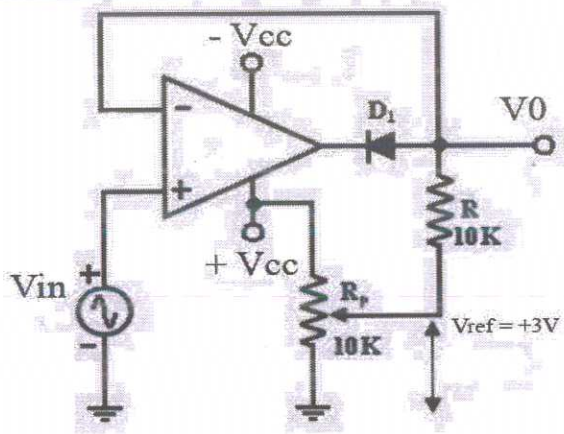
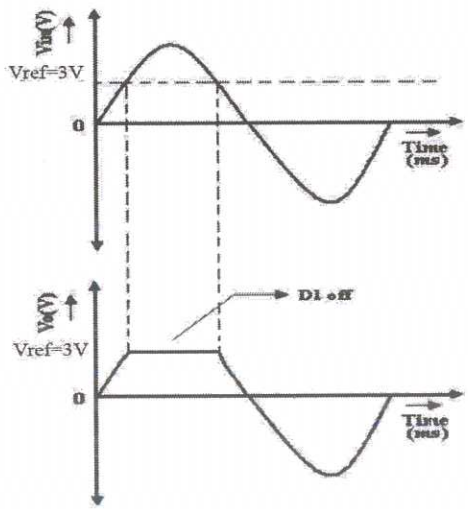
	PART B			24
II 1	◉ Differential Amplifier  	1	3	3
	◉ Inverting Amplifier  	1		
	◉ Non inverting Amplifier  	1		
II 2	 • An amplifier whose output voltage is equal to input • I/P impedance is high, giving isolation of the o/p from the signal source • Draws very little power from the signal source, avoiding loading effects • If Rf=0 or R1=infinity, we get a voltage follower	2 Fig. 1 Des.	3	3

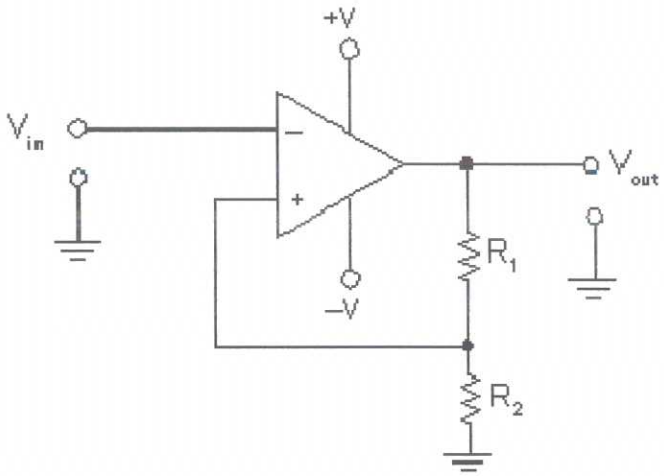
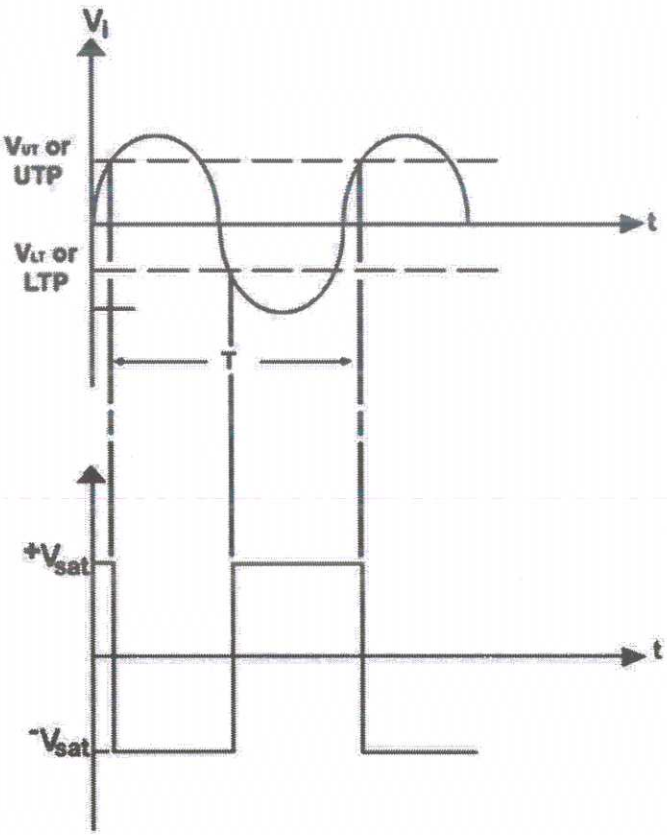
II 3	 • A node is virtually grounded • The point is not physically connected to ground but voltage at that point/node is '0V' so we refer to it as Ground • In ideal Op-Amp Configuration, differential input voltage is '0', ie. V(non-inv) — V(inv) =0 • So ideally V(inv) = V(non-inv.) • In Inverting Configuration, V(non-inv)=0 • Since V(inv) = V(non-inv.), V(inv) is also equal to '0V'	2 Fig 1 Des.	3	3
II 4	 • Feedback network offers 180 degree phase shift and inverting amplifier also provides 180 degrees phase shift. Hence, the total phase shift around the loop is 360 degrees • Each of the R-C filter produces a phase shift of 60° so the whole filter circuit generates 180° phase shift. • The energy storage capacity of a capacitor or noise in resistor produces a noise voltage which is likely to a small sine wave, it is then amplified using an op amp inverting amplifier.	2 Fig 1 Des.	3	3
II 5		1.5 Fig	3	3

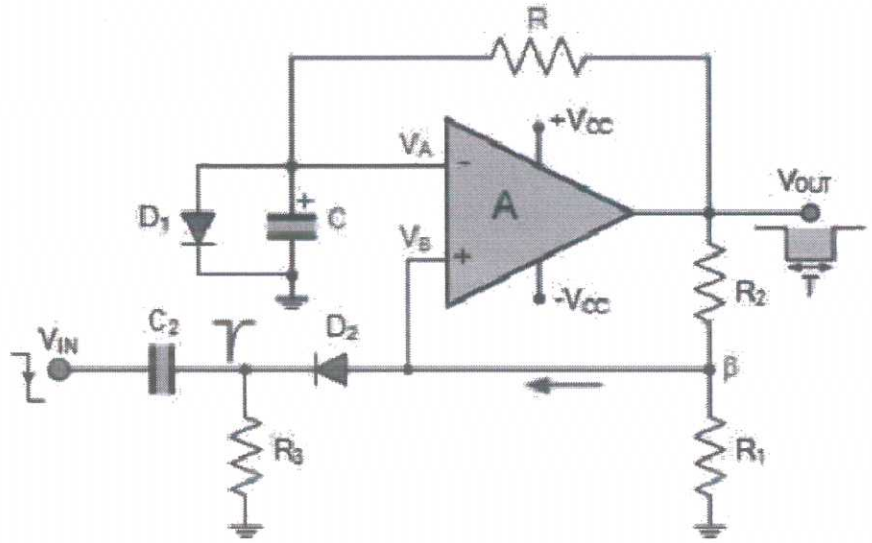
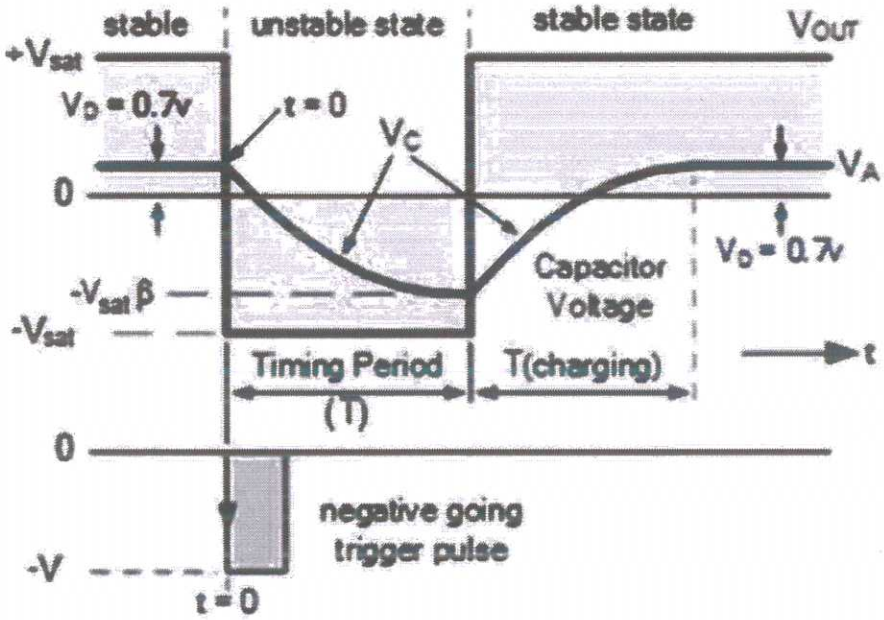
		1.5 Fig		
II 6	 A voltage comparator is a two-input circuit that compares the voltage at one input to the voltage at the other input. The output will be at its negative saturation value when the input is greater than the reference (4V) and at its positive saturation value when the input is less than the reference.	2 Fig. 1 Des.	3	3
II 7	 Pin 1: Ground Terminal ➢ All the voltages are measured with respect to the Ground terminal Pin 2: Trigger Terminal ➢ Used to feed the trigger input Pin 3: Output Terminal Pin 4: Reset Terminal: ➢ To reset the IC Pin 5: Control Voltage Terminal: ➢ The threshold and trigger levels are controlled using this pin Pin 6: Threshold Terminal ➢ This is the non-inverting input terminal of comparator 1 Pin 7: Discharge Terminal ➢ This pin is connected internally to the collector of transistor Pin 8: Supply Terminal ➢ A supply voltage of + 5 V to + 18 V is applied to this terminal	1 Fig. 2 Des.	3	3

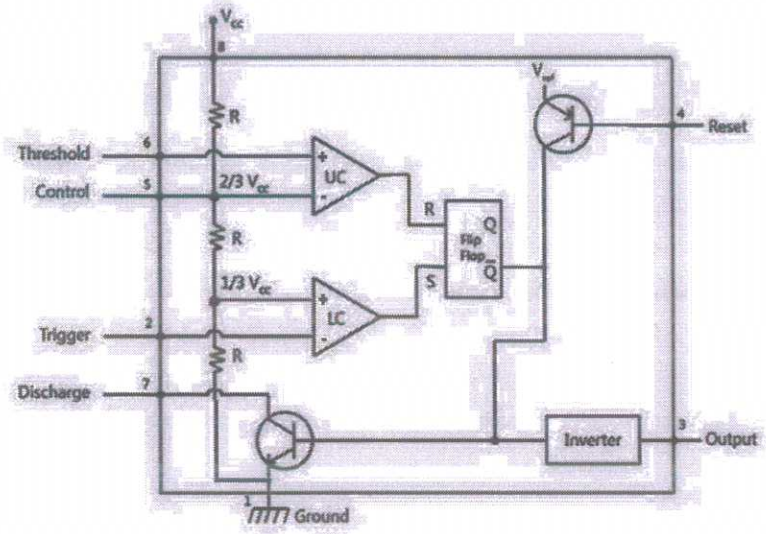
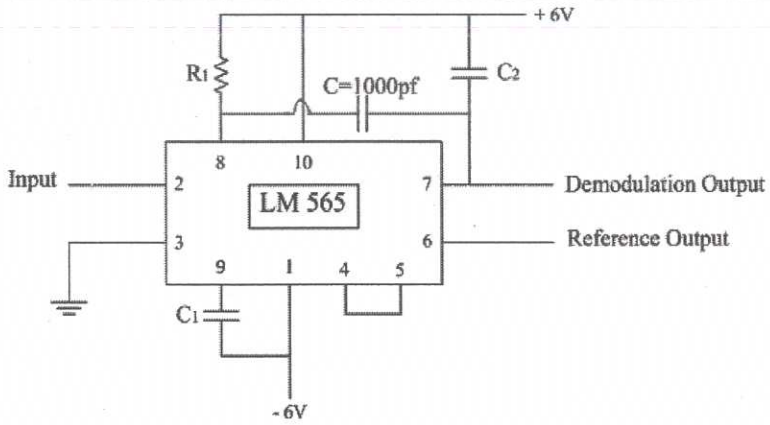
II 8		3 Fig	3	3
II 9	 [check for suitable values of C, R_A and R_B] Let C = 0.1 µF t_{ON} = 1ms = 0.69(R_A+R_B)C t_{OFF} = 0.5ms = 0.69(R_B)C, So R_B = 7.2 KΩ ≈ 6.8KΩ (std) 0.69 (R_A+R_B) C = 1ms R_A + R_B = 14.4 KΩ, R_A = 14.4 KΩ – R_B R_A = 7.6 KΩ = 6.8KΩ (std)	2 Fig. 1 Design	3	3
II 10	 The working principle of an opto-coupler is based on the modulation of light by an electrical signal. The input circuit is connected to an LED that emits light when a voltage is applied across its terminals. The output circuit is connected to a photodetector, such as a photodiode or phototransistor that generates an electrical signal in response to the received light.	2 Fig. 1 Des.	3	3

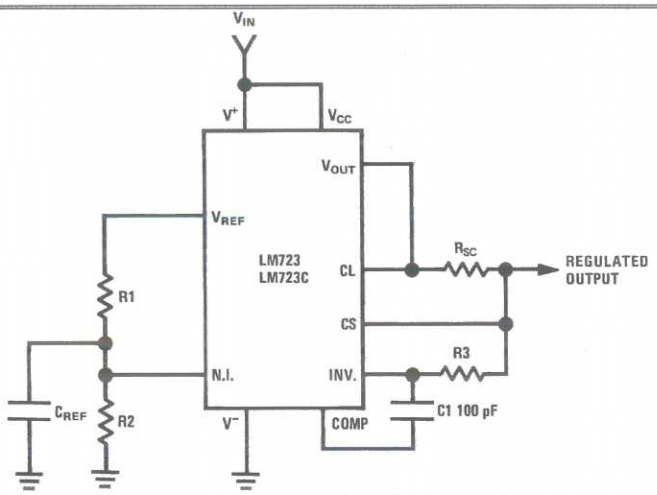
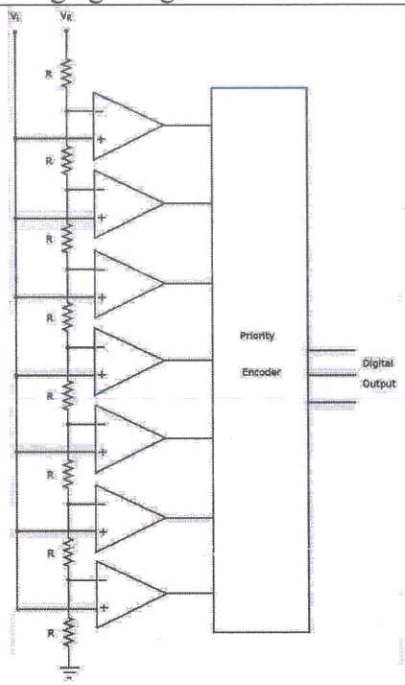
	PART C			42
III 1.	 **Input Stage** : ◉ A dual-input, balanced output differential amplifier. ◉ provides most of the voltage gain to OP-AMP, establishes the input resistance of the OP-AMP. ◉ rejects the common noise signals present at the input terminals and amplifies only the difference between the input signals **Intermediate Stage :** ◉ dual input, unbalanced output differential amplifier. ◉ driven by the o/p of first stage - is used to provide some additional gain. ◉ direct coupling between the first two stages. ◉ d.c. level at the output of intermediate stage is above the ground level. ◉ This is undesirable **Level Shifting Stage :** ◉ This is an emitter follower using constant current source. ◉ shift the d.c. level at the output of intermediate stage downwards to 0v. **Output Stage :** ◉ push-pull or complementary symmetry push-pull amplifier. ◉ large o/p voltage swing capability-large o/p current swing capability - low o/p resistance.	4 Block 3 Des.	7	7
III 2.	 $\frac{V_0 - Vin}{Rf} = \frac{V_{in} - 0}{R1}$ $\frac{V_0}{Rf} - \frac{V_{in}}{Rf} = \frac{V_{in}}{R1}$ $\frac{V_0}{Rf} = \frac{V_{in}}{R1} + \frac{V_{in}}{Rf}$ $\frac{V_0}{Vin} = 1 + \frac{Rf}{Rin}$ $Av = 1 + \frac{Rf}{Rin}$	4 Fig. 3 Deriva tion	7	7

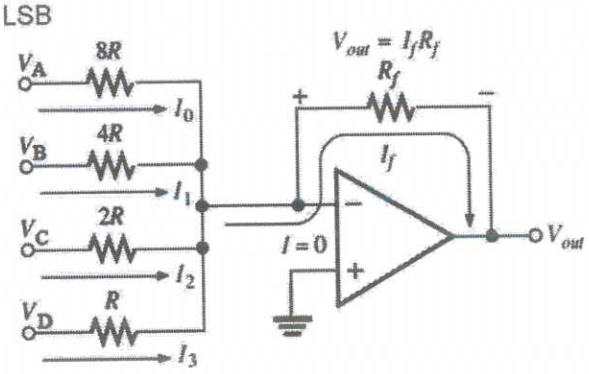
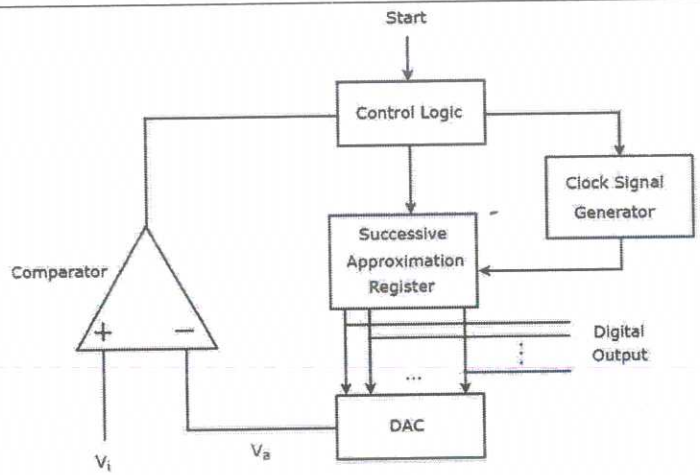
III 3.	 ◉ Nodal eqn at a $I_1+I_2+I_3=0$ $\frac{V1-Va}{R1}+\frac{V2-Va}{R2}+\frac{V3-Va}{R3}=0$ $\frac{V1}{R1}+\frac{V2}{R2}+\frac{V3}{R3}=Va\left[\frac{1}{R1}+\frac{1}{R2}+\frac{1}{R3}\right]$ $Va=\frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}}$ $V_0=\left(1+\frac{Rf}{R}\right)Va=\left(1+\frac{Rf}{R}\right)\left[\frac{\frac{V1}{R1}+\frac{V2}{R2}+\frac{V3}{R3}}{\frac{1}{R1}+\frac{1}{R2}+\frac{1}{R3}}\right]$ ◉ If R1=R2=R3, and $\left(1+\frac{Rf}{R}\right)=3$ then $V0=[V1+V2+V3]$	4 Fig 3 Proof	7	7
III 4.	 	3 Fig. 2 Wave	7	7

	- When $V_{in} < V_{ref}$, V_0 of the op-amp becomes negative to drive D_1 into conduction. When D_1 conducts it closes feedback loop and op-amp operates as a voltage follower. (i.e.) Output V0 follows input until $V_{in} = V_{ref}$. - When $V_{in} > V_{ref}$, V_0 becomes +ve to drive D_1 into off. It opens the feedback loop.	2 Des.		
III 5.	  ◉ When output=+Vsat, the voltage appearing at the non-inverting terminal is V_{UT} or UTP = +Vsat*R2/(R1+R2) ◉ When input Vin is greater than UTP, then the voltage at inverting terminal is greater than the voltage at non inverting terminal. So the output will switch from +Vsat to –Vsat. ◉ When output =–Vsat, the voltage appearing at the non-inverting terminal is called V_{LT} or LTP =–Vsat*R2/(R1+R2) ◉ Now if the input is allowed to fall below LTP, then the voltage at non inverting terminal is greater than the voltage at inverting terminal ◉ The output will switch from – Vsat to +Vsat	3 Fig. 2 Wave 2 Des.	7	7

III 6.		3 Fig.	7	7
		2 Wave		
	• Assume that Vout=+Vsat. Then the voltage at the non-inverting input +βVsat where β is the feedback fraction • The inverting input is held at 0.7 volts • C charges up to the same 0.7 volts • If a negative pulse is applied to the non-inverting input, the output switches state and saturates towards the negative supply, -Vcc. The result is that the potential at VB is now equal to -Vcc.β. • Capacitor charges up exponentially in the opposite direction • D1 becomes reverse-biased • C will discharge with a time constant T=RC • When the capacitor voltage reaches–βVsat, the op-amp switches back to its stable state (i.e. Vout=+Vsat)	2 Des.		

III 7.	 • Comparator 1 compares threshold voltage with a reference voltage + 2/3 VCC volts. Comparator 2 compares the trigger voltage with a reference voltage + 1/3 VCC volts. Output of both the comparators is supplied to the flip-flop • One transistor is a discharge transistor - collector is connected to pin 7, transistor saturates or cuts-off according to the output state of FF • The saturated transistor provides a discharge path to a capacitor • Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the timer • Output of the upper comparator is applied to (R) input of the flip-flop • Whenever the threshold voltage exceeds the control voltage, the upper comparator will reset the flip-flop • Discharge transistor saturates and thus discharges the capacitor that is connected externally to the discharge pin 7 • When the voltage at the trigger input falls below + (1/3) Vcc, lower comparator triggers the flip-flop, forcing its output to SET • This also turns the discharge transistor off and forces the power amplifier to output a high • Capacitor connected at pin 7 charges	4 Fig. 3 Des.	7	7
III 8.	 There is shift in carrier frequency about the mean value according to modulating signal at FM transmitter. The deviation or shift in carrier frequency from centre value is converted to a voltage. Assume the loop is in locked condition, so VCO frequency and input frequency is same. FM signal is applied as input to phase detector. Phase detector produce error voltage proportional to frequency shift. This signal is passed through LPF and amplifier to give error voltage. Thus error voltage is proportional to change in frequency. As input frequency is shifted up or down, VCO voltage also varies accordingly.	4 Fig 3 Des.	7	7

III 9.	 Difference between V_{NI} and Vout which is directly fed back to the INV terminal is internally amplified by error amplifier. Referring to internal diagram, the output of error amplifier drives the pass transistor so as to minimise the difference between NI and INV inputs of error amplifier. If the output voltage becomes low, the voltage at the INV terminal of error amplifier also goes down. This makes the output of the error amplifier to become more positive, thereby driving transistor Q1 more into conduction. This reduces voltage across Q1 and drives more current into the load causing voltage across load to increase. So the initial drop in the load voltage has been compensated. Similarly, any increase in load voltage, or changes in the input voltage get regulated.	4 Fig. 3 Des.	7	7
III 10.	 - Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top - All the comparators compare the external input voltage with the voltage drops present at the respective other input terminal - Output of the comparator will be '1' as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, Vi is less than or equal to the voltage drop present at the respective other input terminal. - All the outputs of comparators are connected as the inputs of priority encoder - This priority encoder produces a binary code (digital output)	4 Fig. 3 Des.	7	7

III 11.	LSB  MSB ◉ Each of the input resistors will either have current or have no current, depending on the input voltage level $I_O = \frac{V_A}{8R}, I_1 = \frac{V_B}{4R}, I_2 = \frac{V_C}{2R}, I_3 = \frac{V_D}{R}$ ◉ All of the input currents sum together and go through Rf ◉ The lowest-value resistor (R) corresponds to the highest binary-weighted input (2^3). The other resistors are multiples of R (that is, 2R, 4R, and 8R) and correspond to the binary weights 2^2, 2^1, and 2^0, respectively $V_O = -I_F R_F$ $= -\left(\frac{R_F}{8R}V_A + \frac{R_F}{4R}V_B + \frac{R_F}{2R}V_C + \frac{R_F}{R}V_D\right)$	4 Fig. 3 Des.	7	7
III 12.	 Initially, the digital number in the SAR is zero. The SAR then turns on (sets) its most significant bit (MSB). This causes the DAC to deliver to the second input of the comparator a feedback voltage proportional to this bit. The comparator determines whether the feedback voltage is larger than the input signal. If the feedback voltage is larger, the comparator's output tells the SAR to turn off (clear) the MSB; if the feedback voltage is not larger, the MSB remains set. The SAR then sets the next bit, the comparator again determines whether the new feedback voltage is larger than the input signal, and, depending as before on the result of the comparison, this bit is either allowed to remain or is cleared. This process continues until the least-significant bit has been allowed to remain on or is cleared. Each bit that remains on in the SAR represents a logical 1, and those turned off are logical 0's. At the end the digital representation of analog voltage is stored in the SAR.	4 Fig. 3 Des.	7	7