

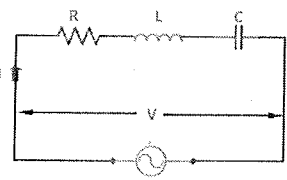
Scoring Indicators

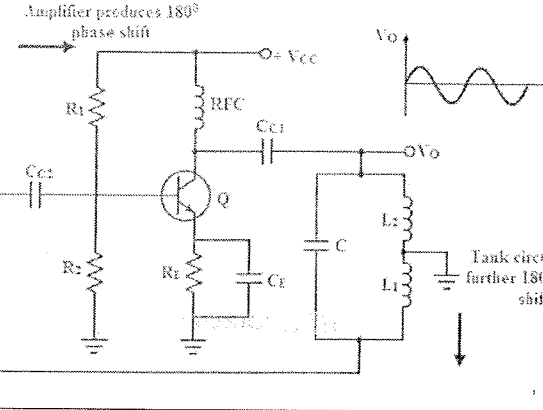
COURSE NAME: ELECTRONIC CIRCUITS

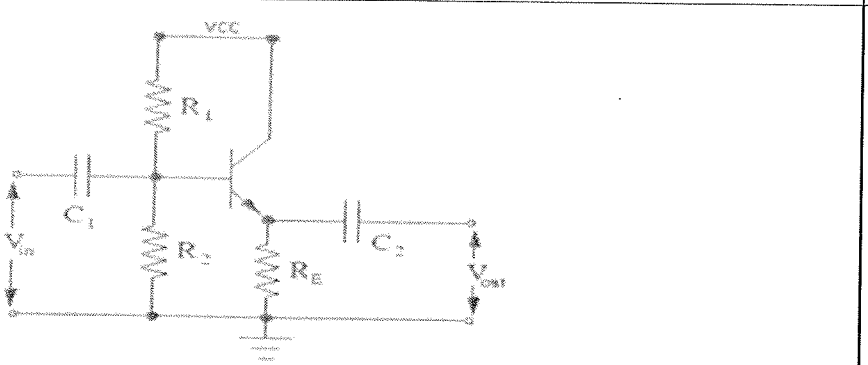
COURSE CODE: 3043

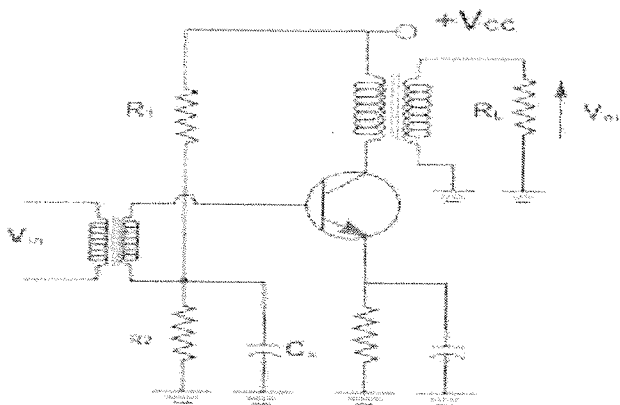
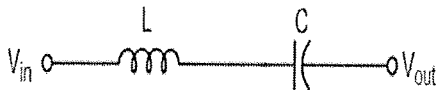
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Q No	Scoring Indicators	Split score	SubTotal	Total score
PART A				9
I.1	Emitter-base is forward biased and collector-base junction is reverse biased		1	
I.2	When no signal is applied to the input		1	
I.3	$BW = f_r/Q$, Where, f_r -Resonance frequency, Q – Quality factor, BW -Bandwidth.		1	
I.4	Efficiency of a power amplifier = P_{ac}/P_{dc} where, P_{ac} - ac output power, P_{dc} - dc output power		1	
I.5	The expression for gain of a positive feedback amplifier. $A_f = A/(1 - A\beta)$		1	
I.6	When an ac voltage is applied across quartz crystal, it vibrates at the frequency of the applied voltage. OR If a mechanical force is applied to a quartz crystal, it generates an a-c voltage.		1	
I.7	Cut-off and saturation		1	
I.8	Astable multivibrator		1	
I.9	Schmitt trigger circuit		1	
PART B				24
II.1	Given $\beta = 100$, $V_{BE} = 0.7$ V, $I_C = 1$ mA and $V_{CC} = 6$ V , We know for fixed bias method, $V_{CC} = I_B R_B + V_{BE}$, $I_B = I_C / \beta$. On substituting values, we get $I_B = 10$ μ A, base resistor $R_B = 530$ k Ω .	1 1 1	3	
II.2	The overall voltage gain in dB of the three-stage amplifier is given as $A_{dB} = A_{dB1} + A_{dB2} + A_{dB3}$		3	

	<p>Here given the voltage gains of the individual stages as ratios.</p> <p>The overall voltage gain is , $A = A_1 \times A_2 \times A_3$</p> $= 40 \times 60 \times 80 = 192\ 000$ <p>Therefore, the overall voltage gain in dB is</p> $AdB = 20 \log_{10} 192\ 000 = 105.6 \text{ dB}$	1		
II.3	 <p>At a particular frequency, when $X_L = X_C$, the circuit behaves as a purely resistive circuit. This phenomenon is called resonance and the corresponding frequency is called resonant frequency.</p> $X_L = 2\pi f r L$ $X_C = 1/2\pi f r C$ <p>At resonance frequency $f_r, X_L = X_C$</p> $2\pi f r L = 1/2\pi f r C$ <p>Therefore ,at resonance frequency $f_r = 1/2\pi(LC)^{1/2}$</p>	1	3	
II.4	<p>In power Amplifier Maximum power will be transferred to the load only if power Amplifier output is same as impedance of load. Impedance matching is achieved by transformer Coupling.</p> $R_i = (N_1/N_2)^2 \times R_L$ <p>R_L- is the load resistance, R_i- is the effective resistance looking in to the primary of transformer. By Selecting a step down transformer of proper turns ratio, maximum power output can be obtained. ie Better impedance matching can be obtained</p>	2	3	

II.5	<ul style="list-style-type: none"> As the transistor remains off for the complete negative half cycle, the power dissipation in the transistor is reduced as compared to that in the class A power amplifier, since in class A power amplifier the transistor conducts for the whole cycle. The efficiency of class B amplifiers is higher than that of the class A power amplifiers. The maximum efficiency of the class-B configuration can be 78.5% which is much higher than that of the class-A power amplifier, which have efficiency in the range 25-50% 	Any two points 1 1/2 1 1/2	3	
II.6	<p>Any three points</p> <ol style="list-style-type: none"> Gain stability $A_f = \frac{A}{1 + A\beta}$ <p>If $A\beta \gg 1$ then $A_f = 1/\beta$</p> <p>Therefore, gain depends only on feedback ratio which in turn depends on passive elements and gain is stabilized.</p> <ol style="list-style-type: none"> Reduced non-linear distortion Reduced noise Increased bandwidth 		3	
II.7	$f_o = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 100k \times 500 Pf} = 3.18kHz$		3	
II.8			3	

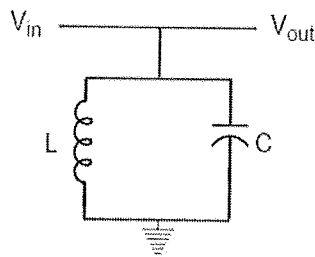
II.9	<p>Solution:</p> $T_2 = 0.69R_1C_1 = 0.69 \times 100 \times 10^3 \times 0.02 \times 10^{-6} = 1.38 \text{ ms}$ $T_1 = 0.69R_2C_2 = 0.69 \times 100 \times 10^3 \times 0.01 \times 10^{-6} = 0.69 \text{ ms}$ $T = T_1 + T_2 = 0.69 + 1.38 = 2.09 \text{ ms}$ $f = \frac{1}{T} = \frac{1}{2.09 \times 10^{-3}} = 483 \text{ Hz}$		3	
II.10	$T = RC \ln(1/1-\eta), \ln(1/1-\eta) = \ln 2 = 0.693$ <p>Now, $f_0 = 1/T$</p> $\therefore 1.5 \times 10^3 = 1/(0.693 \times 10 \times 10^3 \times C)$ $C = 0.096 \mu\text{F}$		3	
PART C				
III. 1	 <p>The emitter resistance R_E itself acts as the load and the ac output voltage V_{out} is taken across it. The biasing is provided either by base resistor method or potential divider method. When input signal V_{in} is applied to the base, the resulting emitter current I_E, develops an output voltage V_{out} equal to $I_E R_E$ across the emitter resistance R_E. It may be noted that when the input signal voltage goes through its positive half cycle, the output voltage V_{out} is also seen to go through its positive half cycle.</p> <p>The important features of Emitter Follower are – (any one)</p> <ul style="list-style-type: none"> It has high input impedance It has low output impedance It is ideal circuit for impedance matching 	3	7	7

<p>III. 2</p>	 <p>In transformer coupled amplifier using transistors the output signal of first stage is coupled to the input of the next stage through an impedance matching transformer. This type of coupling is used to match the impedance between output and input cascaded stage. Usually, it is used to match larger output resistance of AF power amplifier to a low impedance load like loudspeaker. As we know, transformer blocks dc, providing dc isolation between the two stages. Therefore, transformer coupling does not affect the quiescent point of the next stage.</p>	<p>4</p>	<p>7</p>	<p>7</p>
<p>III. 3</p>	<p>A tuned circuit can be Series tuned circuit (Series resonant circuit) or Parallel tuned circuit (parallel resonant circuit) according to the type of its connection to the main circuit.</p> <p><u>Series Tuned Circuit</u></p> <p>The inductor and capacitor connected in series make a series tuned circuit, as shown in the following circuit diagram.</p>  <p>At resonant frequency, a series resonant circuit offers low impedance which allows high current through it. A series resonant circuit offers increasingly high impedance to the</p>	<p>1</p> <p>2</p>	<p>7</p>	<p>7</p>

frequencies far from the resonant frequency.

Parallel Tuned Circuit

The inductor and capacitor connected in parallel make a parallel tuned circuit, as shown in the below figure.



At resonant frequency, a parallel resonant circuit offers high impedance which does not allow high current through it. A parallel resonant circuit offers increasingly low impedance to the frequencies far from the resonant frequency.

Solution:

$$F = 1/2\pi\sqrt{LC}$$

$$= 1/2 \times 3.14 \times \sqrt{2 \times 10^{-6} \times 100 \times 10^{-6}} = 11.26 \text{ kHz}$$

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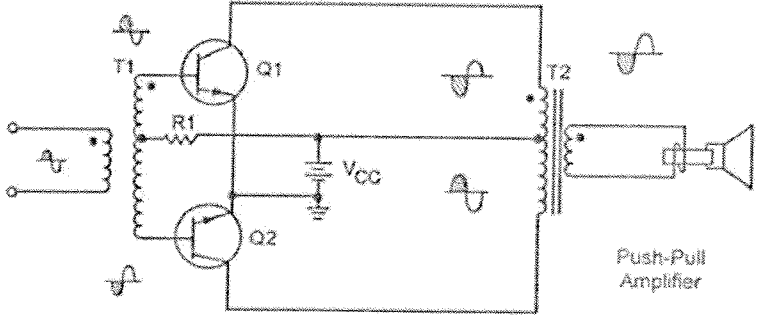
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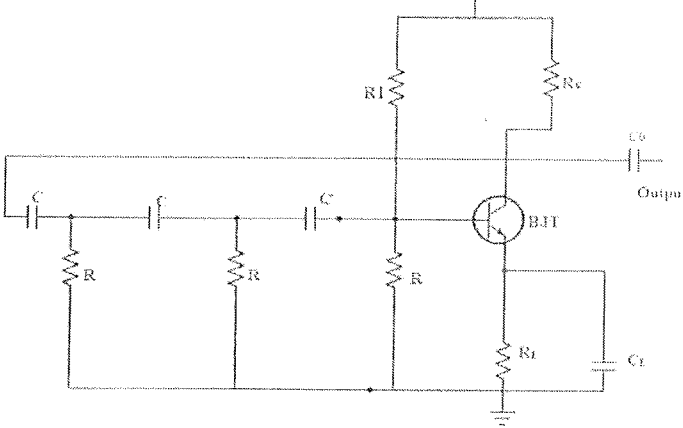
III. 4 **Class A** power amplifier- the collector current flows at all times during the full cycle of the signal.
Class B power amplifier- the collector current flows only during the positive half cycle of the input signal
Class C power amplifier- the collector current flows for less than half cycle of the input signal
Class AB Amplifier- This action is achieved by pre-biasing the two transistors in the amplifiers output stage. Then each transistor will conduct between 180° and 360° of the time depending on the amount of current output and pre-biasing. Thus the amplifier output stage operates as a Class AB amplifier.

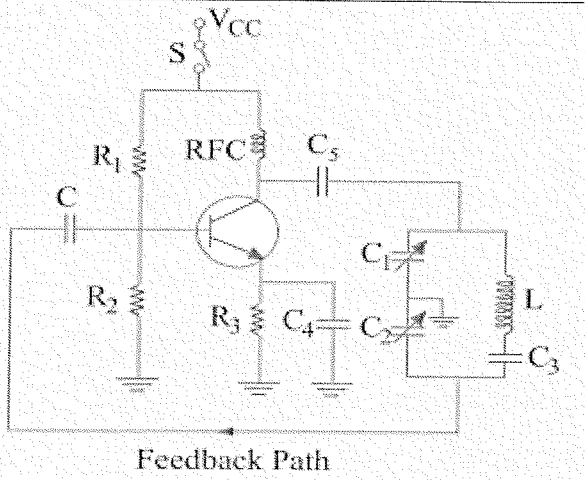
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III. 5	<p>Voltage amplifier</p> <p>Low current gain</p> <p>Very high collector load</p> <p>Low input voltage requirement</p> <p>Low power output</p> <p>Less power dissipation capacity</p> <p>High output impedance</p> <p>RC coupling is used</p> <p>Doesn't need cooling arrangement</p>	<p>Power amplifier</p> <p>High current gain</p> <p>Very low collector load</p> <p>High input voltage requirement</p> <p>high power output</p> <p>high power dissipation capacity</p> <p>low output impedance</p> <p>transformer coupling is used</p> <p>need cooling arrangement</p>	Any 7 points	7	7
III. 6	<p>The construction of the class B power amplifier circuit in push-pull configuration is shown as in the figure below. This arrangement mainly reduces the harmonic distortion introduced by the non-linearity of the transfer characteristics of a single transistor amplifier.</p> <p>In Push-pull arrangement, the two identical transistors T1 and T2, have their emitter terminals shorted. The input signal is applied to the transistors through the transformer T₁, which provides opposite polarity signals to both the transistor bases. The collectors of both the transistors are connected to the primary of output transformer T₂. Both the transformers are center tapped. The V_{CC} supply is provided to the collectors of both the transistors through the primary of the output transformer.</p>		3	7	7
			4		

<p>III. 7</p>	<p>Solution.</p> $f_o = \frac{1}{2\pi RC\sqrt{6}}$ <p>or</p> $R = \frac{1}{2\pi f_o C\sqrt{6}} = \frac{1}{2\pi \times 800 \times 10^3 \times 5 \times 10^{-12} \times \sqrt{6}}$ $= 16.2 \times 10^3 \Omega = 16.2 \text{ k}\Omega$ 	<p>4</p>	<p>3</p>	<p>7</p>
<p>III. 8</p>	<p>Solution.</p> $L_1 = 58.6 \mu\text{H} = 58.6 \times 10^{-6} \text{ H}$ $C_1 = 300 \text{ pF} = 300 \times 10^{-12} \text{ F}$ <p>Frequency of oscillations, $f = \frac{1}{2\pi\sqrt{L_1 C_1}}$</p> $= \frac{1}{2\pi\sqrt{58.6 \times 10^{-6} \times 300 \times 10^{-12}}} \text{ Hz}$ $= 1199 \times 10^3 \text{ Hz} = 1199 \text{ kHz}$	<p>2</p> <p>3</p> <p>2</p>	<p>7</p>	<p>7</p>
<p>III. 9</p>	<p>Colpitts oscillator uses tapped capacitance. The two series capacitors C1 and C2 form the voltage divider used for providing the feedback voltage (the voltage drop across C2 constitutes the feedback voltage). The feedback factor is C1/C2.</p>	<p>7</p>	<p>7</p>	<p>7</p>



4

The tank circuit consists of two ganged capacitors C1 and C2 and a single fixed coil. The frequency of oscillation is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad \text{where} \quad C = \frac{C_1 C_2}{C_1 + C_2}$$

3

Transistor itself produces a phase shift of 180°. Another phase shift of 180° is provided by the capacitive feedback thus giving a total phase shift of 360° between the emitter-base and collector-base circuits. Resistors R1 and R2 form a voltage divider across VCC for providing base bias, R3 is for emitter stabilisation and RFC provides the necessary dc load resistance RC for amplifier action. It also prevents ac signal from entering supply dc VCC. Capacitor C5 is a bypass capacitor whereas C4 conveys feedback from the collector-to-base circuit

III. 10 A portion of the output signal is taken from the output of the amplifier and is combined with the normal input signal. This is known as feedback.

2

Positive feedback	Negative feedback
1. The feedback signal is in same phase with the input signal. 2. Also called regenerative feedback.	1. The feedback signal is in phase opposition or 180 out of phase with the input signal. 2. Also called degenerative feedback.

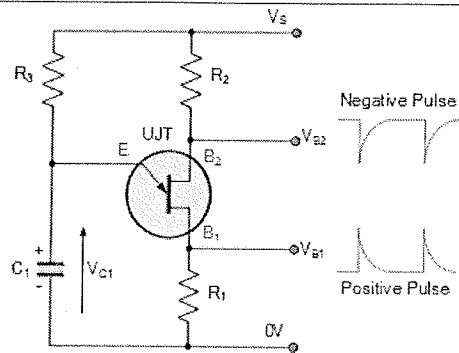
Any 5 points

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	<p>3. It increases the net input to the amplifier.</p> <p>4. It increases the gain of the amplifier.</p> <p>5. It increases the noise and distortion.</p> <p>6. It decreases the stability of amplifier gain.</p> <p>7. Used in oscillator circuits.</p>	<p>3. It reduces the net input to the amplifier.</p> <p>4. It reduces the gain of the amplifier.</p> <p>5. It reduces the noise and distortion.</p> <p>6. It improves the stability of amplifier gain.</p> <p>7. Used in amplifier circuits.</p>				
<p>III. 11</p>			<p>4</p>	<p>7</p>	<p>7</p>	
		<p>3</p>				

III. 12



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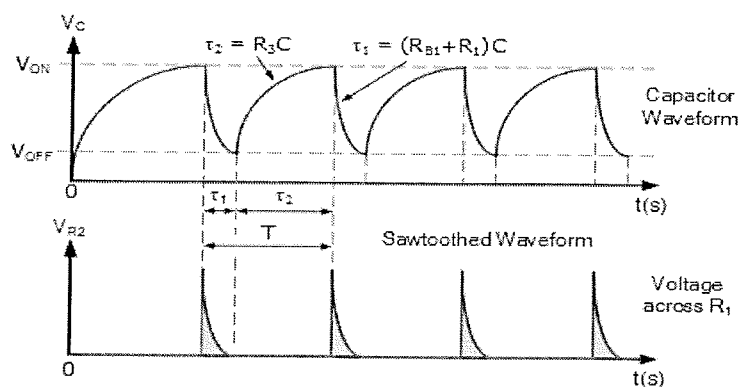
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When a voltage (V_s) is applied, the capacitor C_1 begins to charge up exponentially through resistor R_3 . When the charging voltage V_c across the capacitor becomes greater than the diode volt drop value trigger the UJT into conduction. The unijunction transistor is "ON". Emitter current flows through R_1 .

3

As the ohmic value of resistor R_1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R_1 . When the voltage across the capacitor decreases below the valley point once again the capacitor charges up through resistor R_3 and this charging and discharging process between V_{ON} and V_{OFF} is constantly repeated while there is a supply voltage, V_s applied.



1

Time period of oscillation, $T = RC \ln(1/(1-\eta))$

Decision taken by the JCTE Office on 01.01.2025 based on the complaints received from the students of various Polytechnic Colleges in connection with the Question papers of Diploma Examination November 2024 and recommendations of expert committee.

1. Subject Code :-3025

R (21)	3025 Machine Drawing	An ambiguity occurred in Part A Questions, ie answer any one of the questions instead of any two	15 marks each
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Decision:-

- * If the students have attended two questions , I(1) or I(2) and I(3) or I(4) from Part A, then value the two answers.
- * If the students have attended only one question from Part A,
 - (a) The marks secured will be considered as out of 60
 - (b) The Percentage of marks secured out of 60 shall be calculated and the same percentage of marks out of 15 shall also be added to the marks secured to arrive at the actual marks admissible out of 75.

2. Subject Code :-3341

R(21)	3341 Discrete Mathematics	Part A -6,7,8,9 Part B-6,7,8,10 Part C- IX,X,XI,XII	1 Mark each 3 Marks each 7 Marks each
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Decision:-

- * Questions 6,7,8 & 9 of Part A , 6,7,8 & 10 of Part B and IX,X,XI and XII of Part C are cancelled.
- Value the remaining questions.
- * Part B -Consider the marks of 4 highest scored questions out of remaining 6 questions.

- * The marks secured will be considered as out of 45
- * The percentage of marks secured out of 45 shall be calculated and the same percentage of marks out of 30 shall also be added to the marks secured to arrive at the actual marks admissible out of 75.

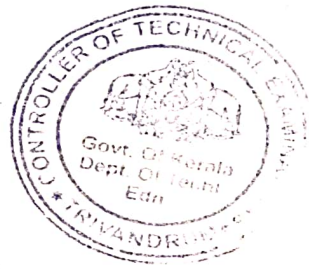
3. Subject Code :-3043


R(21)	3043 Electronic Circuits	Part B -3,9	3 Marks each
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Decision:-

Part B

- * Question No: 3 and 9 are cancelled
- * Consider the marks of 6 highest scored questions out of remaining 8 questions
- * Marks secured will be considered as out of 69
- * The percentage of marks secured out of 69 shall be calculated and the same percentage of marks out of 6 shall also be added to the marks secured to arrive at the actual marks admissible out of 75.




V.V Ray
Joint Controller
Joint Controller of
Technical Examinations