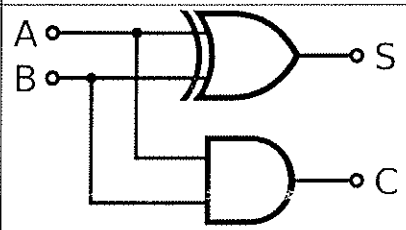
ScoringIndicators

COURSENAME: DIGITAL ELECTRONICS

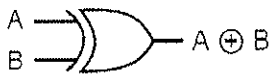
COURSECODE: 3044 QID: 2110220231

QNo	ScoringIndicators	Split score	Sub Tota L	Total score
	PARTA			**9**
I.1	1111	1	1	
I.2	11011101	1	1	
I.3	universal	1	1	
I.4	Very large scale integration	1	1	
I.5		1	1	
I.6	TWO	1	1	
I.7	Preset and Clear	1	1	
I.8	Ripple counters	1	1	
I.9	EEPROM	1	1	
	PARTB			24
II.1	10100	3	3	

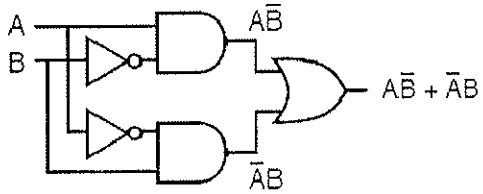
II.2

A	B	$A \oplus B$	$\bar{A}$	$\bar{B}$	$A\bar{B}$	$\bar{A}B$	$A\bar{B} + \bar{A}B$
0	0	0	1	1	0	0	0
0	1	1	1	0	0	1	1
1	0	1	0	1	1	0	1
1	1	0	0	0	0	0	0

1.5+1.5 | 3



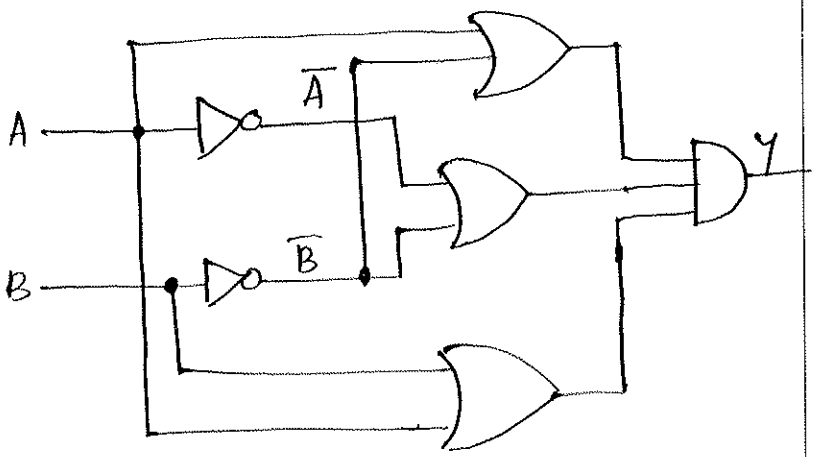
. . . is equivalent to . .



$A \oplus B = A\bar{B} + \bar{A}B$

II.3

3 | 3

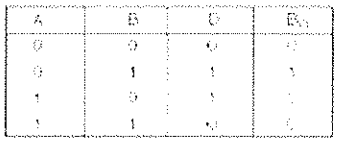
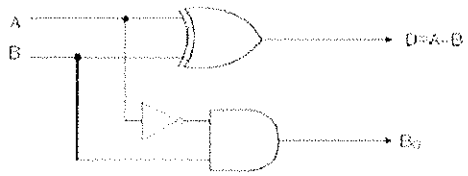
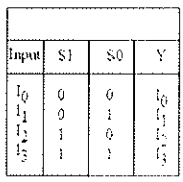
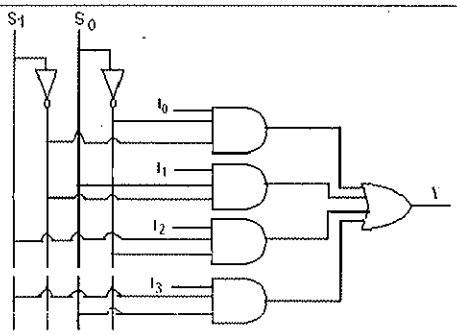
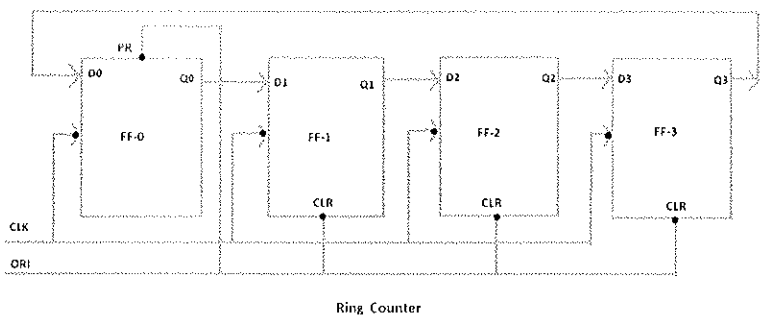


II.4

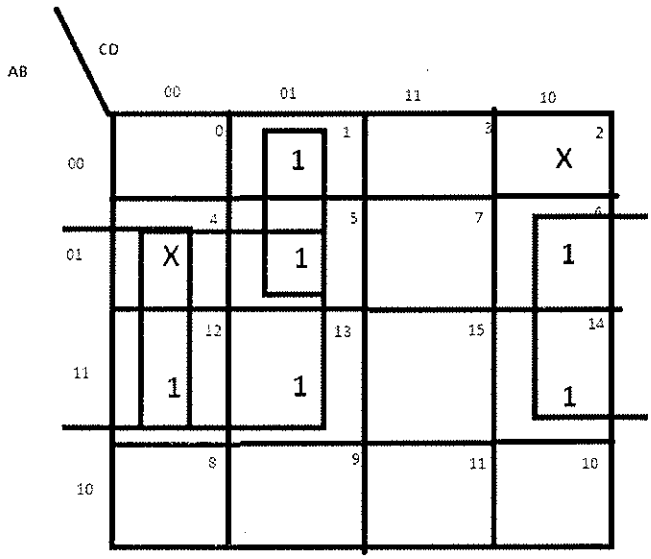
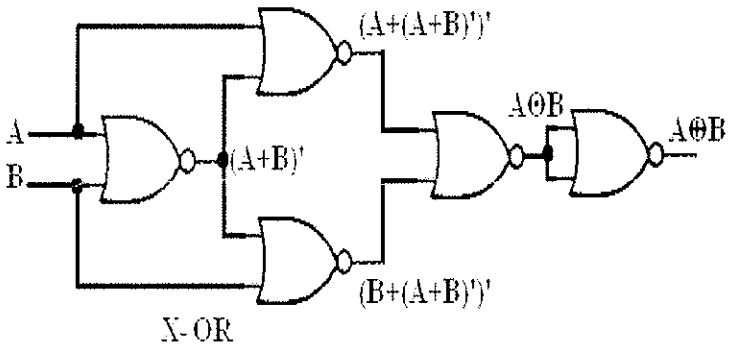
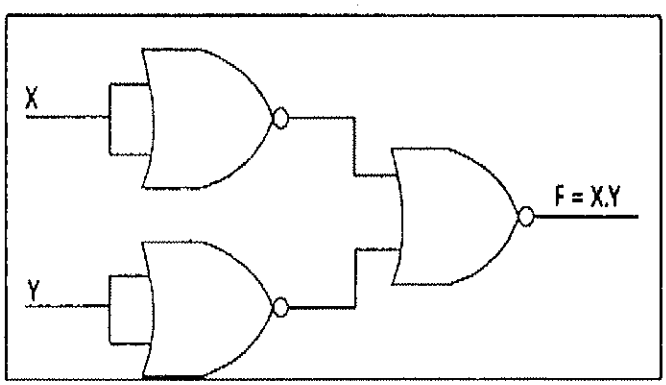
a) The fan-in of a logic gate is defined as the number of inputs that the gate is designed to handle.

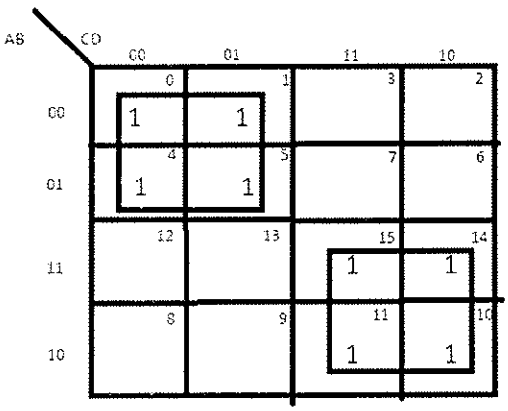
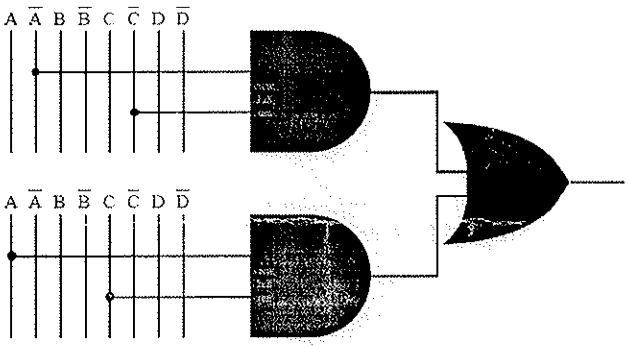
b) The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise voltages at its inputs. A quantitative measure of noise immunity is called noise margin.

1.5+1.5 | 3

II.5	$D = \overline{A}B + A\overline{B}$ $B_o = \overline{A}B$   Half Subtractor  	Truth table- 1mark+ Equation- 1mark+ logic diagram -1 mark	3	
II.6	 $Y = S_1S_0I_3 + S_1\overline{S}_0I_2 + \overline{S}_1S_0I_1 + \overline{S}_1\overline{S}_0I_0$  	1+ 2	3	
II.7	Combinational logic circuits	Sequential logic circuits	1.5+ 1.5	3	
	1. Output level at any instant of time are dependent only on the levels present at the inputs at that time.	Output level at any instant of time are dependent not only on the levels present at the inputs at that time, but also on the prior input level conditions.			
	2. Have no memory	Have memory			
II.8	 Ring Counter	3	3	

II.9	The number of states through which the counter passes before returning to the starting state is called the modulus of the counter. Number of states in a mod-4counter is 4.	2+ 1	3	
II.10	<table><tr><th>RAM</th><th>ROM</th></tr><tr><td>1. RAM is random access memory</td><td>ROM is read only memory</td></tr><tr><td>2. RAM is a volatile memory which could store the data as long as the power is supplied</td><td>ROM is a non-volatile memory which could retain the data even when power is turned off</td></tr><tr><td>3. Data stored in RAM can be retrieved and altered.</td><td>Data stored in ROM can only be read.</td></tr></table>	1+ 1+ 1	3	
	PART C			**42**
III. 1	a) 69_{16} -43_{16}=01101001+ 10111101 =100100110 = 26_{16} (ignore carry) Carry is 1. Carry indicates result obtained is positive and is in hex itself. 69_{16} -43_{16}=26_{16} b) 27_{16}-73_{16}=00100111+ 10001101 =10110100 =B4 (no carry) No carry indicates that the answer is negative and is in its 2's complement form. The 2's complement of B4 is 4C. Therefore the final result is – $4C_{16}$ 27_{16}-73_{16} = – $4C_{16}$	3.5+ 3.5	7	7

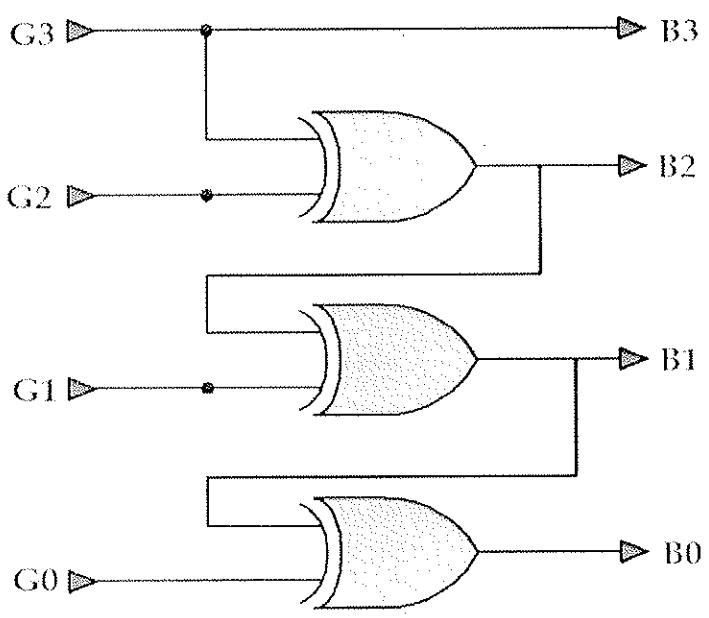
III. 2	 $f = B\bar{C} + B\bar{D} + \bar{A}\bar{C}\,D$	K map 5+ Answer 2	7	7
III. 3	EX-OR gate  X-OR AND gate 	3.5+ 3.5	7	

III. 4	$F = \sum m\,(0,\ 1,\ 4,\ 5,\ 10,\ 11,\ 14,\ 15)$  $F = AC + \bar{A}\bar{C}$ 	K-map 3+ Minimized function 2+ Logic diagram 2	7	

III. 5									Truth table 2+ K map and equation 3+ Logic diagram 2	7	7

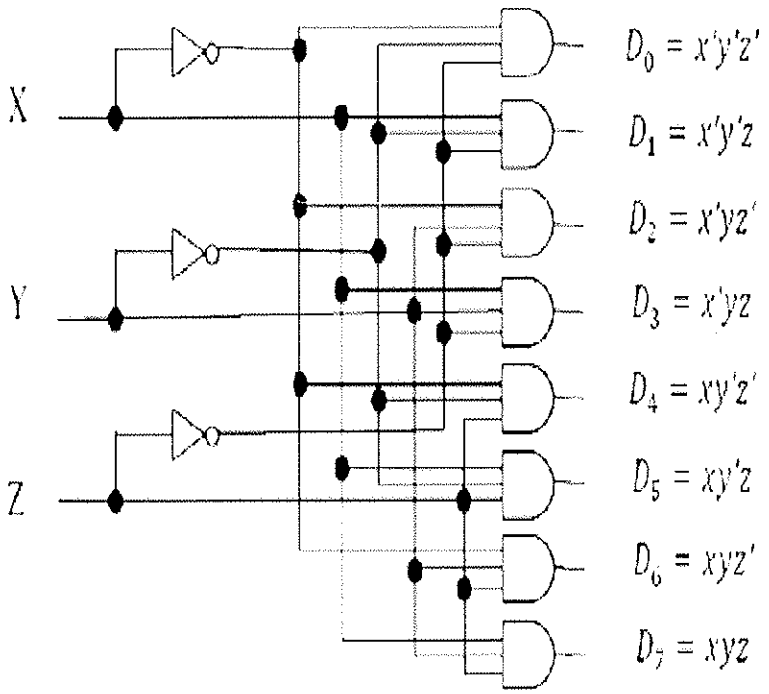
Gray Code Input				Binary Code Output			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Draw k map for B3,B2,B1,B0



III. 6

Inputs			Outputs							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

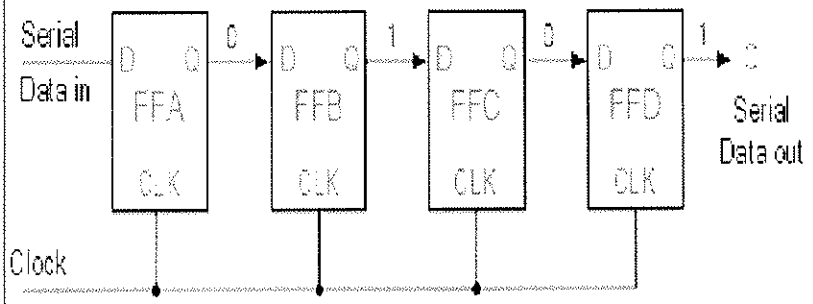
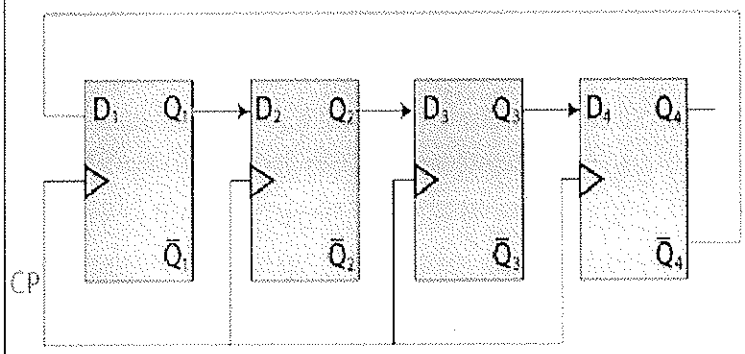


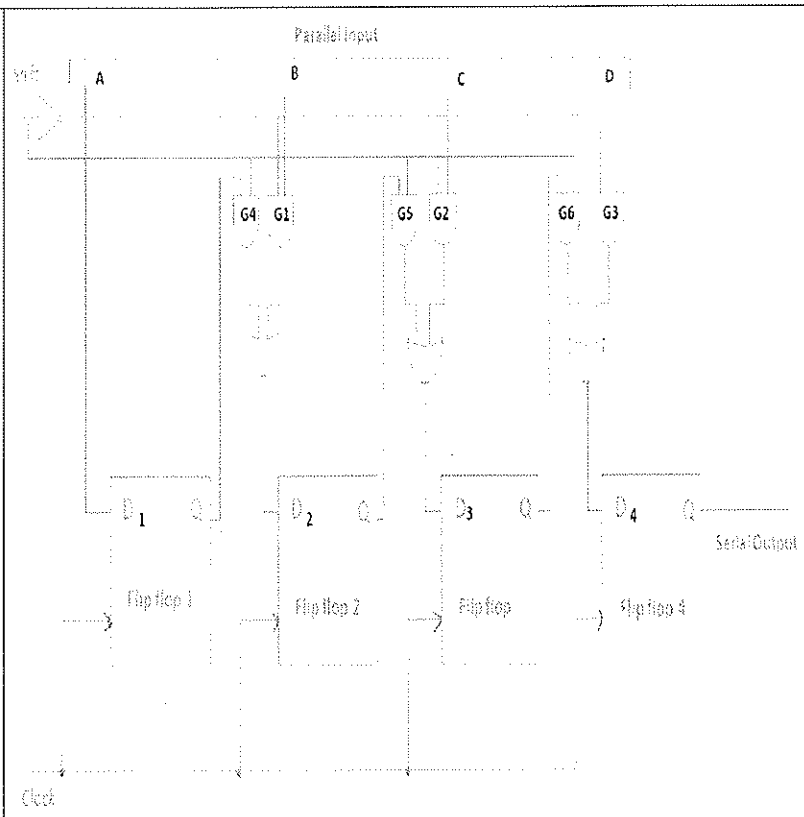
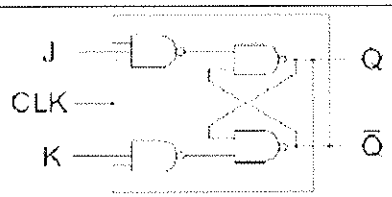
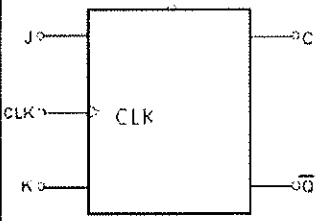
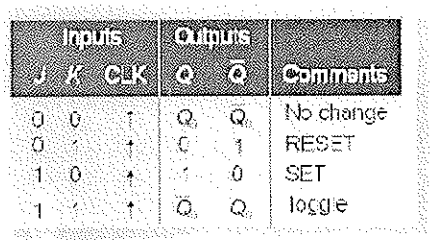
Decoder has 3 inputs and 8 outputs. It uses all AND gates and therefore outputs are active high.

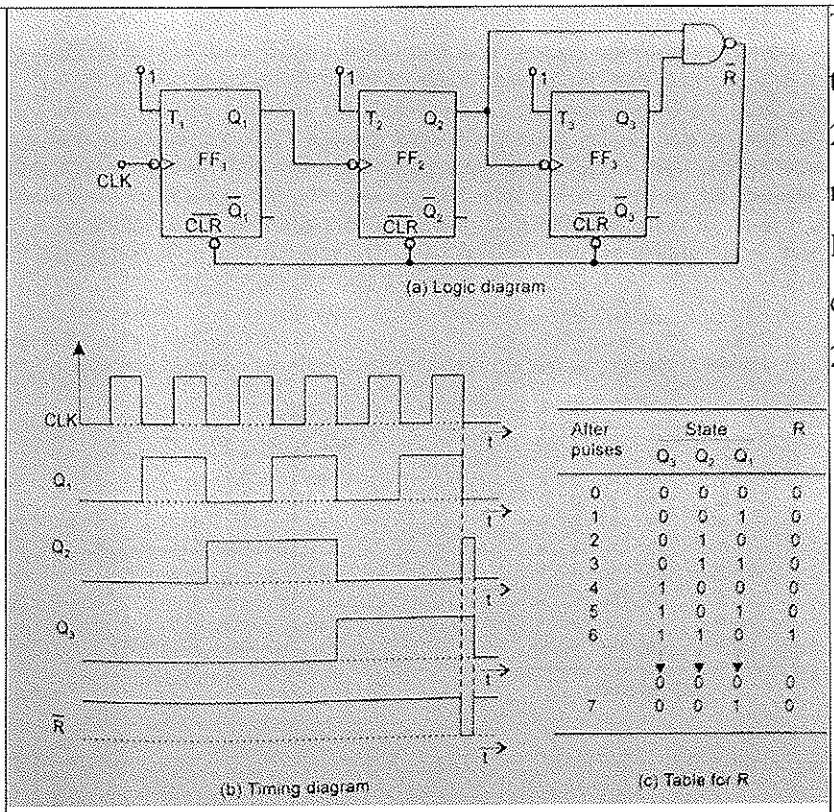
Truth table 2+ Logic diagram 3+ Explanatin 2

7

7

III. 7	 Explain with an example (input binary sequence)	Logic diagram 3+ Explan 4	7	7
III. 8	Johnson counter is obtained from a serial-in serial-out shift register by providing a feedback from the inverted output of the last flip flop to the D input of the first flip flop.  	CP	Q1	Q2	Q3	Q4
0	1	0	0	0
1	0	0	0	0
2	0	1	0	0
3	0	1	1	0
4	0	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	1	0	0	0		Logic diagram -3+ Sequence table 2+ Expln 2	7	7

III. 9		Logic diagram 4+explanation 3	7	7
III. 10	  Logic symbol  Truth table	Circuit 4+truth table 1+explanation 2	7	7

III. 11	 A mod 6 counter has six stable states 000, 001, 010, 011, 100, and 101. When the sixth clock pulse is applied the counter temporarily goes to 110 state, but immediately resets to 000 because of the feedback provided. It requires 3 flipflops. For active low reset $\bar{R}$ is used. R= 0 for 000 to 101 R= 1 for 110 And R=X for 111 $R = Q_3Q_2\bar{Q}_1 + Q_3Q_2Q_1 = Q_3Q_2$	Truth table - 2+design 3+ Logic diagram 2	7	7

III. 12	RAM is random access memory. The information stored in this type of memory is lost when the power supply is switched OFF. It is the volatile memory. Types of RAM 1. Static RAM (SRAM) Memory cells are flip flops that will stay in given state indefinitely provided that power to the circuit is not interrupted 2. Dynamic RAM(DRAM) Store data as charges on capacitors. The stored data will gradually disappear because of capacitor discharge, therefore it is necessary to periodically refresh the data(recharge the capacitors) 3. SDRAM(synchronous dynamic RAM) Are synchronized with the clock speed that the microprocessor is optimized for. 4. DDRAM(double data rate synchronous DRAM) Supports data transfers on both edges of each clock cycle. doubling the memory chip's data throughput, consumes less power	1+ 2+ 2+ 2	7	7