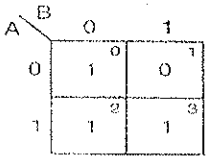
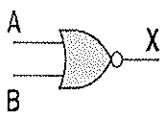
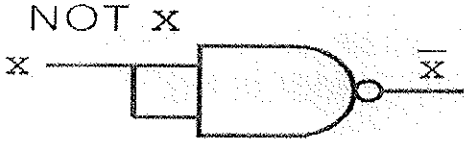
Scoring Indicators

Course Name:Digital Computer Fundamentals
Course Code:3134 **QID :**

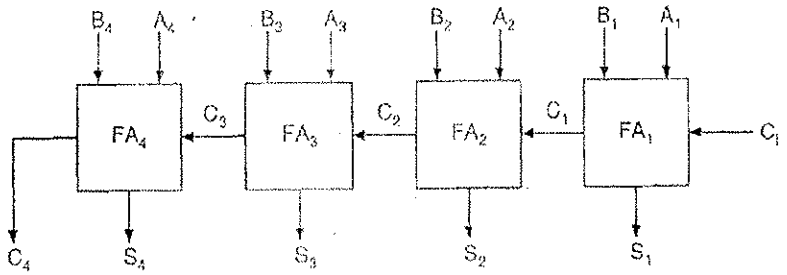
Q. No.	Scoring Indicators	Split score	Sub Total	Total score
	PART A			9
I.1	8		1	
I.2	0010		1	
I.3	0		1	
I.4	0		1	
I.5	1		1	
I.6	1011		1	
I.7	False		1	
I.8	True		1	
I.9	4		1	
	PART B			24
II.1	173	3	3	
II.2	Error detecting and error correcting codes: When data transmitted through a channel, due to noise they may be get corrupted Error detection and correcting codes are used to detect and correct errors, eg: hamming code	3	3	
II.3		3	3	
II.4	Logic Diagram Symbol  Truth Table A B X 0 0 1 0 1 0 1 0 0 1 1 0	TT 1.5 Symbol 1.5	3	
II.5	NOT x  Short the inputs	1.5 1.5	3	
II.6	Law 1 $\overline{A+B} = \overline{A}\,\overline{B}$	1.5 1.5 proof	3	

A	B	A+B	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

=

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}$ $\overline{B}$
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

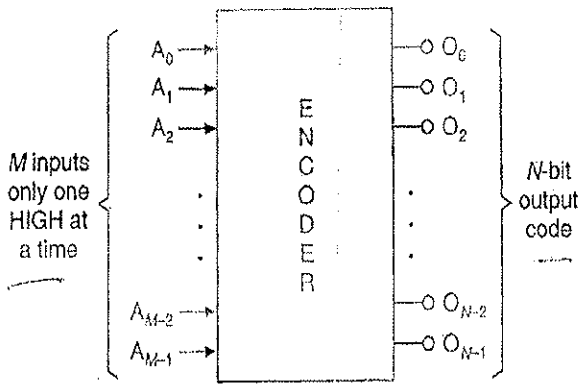
II.7



3

3

II.8



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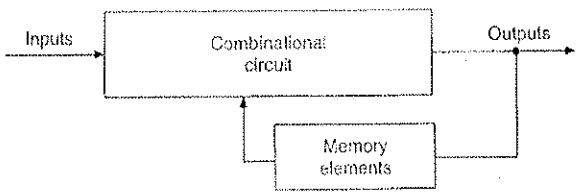
1.5

1.5

- It has a number of input lines
- One of which is activated at a given time
- It produces N-bit output code depending on the input line selected/activated

II.9



3

1.5

- In sequential logic circuit, the out depends up on the state of the logic circuit. 1.5
- It depends upon both the input as well as the previous output of the circuit.

Examples: Latches, Flip flops, counters, registers etc.

II.10

- When j =1 k = 1 and clk = 1; Q output will toggle as long as CLK is high. 3
- Thus the output will be unstable creating a race-around problem with this basic JK circuit.
- This problem is avoided by ensuring that the clock input is at logic "1" only for a very short time,

PART C

42

III.1 a)119 3.5 7

b)(7E3)16 3.5

III.2 Solution: 2's complement of 11001 with 6 bit is (100110 + 1) i.e. 100111. Hence

Minuend - 101011

2's complement of subtrahend - 100111

Result of addition - 010010 with carry

After dropping the carry we get the result of subtraction to be **010010**.

2's comp 2M
Width adjust 1M
Add 3M
Carry ignore 1M

7

III.3

The given expression is	$f = A[B + \bar{C}(\overline{AB + A\bar{C}})]$
Demorganize $\overline{AB + A\bar{C}}$	$= A[B + \bar{C}(\overline{AB}\,\overline{A\bar{C}})]$
Demorganize $\overline{AB}$ and $\overline{A\bar{C}}$	$= A[B + \bar{C}(\bar{A} + \bar{B})(\bar{A} + C)]$
Multiply $(\bar{A} + \bar{B})(\bar{A} + C)$	$= A[B + \bar{C}(\bar{A}\bar{A} + \bar{A}C + \bar{B}\bar{A} + \bar{B}C)]$
Simplify	$= A(B + \bar{C}\bar{A} + \bar{C}\bar{A}C + \bar{C}\bar{B}\bar{A} + \bar{C}\bar{B}C)$
Simplify	$= A(B + \bar{C}\bar{A} + 0 + \bar{C}\bar{B}\bar{A} + 0)$
Simplify	$= AB + A\bar{C}\bar{A} + A\bar{C}\bar{B}\bar{A}$
Simplify	$= AB + 0 + 0$
Simplify	$= AB$

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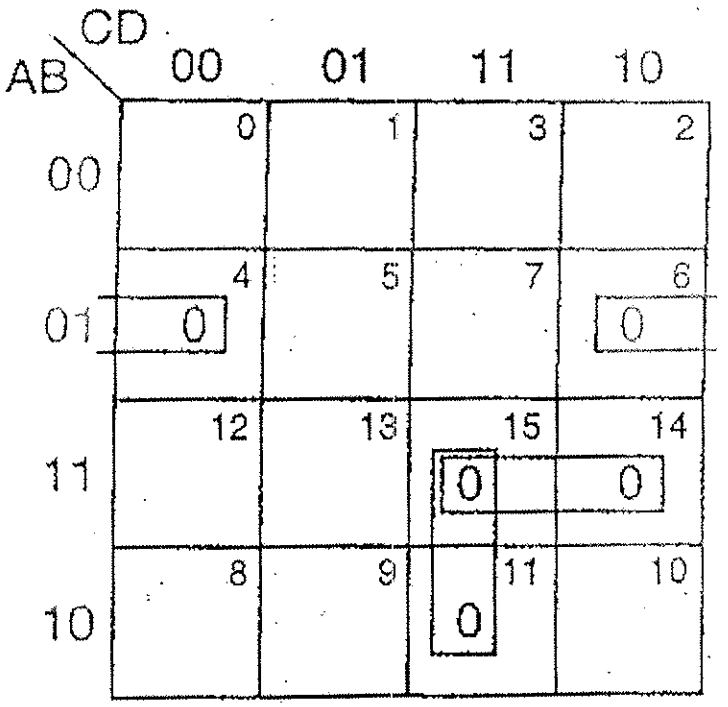
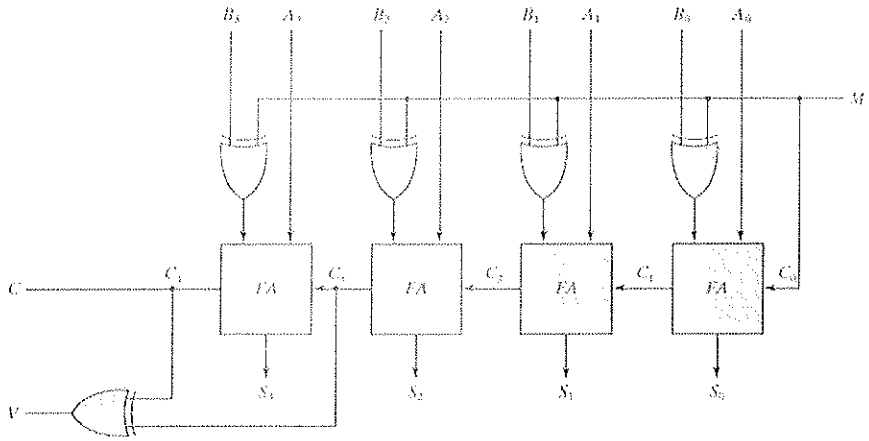
III.4



$f_{min} = (A + \bar{B} + D)(\bar{A} + \bar{C} + \bar{D})(\bar{A} + \bar{B} + \bar{C})$

7

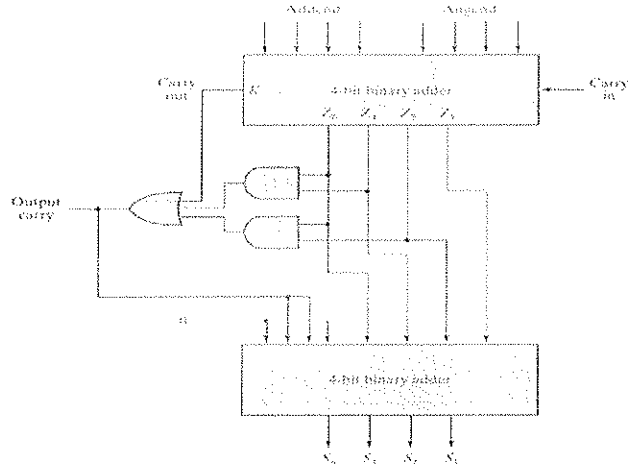
III.5 7



3.5

- The subtraction A - B can be done by taking the 2's complement of B and adding it to A . 3.5
- The 2's complement can be obtained by taking the 1's complement and adding 1
- The 1's complement can be implemented with inverters, and a 1 can be added to the sum through the input carry
- The input carry C0 must be equal to 1 when subtraction is performed
- If M=0 is adder and M=1 is subtractor

III.6 7



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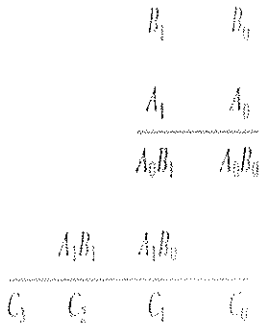
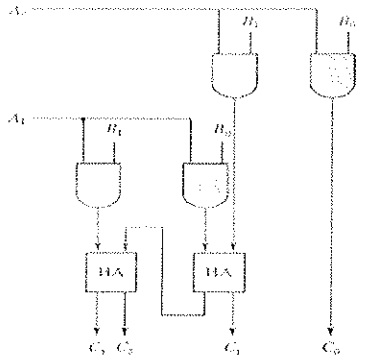
- A correction is needed when the binary sum has an output carry k=0 Expl 3
- The combinations 1010 to 1111 also need a correction.
- The condition for a correction and output carry can be expressed C= K+Z8Z4+Z8Z2
- When c is 1, a 0110 is added to the binary sum

III.7 7



3.5



3.5

III.8 A combinational circuit that performs the addition of two bits is called a half adder. 7

The truth table for the half adder is listed below 1

it has two inputs X and Y

it has two out puts Sum and Carry out

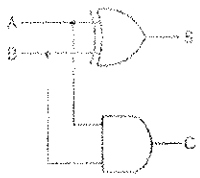
Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2

1

$S = A\bar{B} + \bar{A}B = A \oplus B$

$C = AB$



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III.9 7

Combinational circuits	Sequential circuits
1. In combinational circuits, the output variables at any instant of time are dependent only on the present input variables.	1. In sequential circuits, the output variables at any instant of time are dependent not only on the present input variables, but also on the present state, i.e. on the past history of the system.
2. Memory unit is not required in combinational circuits.	2. Memory unit is required to store the past history of the input variables in sequential circuits.
3. Combinational circuits are faster because the delay between the input and the output is due to propagation delay of gates only.	3. Sequential circuits are slower than combinational circuits.
4. Combinational circuits are easy to design.	4. Sequential circuits are comparatively harder to design.

3.5

3.5

III.10

Synchronous sequential circuits	Asynchronous sequential circuits
1. In synchronous circuits, memory elements are clocked FFs.	1. In asynchronous circuits, memory elements are either unclocked FFs or time delay elements.
2. In synchronous circuits, the change in input signals can affect memory elements upon activation of clock signal.	2. In asynchronous circuits, change in input signals can affect memory elements at any instant of time.
3. The maximum operating speed of the clock depends on time delays involved.	3. Because of the absence of the clock, asynchronous circuits can operate faster than synchronous circuits.
4. Easier to design.	4. More difficult to design.

3.5
3.5

7

III.11 Serial In / Serial Out Shift Registers (SISO)
Serial In /Parallel Out Shift Registers (SIPO)
Parallel In / Serial Out Shift Registers (PISO)
Parallel In / Parallel Out Shift Registers (PIPO)

Any 3
(3*2)
(exp1+fig1)
+
List 1m

7

III.12

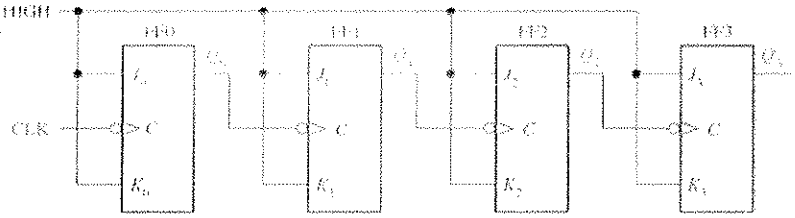

Fig 5M
Expl 2M

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