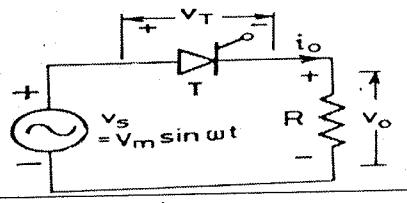
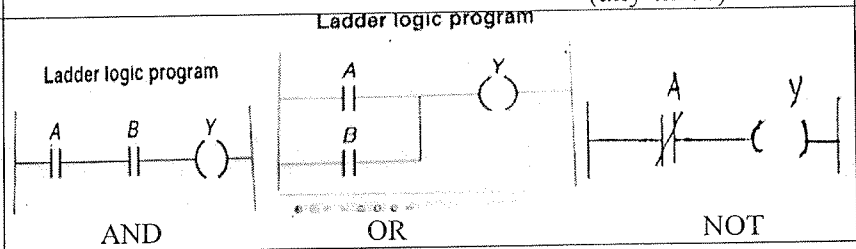
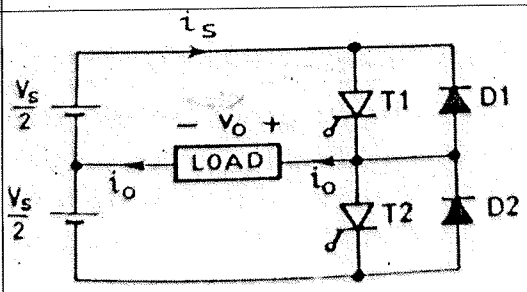
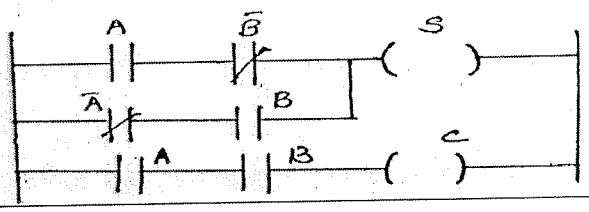
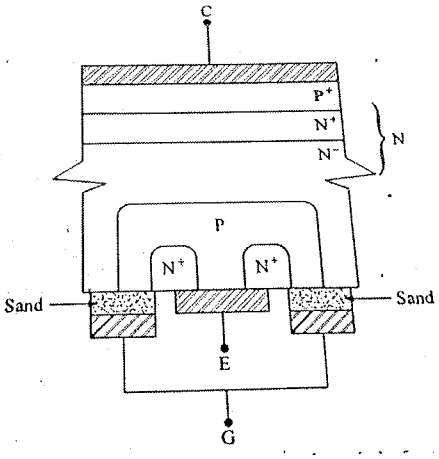
Scoring Indicators

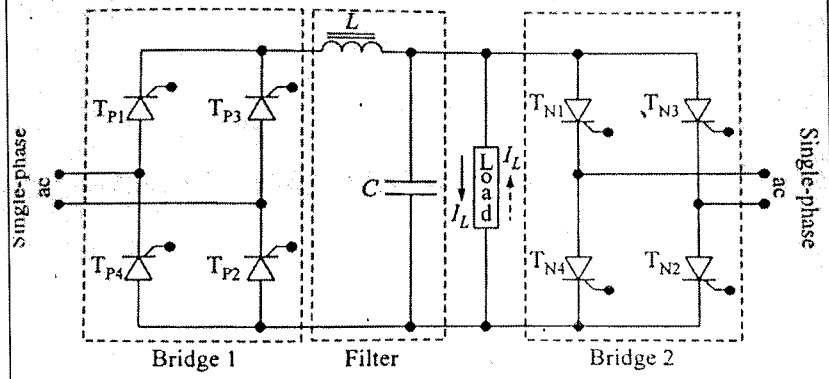
COURSE NAME: INDUSTRIAL AUTOMATION

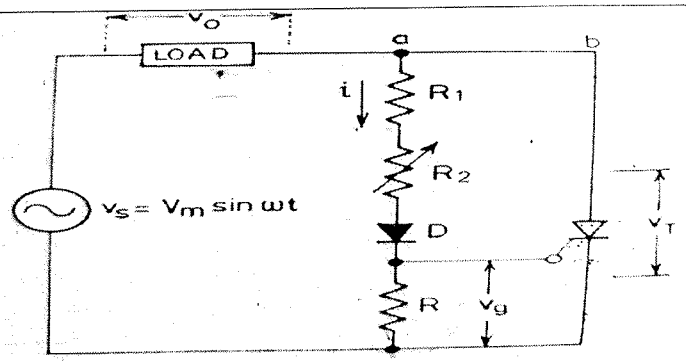
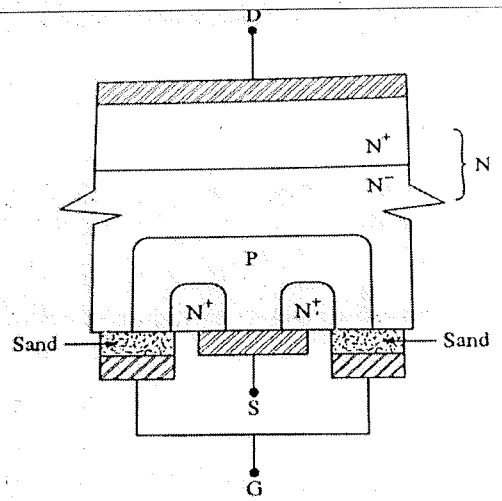
COURSE CODE: 5042 **QID: 2109230086**

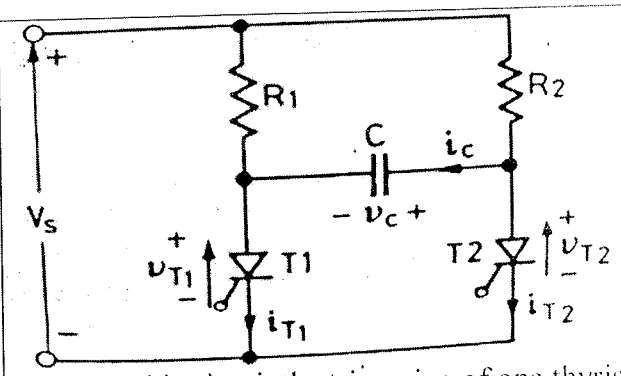
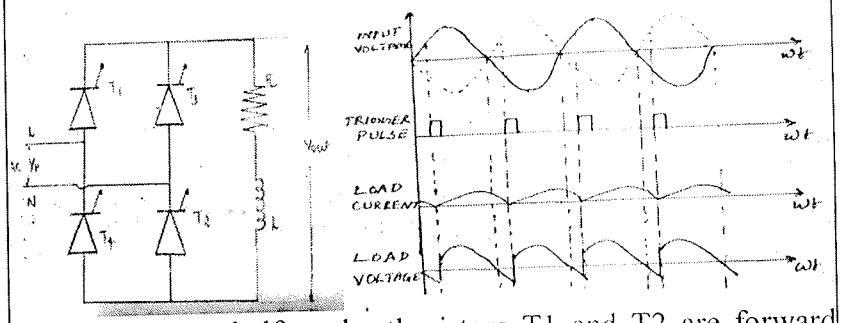
Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			**9**
I. 1	Three		1	
I. 2	Cycloconverter		1	
I. 3	Heat is concentrated near the surface, Rate of heating is high, less wastage of heat, Heat can be controlled accurately, can be done in vacuum or any gas, unskilled persons may operate. (any two)	1/2 * 2	1	
I. 4	Programmable Logic Controller		1	
I. 5	Squeeze time		1	
I. 6	90°		1	
I. 7	Domestic and Industrial heating, lighting control, speed control of single phase and three phase ac drives, starting of induction motors. (any two)	1/2 * 2	1	
I. 8	Electric Drive		1	
I. 9	Increased reliability, More flexibility, lower cost, Faster response, Wiring can be reduced by 80% (any two)	1/2 * 2	1	
	PART B			24
II. 1	**Latching current (IL)**:-Minimum anode current required to maintain the SCR in ON state after the thyristor has been turned on and removes the gate signal. **Holding current (IH)**:- Minimum anode current below which the SCR stops conducting and returns to its OFF state.	1 ½ *2	3	
II. 2			3	
II. 3	Induction heating 1. Caused by eddy current loss Dielectric heating 1. Depends on electrostatic effect	1*3	3	

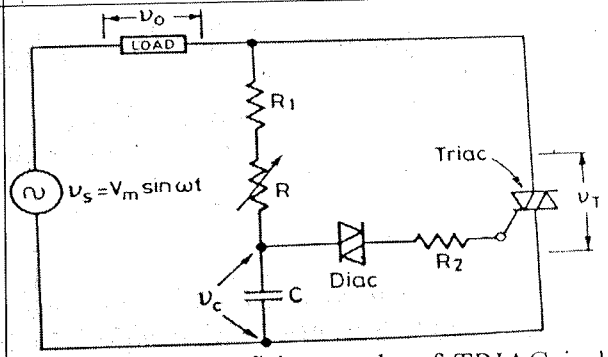
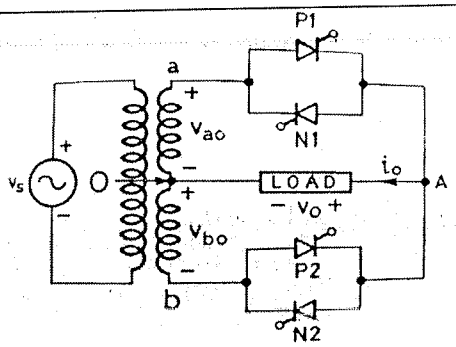
	2. Operating frequency 200KHz -500Khz 3. Surface heating 4. Equipment cost is low 5. Used to heat metals	2. Operating frequency 1MHz-50 MHz 3. Volume heating 4. High 5. To heat non metallic items. (any three)		
II. 4				3
II. 5	**NATURAL COMMUTATION** When a thyristor is used in AC circuits the natural commutation takes place. As the current passes through its natural zero, the current through the SCR also reaches zero. Therefore the device goes to off state. This commutation is automatic and is natural. **FORCED COMMUTATION** In DC applications, there cannot be any zero crossing due to unidirectional characteristics of DC. So forced commutation is needed there. The external circuit used for forced commutation is called commutation circuit and the components used in commutation circuit are called commutating components.			3
II. 6	 A single phase half bridge inverter consists of two SCRs, two diodes and three wire supply. For $0< t < T/2$, thyristor T1 conducts and the load is subjected to a voltage Vs/2 due to the upper source. At t=T/2, thyristor T1 is commutated and T2 is gated ON. During the period $T/2 < t < T$, thyristor T2 conducts and the load is subjected to a voltage –Vs/2 due to the lower voltage source Vs/2.	1 1/2 1 1/2	3	
II. 7	In electric resistance welding, two or more pieces of metals are fused together by ac or dc current of high value that flows for a short duration through the area of contact. The heat is produced by the resistance offered to the flow of the current at the junction of the two metals. **TYPES OF ELECTRIC RESISTANCE WELDING** SPOT WELDING, SEAM WELDING, BUTT WELDING, FLASH BUTT WELDING, PROJECTION WELDING	1 2	3	

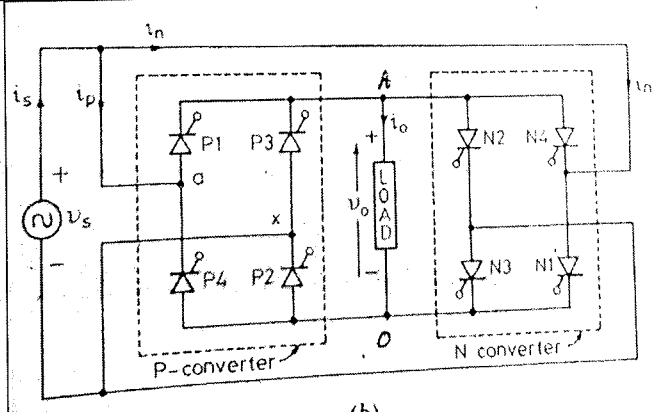
II. 8	SUM = $A\bar{B} + \bar{A}B$ C = AB  		3	
II.9	 The outer P^+ layer forms the collector of the IGBT. The adjacent N region consist of N^+ layer and an N^- layer. Adjacent to the N region is a relatively large P island. Inside the P island are again N^+ islands.The collector and emitter are the power terminals of IGBT. The switching control voltage is applied across the gate and the emitter.	1 1/2 1 1/2	3	

II.10			3	
	PART C			42
III	**TRIGGERING METHODS OF SCR** When a thyristor is switched in to ON state, it is said to be fired or triggered. Some of the methods that can be used to trigger a thyristor are - Forward voltage triggering, Gate triggering, dv/dt triggering, Temperature triggering, Light triggering. **Forward voltage triggering** When anode to cathode forward voltage is increased with gate circuit open, reverse biased junction J2 will break due to avalanche breakdown at the break over voltage. At this voltage thyristor changes from OFF state to ON state. **Gate triggering** Application of a positive voltage to the gate terminal of the thyristor with respect to the cathode can trigger the SCR. Higher the gate current, lower is the break over voltage. **dv/dt triggering** With forward voltage across the anode and cathode of the thyristor, space charges exist in the depletion region near reverse biased junction J2 and therefore junction J2 behaves like a capacitance. If forward bias is suddenly applied, a charging current through the junction capacitance may turn on the SCR. **Temperature triggering** Thyristor can be triggered by rising the junction temperature only when anode to cathode voltage is close to the break over voltage. **Light triggering** In this method light particles are made to strike the reverse biased junction. This causes an increase in the number of electron-hole pairs and triggers the thyristor.		7	7

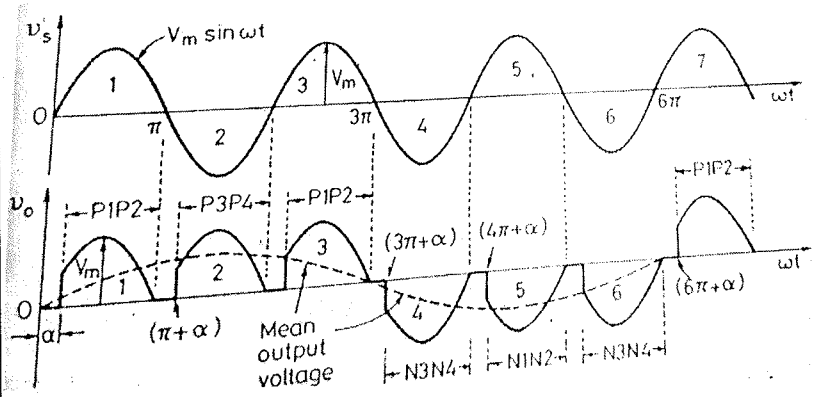
IV	 Resistance triggering circuits suffer from a limited range of firing angle control (0-90°). The potentiometer setting R2 determines the gate voltage amplitude. When R2 is large, current i is small and the voltage across R ie, Vg=iR is also small. As Vgp < Vgt, SCR will not turn on. Therefore load voltage Vo=0 When R2 is adjusted such that Vgp=Vgt. This gives the value of firing angle as 90°. If R2 is adjusted such that Vgp>Vgt. As soon as Vg becomes equal to Vgt for the first time, SCR is turned on. So firing angle is always less than 90°.	4 3	7	7
V	 The N layer (combination of N^+ and N^- layer) on the top constitutes the Drain. N^-layer gives high voltage capability. Adjacent to the N^- zone is a large P island. Inside the P Island are again N^+ islands. The source metal deposition covers a part of the N^+ islands and also the middle part of the P Island between the N^+ islands. Silicon dioxide is an insulation between the Silicon surface and the gate. A +ve voltage applied to the gate with respect to the source creates an electric field which pulls electrons from the N^+ zone in to the P zone immediately near the gate. In this way an N channel is created linking the source N^+ region and the drain N-region. This channel now provides the path for flow of current	3 2 2	7	7

	from the drain to the source.			
VI	 In this circuit the triggering of one thyristor turns off the other. Initially the capacitor is uncharged. When thyristor T1 is turned on by applying a gate pulse, load current flows from battery to load R1 through thyristor T1, along with a capacitor charging current from battery through load2(R2), capacitor C and thyristor T1. This current charges capacitor C to battery voltage Vs with polarity as shown in figure. To turn off T1, trigger pulse is applied to complementary thyristor T2. The capacitor voltage now appears as reverse bias across T1 and turns it off. Now load current flows from battery to load 2 (R2) through T2. In addition a charging current flows from battery through load1 (R1), capacitor C and T2. This charging current charges capacitor to supply voltage in the reverse polarity. When T1 is turned ON again, voltage across C reverse biases thyristor T2 and turns it off and the process repeats.	4 3	7	7
VII	 During the +ve half cycle, thyristors T1 and T2 are forward biased and when these two thyristors are triggered simultaneously at wt= α, current flows through the path L-T1-RL-T2-N. Supply voltage from this instant appears across the output terminal and forces the current through the load. At instant π, input voltage reverses. Because of large inductance L, a part of negative supply voltage appears across the output terminals. During –ve half cycle of the input voltage, thyristors T3	3+2 2	7	7

	and T4 are forward biased and are fired at $\pi + \alpha$. So T1 and T2 will be turned off and the load current will be transferred from T1 and T2 to T3 and T4. The current now flows through the path N-T3-RL-T4-L. This continues in every half cycle and we get the output voltage as shown in figure.			
VIII	 When R is high, firing angle of TRIAC is large. When R is small, firing angle is small. When capacitor C charges to break over voltage of DIAC, it turns ON. Consequently the gate of the TRIAC receives a trigger pulse through the DIAC. So the TRIAC is turned ON. Now source voltage Vs appears across the load during the positive half cycle for $(\pi-\alpha)$ radiance. When Vs becomes zero at wt= π, TRIAC turns off. During negative half cycle, the capacitor C now charges with lower plate positive. When Vc reaches Vdt of DIAC, both DIAC and TRIAC turn on and Vs appears across the load during the –ve half cycle .	4 3	7	7
IX.a	Step up cyclo converter: - Here the output frequency is higher than the input frequency . ie, (fo>fs). Step down cyclo converters: - Here the output frequency is lower than the input frequency. ie, (fo<fs).	2	7	7
IX.b		3		

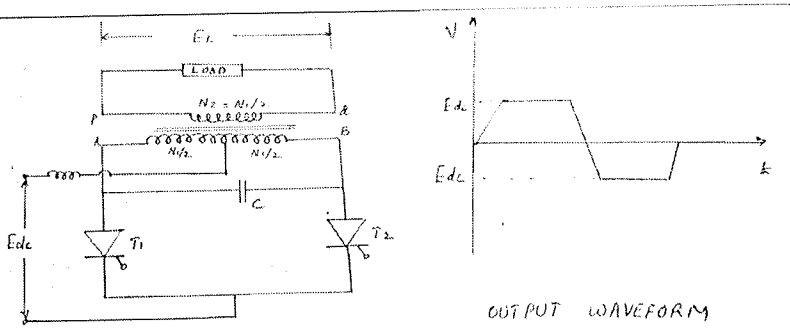


(any circuit)



2

X



3+1

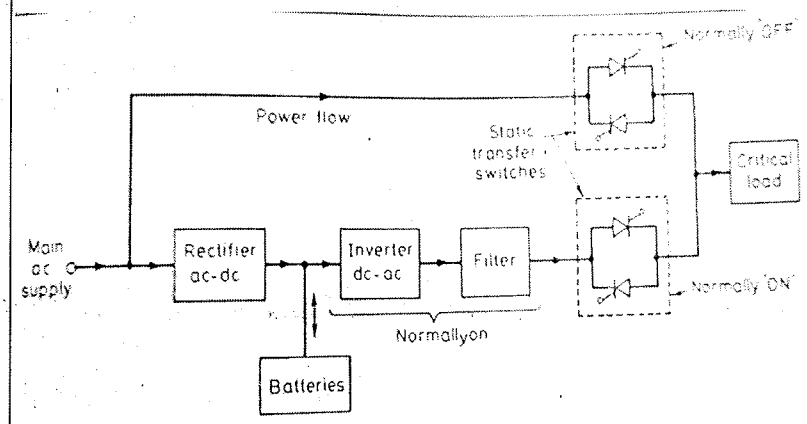
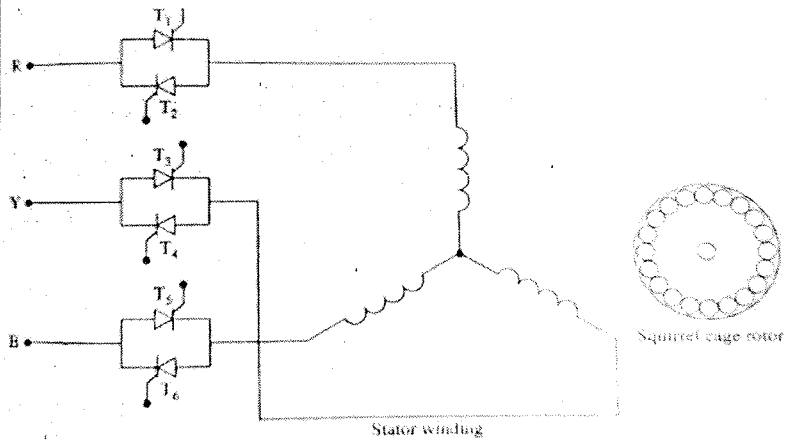
7

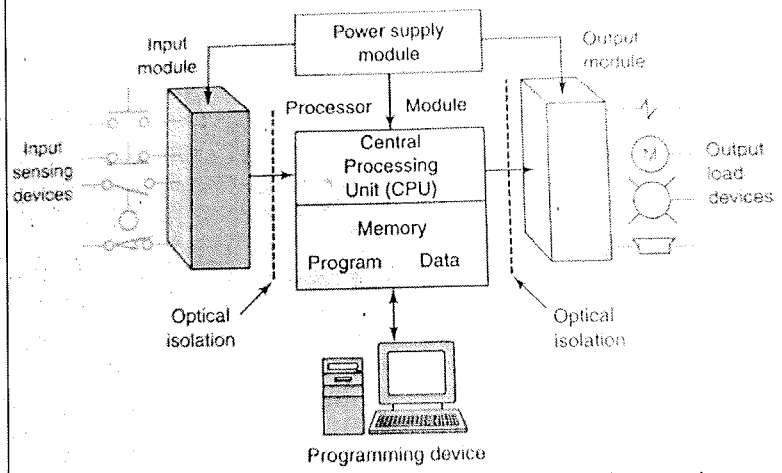
7

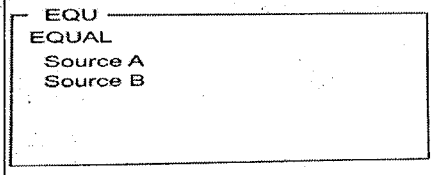
Initially there would not be any current in the circuit because both the SCRs are in blocking state. If now SCR T1 is triggered, neglecting the small voltage drop across L, the supply voltage Edc will appear across the left half of the transformer winding. By transformer action terminal B will be at a potential of 2Edc with respect to A. Thus capacitor will get charged to twice the supply voltage. The load voltage will be positive and of magnitude Edc. The load current at this time is +ve.

3

When thyristor T2 is fired, the commutating capacitor applies a voltage, -2Edc to appear across T1. When this reverse voltage is applied across T1, it will be turned off. SCR T2 will

	now be conducting and a voltage of 2Edc will appear across transformer primary and the commutating capacitor, but with reverse polarity. When T1 is again turned ON, T2 will be turned off. Thus a rectangular waveform will be obtained at the output terminal of the transformer.			
XI	 In this system, main AC supply is rectified and the rectifier delivers power to maintain required charge on the batteries. Rectifier also supplies power to inverter continuously which is then given to AC type load through filter and normally ON switch. In case of main supply failure, batteries at once take over with no break of supply to the critical load. No discontinuity in the illumination is observed in case of no-break UPS.	4 3	7	7
XII	 In this method, the speed of induction motor can be controlled by varying the stator voltage which is possible with the help of 3 sets of SCRs connected in anti parallel with each phase of input supply as shown in figure. The stator voltage can be reduced by delaying triggering pulse of the SCR. If we delay	4 3	7	7

	these pulses, the voltage may be reduced from rated input voltage, which causes to decrease the speed of the motor. Here torque T α V^2 where V is the applied stator voltage. When the motor attains stable speed, T α I/N.			
XIII	 **CPU**:- It is the brain of the system which has three sub parts. a) Microprocessor – Carries out mathematical and logical operations. b) Memory –The area of the CPU in which data and information is stored and retrieved. Storage memory(ROM) -The operating system program set by the manufacturer is stored in ROM. User memory(RAM) – Stores ladder logic program. c) Power supply –Internal power supply-Powers the CPU. - External power supply – Gives AC or DC power supply to I/O modules. **PROGRAMMING DEVICE**:- Help the user to enter and modify the required program in to PLC memory and troubleshoot the PLC ladder diagram. Most commonly used programming device is PC. **INPUT/OUTPUT MODULES** The input module has terminals in to which outside process electrical signals generated by sensors are entered. The output module has terminals to which output signals are sent to activate relays, solenoids, motors, displays etc. **RACK & CHASSIS** Framework on which PLC parts are mounted.	4 3	7	7

XIV	Data comparison instructions are used to compare two values, stored in different words.  **Equal To (EQU)** – This instruction compares two values for equality. If the values stored in Source A and Source B are equal, the rung output becomes true. **Greater than or Equal To (GEQ)**- This instruction compares if a value is greater than or equal to another value. **Greater than (GRT)** – If the value stored in Source A is greater than the value stored in source B, then the rung output becomes true. **Less than or Equal to (LEQ)** – If the value stored in source A is less than or equal to value in source B, then the rung output becomes true. **Less Than (LES)** – If the value stored in source A is less than the value in source B , then the rung output becomes true. **Not Equal To (NEQ)** – If the values stored in source A and Source B are unequal, then the rung output becomes true. **Limit Test (LIM)-** It compares if the given value lies within a specified range. **Masked Compare Equal To (MEQ)**- This instruction uses selected bits to compare two values for equality.		7	7