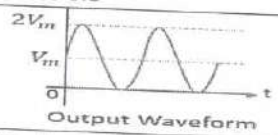
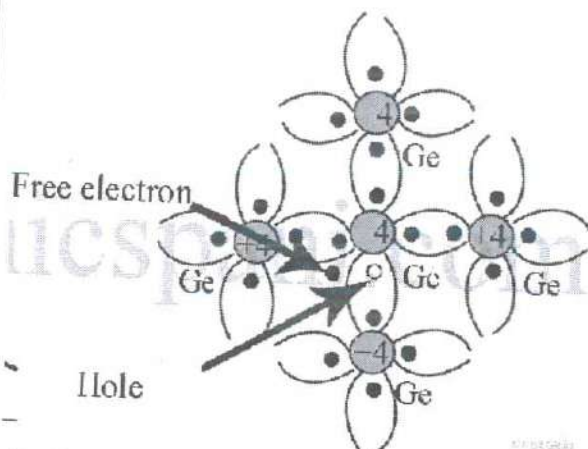


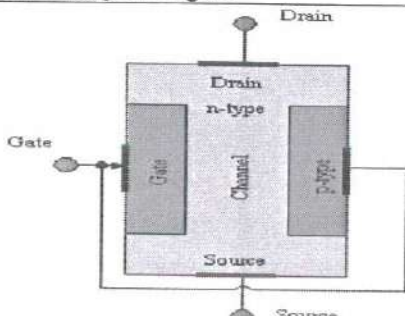
Scoring Indicators

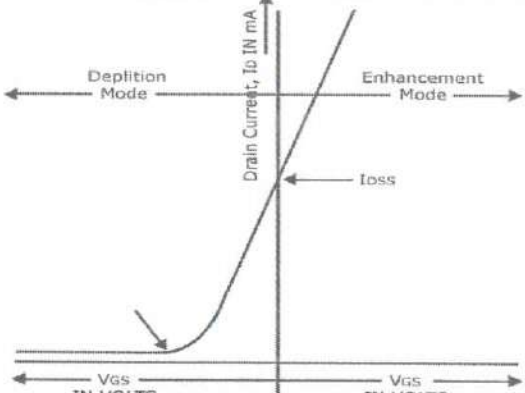
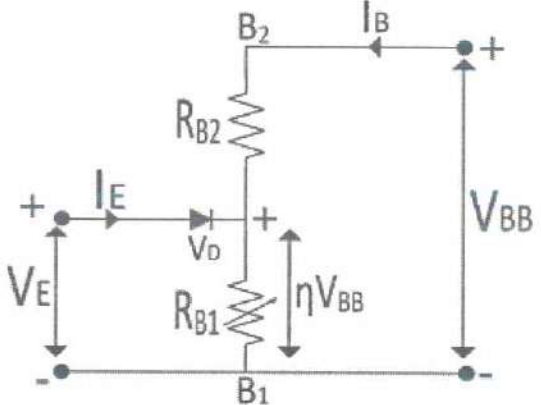
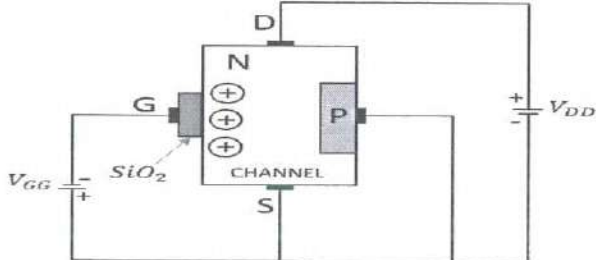
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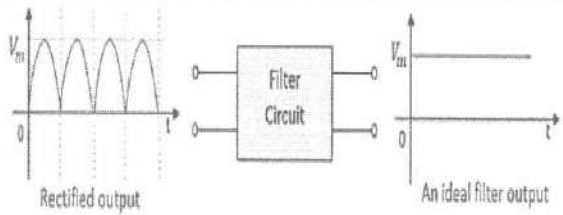
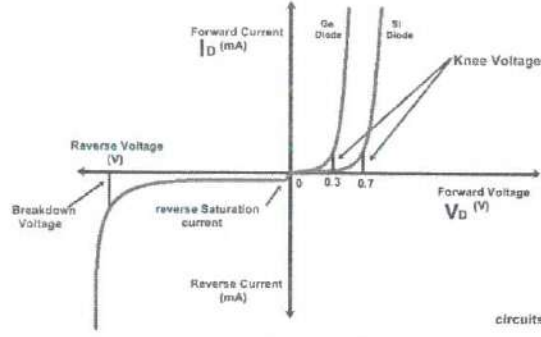
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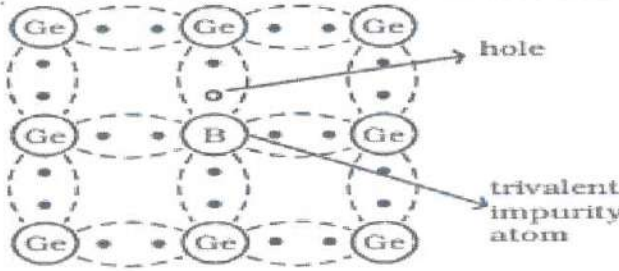
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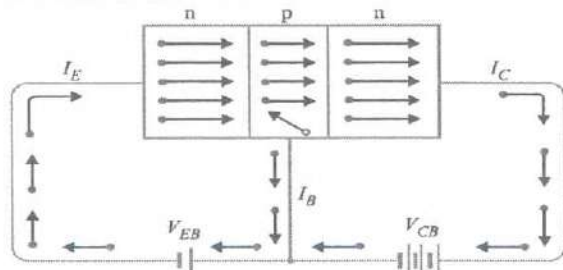
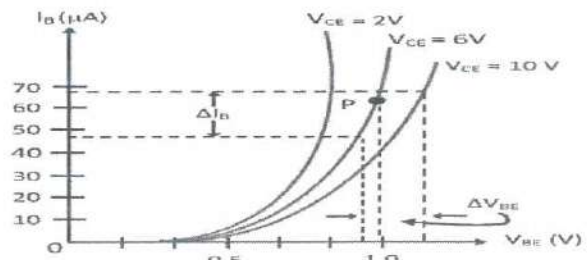
QueNo:	Scoring Indicators	Split score	Sub Total	Total Score
PART A				
1.1	1.1eV for Silicon and 0.7eV for Germanium	0.5+0.5	1	1
1.2	Breakdown voltage is the reverse voltage at which PN junction breaks down with sudden rise in reverse current	1	1	1
1.3	PIV is the maximum value of reverse voltage that a diode can withstand without damaging	1	1	1
1.4	Emitter	1	1	1
1.5	Base and collector leads	0.5+0.5	1	1
1.6	Current flowing through JFET is only due to one type of charge carriers. Ie: either holes or electrons	1	1	1
1.7	0.5 to 0.8	1	1	1
1.8	 <p style="text-align: center;">Output Waveform</p>	1	1	1
1.9	Much smaller than the time period of the input waveform	1	1	1
PART B				
II.1	 <p>At absolute zero an intrinsic S.C behaves as an insulator. At room temperature some of covalent bonds in intrinsic s.c break generating equal number of electrons and holes .This type of simultaneous generation of electron hole pairs is called thermal generation. The electrons randomly moves throughout the crystal, The negatively charged electrons and positively charged holes are termed as charge carriers. Whenever</p>	Fig:1.5 Expln:1. 5	1.5+1. 5	3

	the hole electron pair generated the holes exists in valence band and electrons in conduction band to take part in conduction of current			
II.2	<p>Reverse Breakdown voltage: Under normal reverse bias voltage a very little amount of reverse current flows through PN junction. On increasing the reverse voltage point reached at which the junction breakdown with a sudden rise in reverse current. Breakdown voltage is defined as the reverse voltage at which PN junction breaks down with a sudden rise in current.</p> <p>Knee Voltage: With forward bias to PN junction a very little current flows until the forward voltage exceeds junction barrier potential voltage. The forward voltage at which the current through the junction starts increasing rapidly is known as Knee voltage.</p>	<p>Breakdown voltage: 1.5</p> <p>Knee Voltage: 1.5</p>	1.5+1.5=3	3
II.3	<p>Static resistance is resistance offered by diode to dc in forward bias condition or ratio of dc forward voltage to dc current flowing through diode at operating point in forward bias condition</p> <p>Dynamic resistance is resistance offered by diode to ac in forward bias condition or ac forward resistance=change in voltage across diode/resulting change in current through diode</p>	1.5	1.5+1.5=3	3
II.4	<p>For an ideal amplifier circuit the input impedance should be as high as possible and output impedance should be as low as possible. For CC configuration even though the input impedance is very high, but gain is less than unity. So CC configuration is not suitable for amplifier circuits.</p> <p>The input impedance of CE is much higher than CB configuration, also the output impedance is much lower for CE compared to CB. The current gain of CB is less than unity, but for CE is very high. Such high gain in CE makes it possible to obtain high voltage and power gain</p>	3	3	3
II.5		Fig:1.5 Expln:1.5	1.5+1.5=3	3

	<p>Consists of a N type bar with two p regions diffused on opposite sides on in middle part. Both P-regions are connected internally and a single lead is taken out known as Gate. Two electrical connectors taken both ends on N region known as Drain and source</p>			
<p>II.6</p>	 <p>The graph shows Drain Current (I_D) in mA on the y-axis versus V_{GS} in Volts on the x-axis. The x-axis is divided into two regions: Depletion Mode (left, negative V_{GS}) and Enhancement Mode (right, positive V_{GS}). A curve starts at a minimum current I_{oss} at V_{GS} = 0. In the depletion mode, the current increases as V_{GS} becomes more negative. In the enhancement mode, the current increases as V_{GS} becomes more positive.</p>	<p>Fig only 3marks</p>	<p>3</p>	<p>3</p>
<p>II.7</p>	 <p>The diagram shows a diode-connected transistor. The emitter is connected to a voltage source V_E and a diode. The base is connected to a voltage source V_{BB} through a resistor R_{B2}. The collector is connected to the base through a resistor R_{B1}. The diode is represented by a junction with voltage V_D. The intrinsic stand-off ratio is denoted by η.</p> <p>The PN junction is represented at the emitter with a diode. Heavily doped silicon bar has high resistance is represented by 2 resistors connected in series R_{B1} & R_{B2}. R_{B1} lies between junction and base1 terminal is a variable resistor whose magnitude changes with changes in I_E. R_{B2} from base2 terminal to junction. The total resistance of silicon bar ie: R_{B1}+R_{B2}=R_{BB} with emitter terminal open is called inter base resistance. η is the intrinsic stand off ratio ie: $\eta = R_{B1} / [R_{B1} + R_{B2}]$</p>	<p>Fig:1.5 Expln:1. 5</p>	<p>1.5+1. 5=3</p>	<p>3</p>
<p>II.8</p>	 <p>The diagram shows a cross-section of a MOSFET. It features an N-type channel between two P-type regions. A SiO₂ gate oxide layer covers the top, with a Gate (G) terminal. The Drain (D) and Source (S) terminals are also shown. A V_{DD} supply is connected to the drain.</p> <p>The negative voltage on Gate induces a positive charge in the channel, so free electrons are repelled away from channel. Hence the channel gets depleted off free electrons. As the increase in V_{GS} the channel gets</p>	<p>Fig:1.5 Expln:1. 5</p>	<p>1.5+1. 5=3</p>	<p>3</p>

	completely depleted off free electrons and so the drain current reduces to zero			
II.9	FET	BJT	Any 3:3marks	1*3=3 3
	Unipolar device	Bipolar device		
	Voltage controlled device	Current controlled device		
	i/p resistance is high	i/p resistance is low		
	Has negative temp coefficient at high current levels	Has positive temp coefficient at high current levels		
	Does not effect from minority carrier storage effects	effect from minority carrier storage effects		
	Less noisy	More noisy		
II.10	 <p>The output of a rectifier consists of ac and dc components. This presence of pulsating ac components is undesirable and in order to remove this component filter circuits are used</p>	Fig:1.5 Expln:1. 5	1.5+1. 5=3	3
PART C				
III.1	 <p style="text-align: center;">P-N Junction Diode V-I Characteristics</p> <p>In forward biased condition , p-type of the pn junction is connected to the positive terminal and n-type is connected to the negative terminal of the external voltage. This results in reduced potential barrier. At some forward voltage i.e 0.7 V for Si and 0.3 V for Ge, the potential barrier is almost eliminated and the current starts flowing in the circuit. From this instant, the current increases with the increase in forward voltage.</p> <p>In reverse bias condition , the p-type of the pn junction is connected to the negative terminal and n-type is connected to the positive terminal of the external voltage resulting increased potential barrier</p>			

	<p>at the junction. so the junction resistance becomes very high and practically no current or a very small current of the order of μA, flows through the circuit known as reverse saturation current (I_s) and it is due to the minority carriers in the junction.</p> <p>If the applied reverse voltage is increased continuously, the kinetic energy of the minority carriers may become high enough to knock out electrons from the semiconductor atom. At this stage breakdown of the junction may occur. This is characterized by a sudden increase of reverse current.</p>			
<p>III. 2</p>	 <p>When a small amount of trivalent impurity (such as indium, boron or gallium) is added to a pure semiconductor crystal, the resulting semiconductor crystal is called P-type semiconductor.</p> <p>Fig shows the crystal structure obtained, when trivalent boron impurity is added with pure germanium crystal. The three valence electrons of the boron atom form covalent bonds with valence electrons of three neighbourhood germanium atoms. In the fourth covalent bond, only one valence electron is available from germanium atom and there is deficiency of one electron which is called as a hole. Hence for each boron atom added, one hole is created. Since the holes can accept electrons from neighbourhood, the impurity is called acceptor. The hole, may be filled by the electron from a neighbouring atom, creating a hole in that position from where the electron moves. This process continues and the hole moves about in a random manner due to thermal effects. Since the hole is associated with a positive charge moving from one position to another, this is called as P-type semiconductor. In P-type semiconductors, holes are the majority charge carriers and free electrons are the minority charge carriers.</p>	<p>Fig:3 marks Expln:4 marks</p>	<p>3+4=7</p>	<p>7</p>

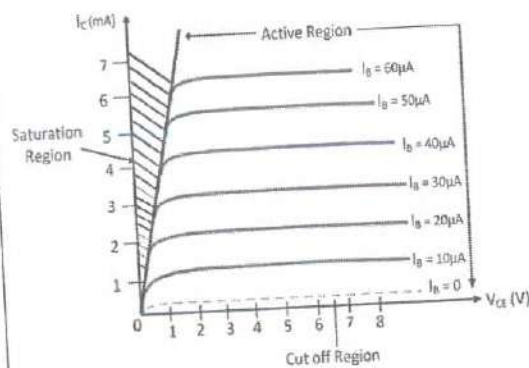
<p>III. 3</p>	 <p>Structure: The Transistor is a three terminal device having 2 PN junctions. 2 types-NPN & PNP. In NPN transistor, P-type material between two N-types respectively. The three terminals drawn from the transistor indicate Emitter, Base and Collector terminals. Emitter: is heavily doped as its main function is to supply a number of majority carriers, i.e. either electrons or holes. This emits electrons, it is called as an Emitter, indicated by letter E. Base middle material is the Base. This is thin and lightly doped. Its main function is to pass the majority carriers from the emitter to the collector, indicated by the letter B. Collector- right side material is Collector, function of collecting the carriers. this is larger in size than emitter and base. It is moderately doped, indicated by the letter C.</p> <p>Working: The emitter-base junction of a transistor is forward biased whereas collector-base junction is reverse biased. The forward bias causes the electrons in the n-type emitter to flow towards the base. This constitutes the emitter current I_E. As these electrons flow through the p-type base, they tend to combine with holes. As the base is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base (note 2) current I_B. The remainder ((Note 3) more than 95%) cross over into the collector region to constitute collector current I_C. In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents i.e.</p> $I_E = I_B + I_C$	<p>Fig:2 Expln:st ructure: 2 Workin g:3</p>	<p>2+2+3 =7</p>	<p>7</p>
<p>III. 4</p>	<p><u>INPUT CHARACTERISTICS</u></p> 	<p>i/p chara:2 +expln: 1.5=3.5 marks o/p chara:2 +expln: 1.5=3.5 marks</p>	<p>3.5+3. 5=7</p>	<p>7marks</p>

Input characteristic curve is drawn between the base current (I_B) and voltage between base and emitter (V_{BE}), when the voltage between collector and emitter (V_{CE}) is kept constant at a particular value. V_{BE} is increased in suitable equal steps and corresponding base current is noted. The procedure is repeated for different values of V_{CE} .

I_B values are plotted against V_{BE} for constant V_{CE} .

Upto knee voltage the I_B value is very small. Beyond knee voltage I_B current increases with increase in V_{BE} . The input impedance of the transistor is defined as the ratio of small change in base - emitter voltage to the corresponding change in base current at a given V_{CE} .

OUTPUT CHARACTERISTICS

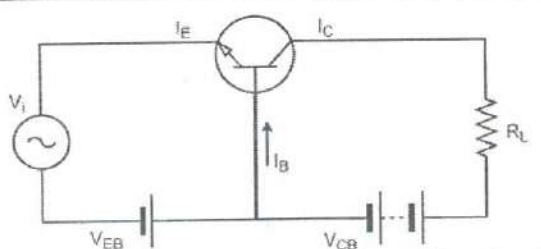


Output characteristics is the relationship between the output current I_C and the output voltage V_{CE} keeping input current constant I_B .

Active Region: In this region, collector junction is reverse biased and emitter junction is forward biased. This region lies above $I_B = 0$ and to the right of the ordinate $V_{CE} =$ a few tenths of a volt. For a given value of I_B the value of I_C increases due to early effect as (V_{CE}) increases.

Cutoff Region : cutoff region lies below $I_B = 0$ but now I_C is not zero due to reverse leakage current

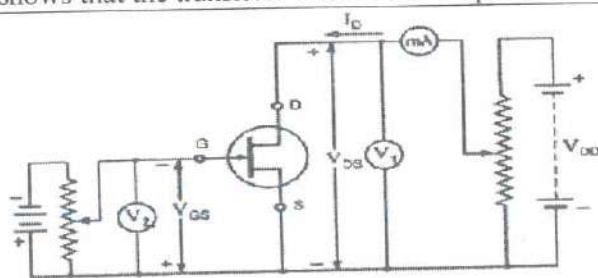
Saturation region : In this region, both emitter and collector junctions are forward biased equal to cut in voltage. In saturation region I_C does not depend on I_B

<p>III. 5</p>	<p>i)</p> <p>Relationship between α and β of a transistor :</p> <p>Relation between α & β:</p> <p>We know that; $I_E = I_B + I_C$.....(i)</p> <p>Dividing equation (i) by I_C.</p> $I_E / I_C = (I_B / I_C) + (I_C / I_C)$ <p>Therefore, $\frac{1}{\alpha} = \frac{1}{\beta} + 1$ (Since $\alpha = I_C / I_E$, $\beta = I_C / I_B$)</p> <p>Therefore $\frac{1}{\alpha} = \frac{1+\beta}{\beta}$</p> <p>Therefore $\alpha = \frac{\beta}{1+\beta}$</p> <p>Therefore $\frac{1}{\alpha} = \frac{1+\beta}{\beta}$</p> <p>Therefore $\alpha = \frac{\beta}{1+\beta}$</p> <p>$\alpha(1+\beta) = \beta$</p> <p>$\alpha + \alpha\beta = \beta$</p> <p>Therefore $\alpha = \beta - \alpha\beta$</p> <p>Therefore $\alpha = \beta (1 - \alpha)$</p> <p>Therefore $\beta = \frac{\alpha}{1-\alpha}$</p>	<p>Upto $\alpha =$ 2marks Upto β 2marks</p>	<p>2+2=4</p>	<p>4+#=7</p>
	<p>ii) $\beta=150$, $I_E=10\text{mA}$ $\alpha = \beta / [\beta + 1] = 150 / 150 + 1 = 150 / 151 = 0.993$ Also $\alpha = I_C / I_E$ $I_C = \alpha * I_E = 0.993 * 10\text{mA} = 9.93\text{mA}$ $I_E = I_C + I_B$ $I_B = I_E - I_C = 10 - 9.93 = 0.07\text{mA}$</p>	<p>3</p>	<p>3</p>	
<p>III. 6</p>	 <p>Transistor acts as an amplifier by raising the strength of a weak signal. The DC bias voltage applied to the</p>	<p>Fig:3 Expln:4</p>	<p>3+4=7</p>	<p>7</p>

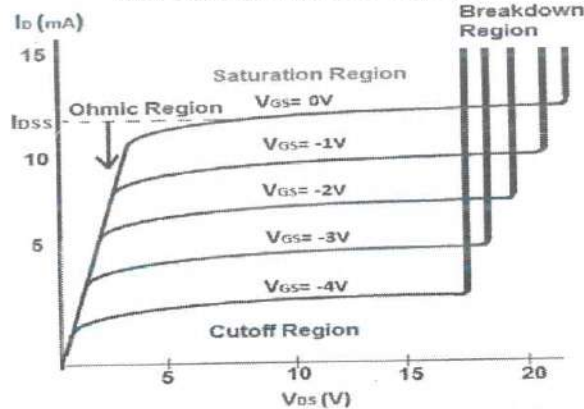
emitter base junction, makes it remain in forward biased condition. This forward bias is maintained regardless of the polarity of the signal. The below figure shows how a transistor looks like when connected as an amplifier.

The low resistance in input circuit, lets any small change in input signal to result in an appreciable change in the output. The emitter current caused by the input signal contributes the collector current, which when flows through the load resistor R_L , results in a large voltage drop across it. Thus a small input voltage results in a large output voltage, which shows that the transistor works as an amplifier

III. 7



FET Characteristics Curve



Ohmic Region : This part of the characteristic is linear indicating that for low values of V_{DS} , current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till called knee point is reached.

Pinch-off Region:or saturation region Here JFET operates as a constant-current device because I_D is relatively independent of V_{DS} . In this region the I_d remains constant at I_{DSS} . As V_{DS} increases, channel resistance also increases proportionally thereby keeping I , practically constant at I_{DSS} .

Breakdown Region: If V_{DS} increased further avalanche breakdown occurs JFET enters the breakdown region where I_D increases to an excessive value. This happens because the reverse-biased gate-channel P-N junction undergoes avalanche

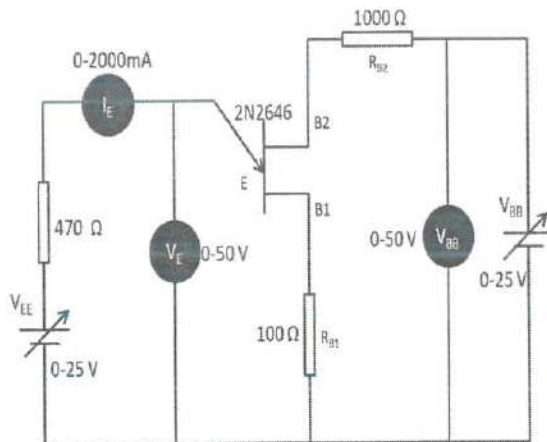
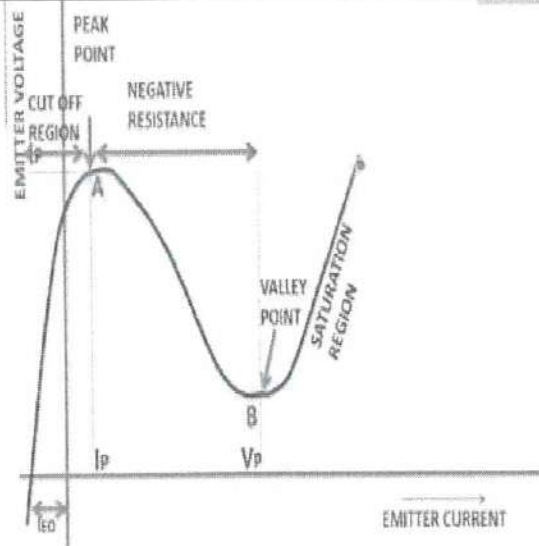
Ckt:2 marks
Charact
eristics:
3 marks
Expln:2
marks

2+3+2
=7

7

breakdown when small changes in V_{DS} produce very large changes in I_D .

III. 8



The emitter voltage V_E is applied between emitter E and base B1. V_E is positive with respect B1. Let increasing this voltage from zero.

The PN junction is reverse biased and emitter current I_E is negative as long as the emitter voltage $V_E < \eta V_{BB}$ as shown by the curve. The current flowing are very close to the reverse leakage current of PN junction reverse biased.

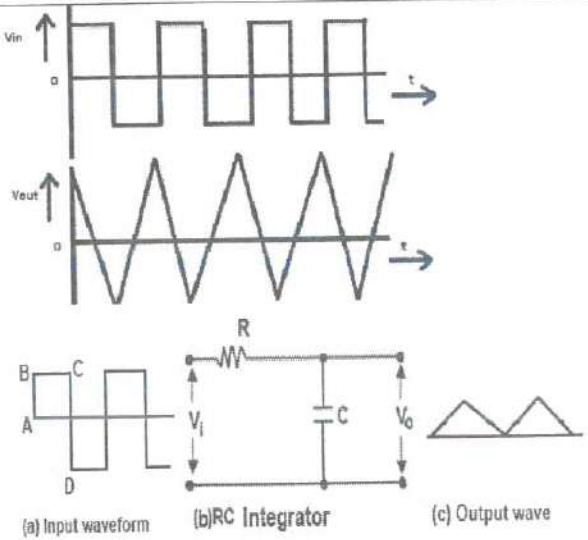
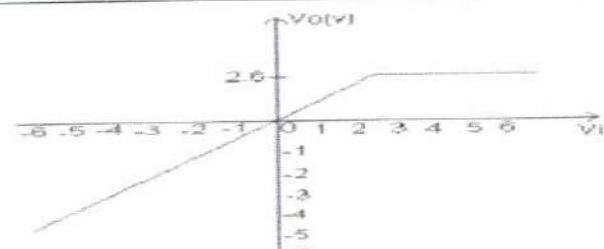
At point A, the emitter voltage V_E is equal to $\eta V_{BB} + V_D$ the PN junction is forward biased and UJT starts conducting. The point B is known as the **peak point** and the voltage and current across its known as peak point voltage (V_P) and peak point current (I_P) respectively.

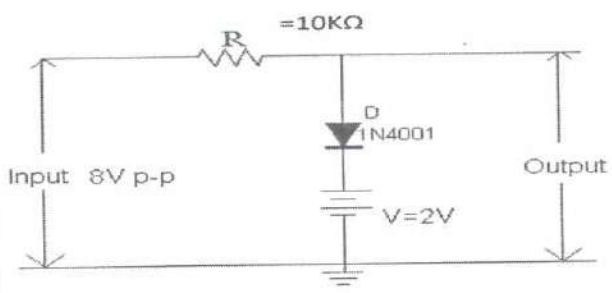
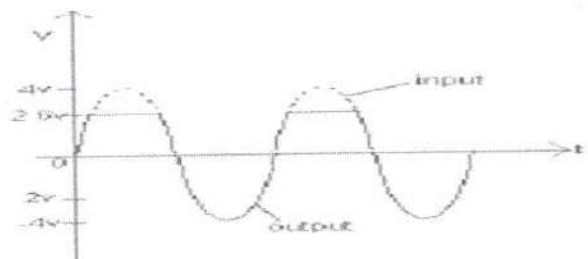
The emitter voltage V_E decreases with increase in emitter current I_E . Due to drop in resistance r_{b1} with

Chara:2
marks
Ckt:2ma
rks
Expln:3
marks

2+2+3
=7

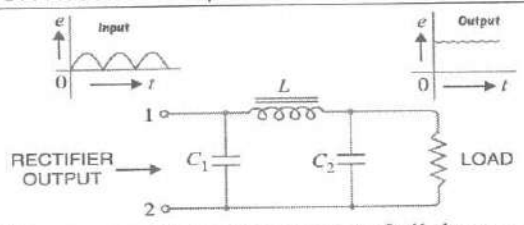
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	<p>increase in the value of I_E reduction in voltage across UJT.</p> <p>Thus the device exhibits a negative resistance region as shown by the curve AB</p> <p>The entire base region is saturated at point B and R_{BI} does not decrease any more. As shown in curve CQ, the rise in voltage V_E, further increase in I_E. The point B is known as valley voltage and the voltage and current across is known as valley voltage (V_V) and valley current (I_V).</p>			
<p>III. 9</p>	 <p>(a) Input waveform (b) RC Integrator (c) Output wave</p> <p>To obtain a triangular wave as output the wave shaping circuit is an integrator since when the input signal is a square wave the output of integrator is a triangular wave. Integration means summation, so output from integrator is the sum of all input signals at any instant. The sum is zero at point A and goes on increasing till it becomes maximum at point C. After this the summation goes to decrease to negative movements CD of the input signal</p>	<p>Waveff orms:3 Ckt :2 Expln :2</p>	<p>3+2+2 =7</p>	<p>7</p>
<p>III. 10</p>		<p>Fig:3 Transfer chara:2 Expln:2</p>	<p>3+2+2 =7</p>	<p>7</p>



$V_R = 2V, V_r = 0.6V$
 When the diode is forward biased $V_o = V_r + V_R = 2.6V$
 When $V_i > V_R + V_r = 2.6V$ the diode is forward biased and hence it conducts since it is ON it is short circuited. When $V_i < V_R + V_r$ the diode is reverse biased and hence it is OFF. It acts as an open circuit. $V_o = V_i$

III. 11



The construction arrangement of all the components resembles the shape of Greek letter Pi (π). Thus it is called **Pi filter**.

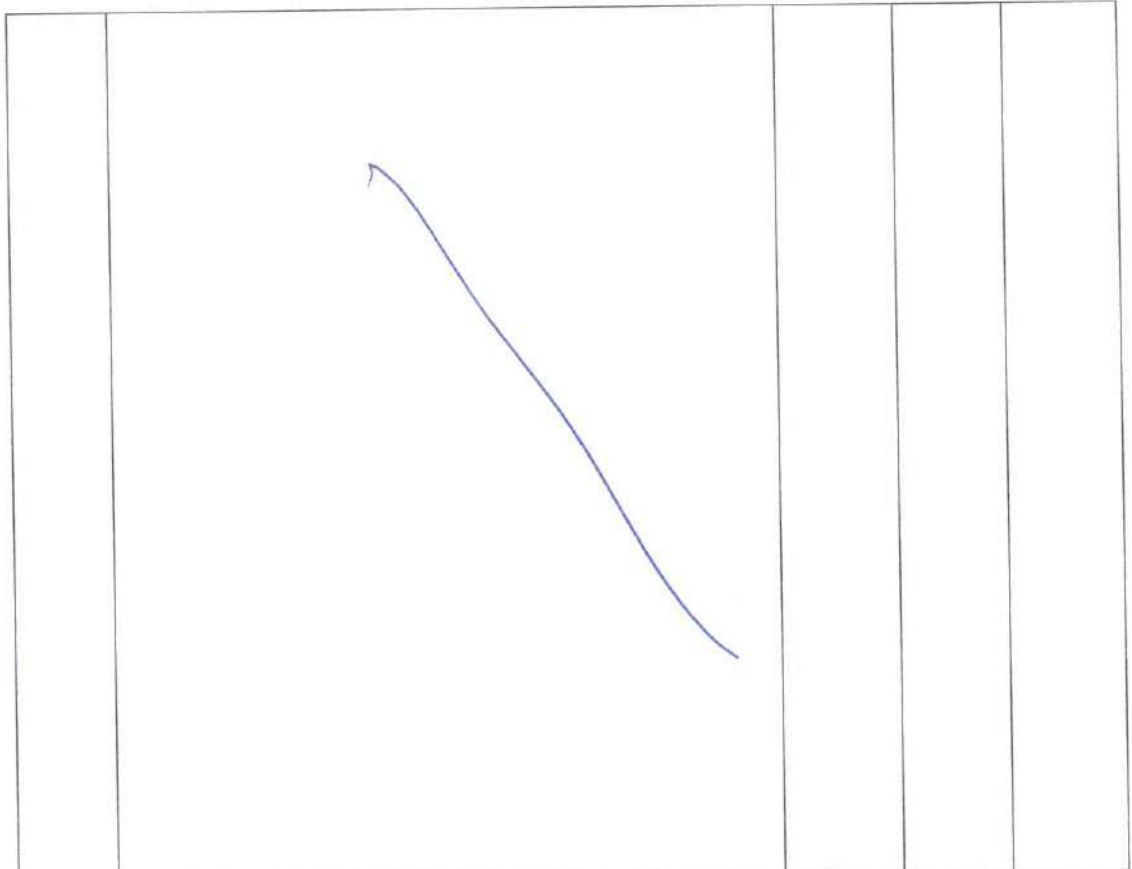
The output voltage coming from rectifier also consist of AC components. Thus it is a crucial need to remove these AC ripples to improve the performance of the device. The output from the rectifier is directly applied to the input capacitor. The capacitor provides a low impedance to AC ripples present in the output voltage and high resistance to DC voltage. Therefore, most of the AC ripples get bypassed through the capacitor in input stage only.

The residual AC components which are still present in filtered DC signal gets filtered when they pass through the inductor coil and through the capacitor connected parallel across the load. In this way, the efficiency of filtering increases multiple tim

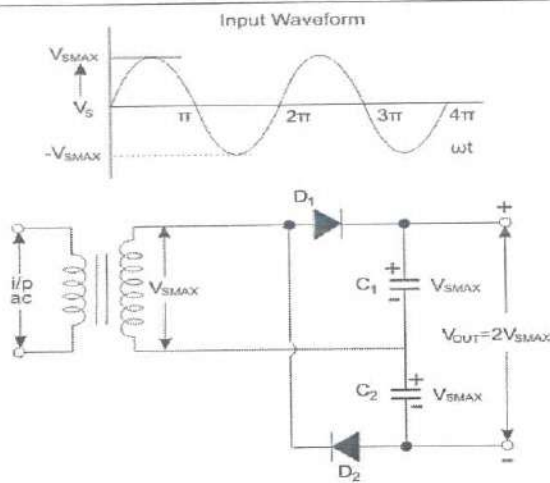
Wavefo
rms:2m
arks
Ckt:2ma
rks
Expln:3
marks

2+2+3
=7

7



III. 12



In this doubler, right through the positive cycle of input AC voltage, the first diode (D_1) is in the conducting state. That is a forward biased state, and it will charge the connected capacitor (C_1) equal to the peak value of AC secondary voltage of transformer ($V_{S\text{MAX}}$). At this time, D_2 will be in reverse biased condition or non-conducting state. Throughout the negative cycle of input AC voltage, the second diode (D_2) will be in forwarding biased state, and the second capacitor (C_2) gets charged.

Ckt:2marks
Waveforms:2 marks
Expln:3 mRKS

2+2+3 =7

7

	In the no-load condition, the entire voltages of $V_{C1}+V_{C2}=2V_{S_{MAX}}$ capacitors are delivered as the output voltage.			
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