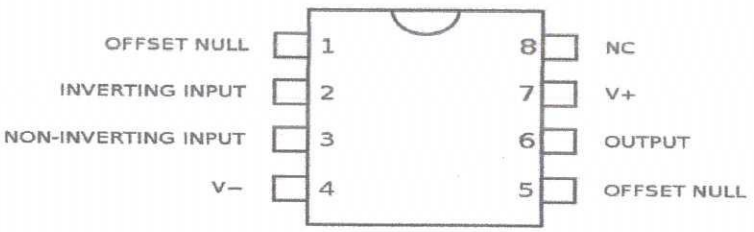
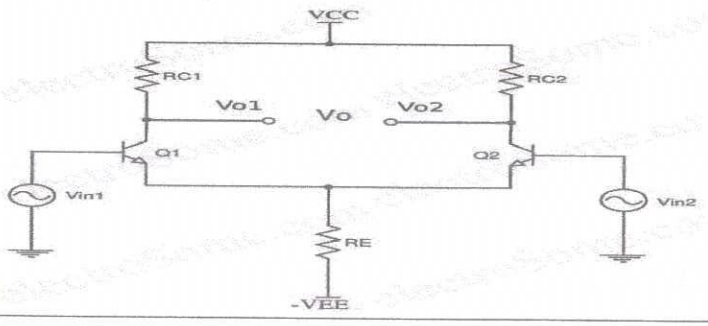
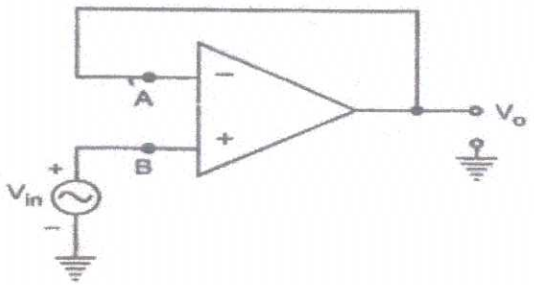
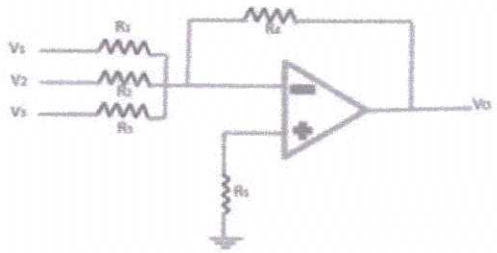
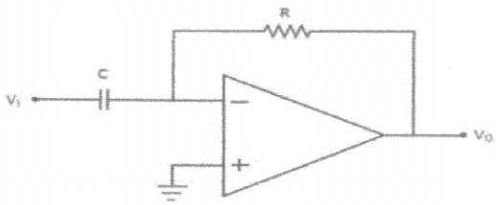
Scoring Indicators

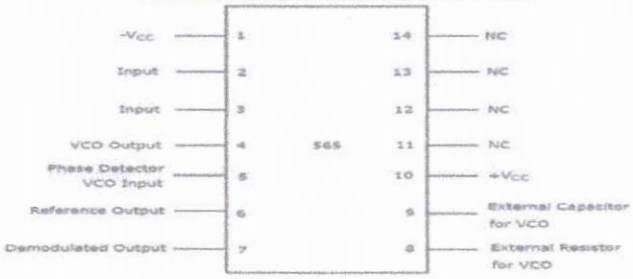
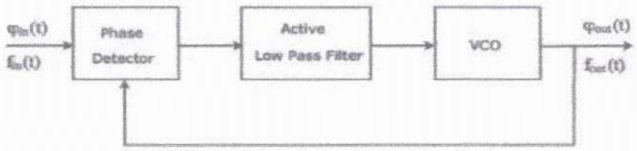
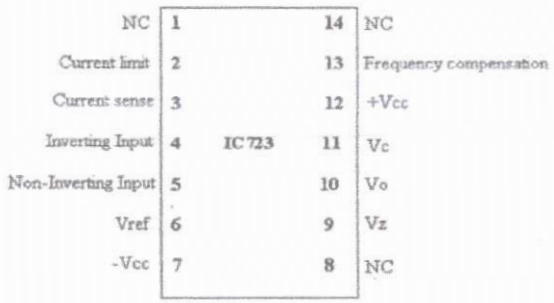
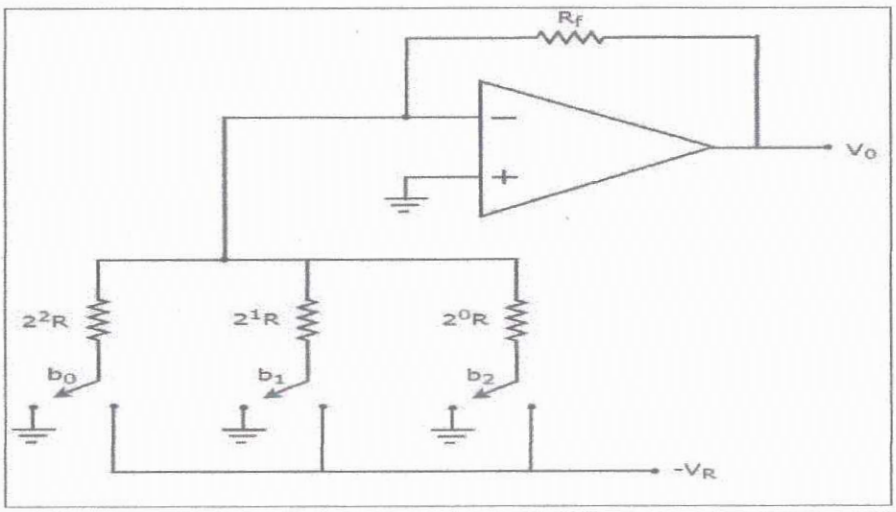
COURSE NAME : LINEAR INTEGRATED CIRCUITS

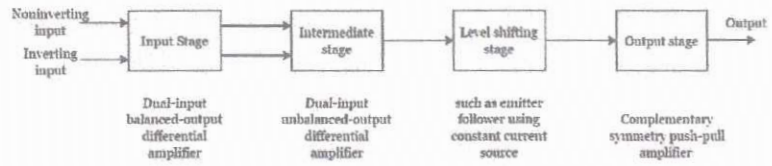
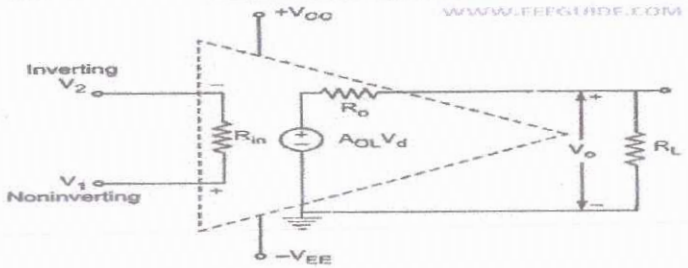
COURSE CODE : 4043 (2021)

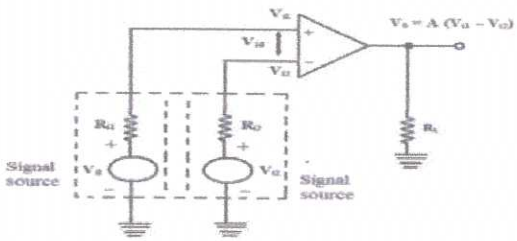
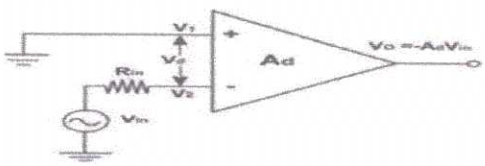
2103230122 : QID :

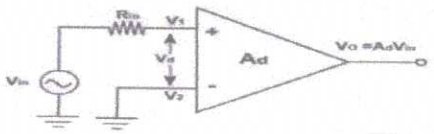
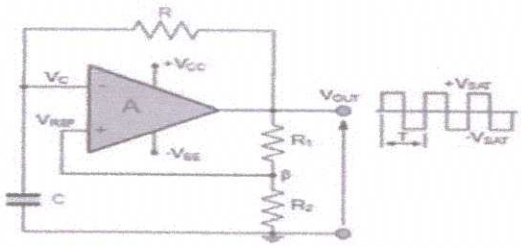
Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			9
I. 1	Common Mode Rejection Ratio		1	
I. 2	Infinite		1	
I. 3	Complementary symmetry push pull amplifier		1	
I. 4	Upper triggering point		1	
I. 5	8^{th} pin		1	
I. 6	Vo = - d/dt (Vi)		1	
I. 7	One		1	
I. 8	- 5 V		1	
I. 9	3 terminals		1	
	PART B			24
II. 1			3	
II. 2	Differential amplifier 		3	

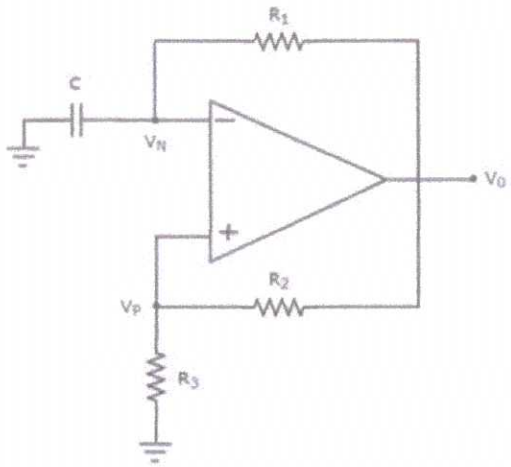
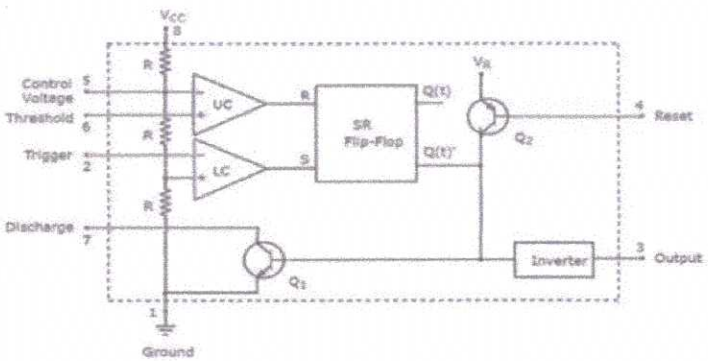
II. 3	 **Fig. 2.23 Voltage follower** • In non-inverting circuit configuration, the input impedance Rin has increased to infinity and the feedback impedance Rf reduced to zero. • The output is connected directly back to the negative inverting input so the feedback is 100% and Vin is exactly equal to Vout giving it a fixed gain of 1 or unity.	1 2	3	
II. 4	**Inverting Summing Amplifier** 		3	
II. 5	**Differentiator** 		3	
II. 6	The important features of the 555 timer are (i) It operates on +5v to +18 v supply voltages (ii) It has an adjustable duty cycle (iii) Timing is from microseconds to hours (iv) It has a current o/p		3	

II. 7	**Pin diagram of IC 565** 		3	
II. 8	**Block Diagram of PLL** 		3	
II.9	**IC-723 Pin diagram** 		3	
II.10	Weighted Resistor type DAC 		3	

	PART C			42
III. 1	 **Block Diagram of an Op-amp** The input stage is the dual input balanced output differential amplifier. This stage generally provides most of the voltage gain of the amplifier and also establishes the input resistance of the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. On most amplifiers, the intermediate stage is dual input, unbalanced output. Because of direct coupling, the dc voltage at the output of the intermediate stage is well above ground potential. Therefore, the level translator (shifting) circuit is used after the intermediate stage downwards to zero volts with respect to ground. The final stage is usually a push pull complementary symmetry amplifier output stage. The output stage increases the voltage swing and raises the ground supplying capabilities of the op-amp. A well designed output stage also provides low output resistance	4 3	7	7
III. 2	 **Fig. 2.8 Equivalent circuit of an op-amp** The Circuit which represents op-amp parameters in terms of physical components, for the analysis purpose is called equivalent circuit of an op-amp. The Equivalent Circuit of Practical Op Amp is shown in the Fig. The Equivalent Circuit of Practical Op Amp shows the op-amp parameters like input resistance, output resistance, the open loop voltage gain in terms of circuit components like R_{in}, R_o etc. The op-amp amplifies the difference $$V_o = A_{OL} V_d = A_{OL} (V_1 - V_2)$$ where • A_{OL} = Large signal open loop voltage gain. • V_d = Difference voltage $V_1 - V_2$ • V_1 = Noninverting input voltage with respect to ground • V_2 = Inverting input voltage with respect to ground • R_i = Input resistance of op-amp • R_o = Output resistance of op-amp The output voltage is directly proportional to the difference voltage V_d. between the two input voltages.	4 3	7	7

III. 3	**Ideal Characteristics of OP-AMP** **Voltage Gain, (A) - Infinite** The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better, so for an ideal amplifier the gain will be infinite. **Input impedance, (Zin) - Infinite** Input impedance is assumed to be infinite to prevent any current flowing from the source supply into the amplifiers input circuitry. **Output impedance, (Zout) - Zero** The output impedance of the ideal operational amplifier is assumed to be zero so that it can supply as much current as necessary to the load **Bandwidth, (BW) - Infinite** An ideal operational amplifier has an infinite Frequency Response and can amplify any frequency signal so it is assumed to have an infinite bandwidth. **Offset Voltage, (Vio) - Zero** The amplifiers output will be zero when the voltage difference between the inverting and non-inverting inputs is zero.		7	7
III. 4	**open loop configurations** In the case of amplifiers the term **open loop** indicates that no connection exists between input and output terminals of any type. ie, output signal is not feedback in any form as part of the input signal. In open loop configuration, The OPAMP functions as a high gain amplifier. There are three open loop OPAMP configurations **The Differential Amplifier**  **The Inverting Amplifier**  **v1= 0,** **v2 = vin.** **vo = -Ad vi**	1 2 2	7	7

	The Non-inverting amplifier  v1 = +vin , v2 = 0 vo = +Ad vin	2		
III. 5	**ASTABLE MULTIVIBRATOR USING OP-AMP**  In the op-amp multivibrator circuit the op-amp works as an analogue comparator. An op-amp comparator compares the voltages on its two inputs and gives a positive or negative output depending on whether the input is greater or less than some reference value, Vref. The Op-amp Multivibrator is an astable oscillator circuit that generates a output waveform using an RC timing network connected to the inverting input of the operational amplifier and a voltage divider network connected to the other non-inverting input. Firstly assume that the capacitor is fully discharged and the output of the op-amp is saturated at the positive supply rail. The capacitor, C starts to charge up from the output voltage, Vout through resistor, R at a rate determined by their RC time constant. the capacitor wants to charge up fully to the value of Vout (which is +V(sat)) within time constants. as the capacitors charging voltage at the op-amps inverting (-) terminal is equal to or greater than the voltage at the non-inverting terminal, the output will change state and be driven to the opposing negative supply rail(-Vsat).	4 3	7	7

III. 6	**Square Wave Generator**  In the circuit diagram, the resistor R1 is connected between the inverting input terminal of the op-amp and its output of op-amp. So, the resistor R1 is used in the negative feedback path. Similarly, the resistor R2 is connected between the non-inverting input terminal of the op-amp and its output. So, the resistor R2 is used in the positive feedback path.A capacitor is connected between the inverting input terminal of the op-amp and ground. So, the voltage across capacitor C will be the input voltage at this inverting terminal of op-amp. Similarly, a resistor R3 is connected between the non-inverting input terminal of the op-amp and ground. So, the voltage across resistor will be the input voltage at this non-inverting terminal of the op-amp.	3 4	7	7
III. 7	**Functional Block Diagram**  The functional diagram of 555 Timer contains a voltage divider network, two comparators, one SR flip-flop, two transistors and an inverter.	4	7	7

Voltage Divider Network

- The **voltage divider network** consists of a three $5K\,\Omega$ resistors that are connected in series between the supply voltage V_{CC} and ground.

- This network provides a voltage of $\frac{V_{CC}}{3}$ between a point and ground, if there exists only one $5K\,\Omega$ resistor. Similarly, it provides a voltage of $\frac{2V_{CC}}{3}$ between a point and ground, if there exists only two $5K\,\Omega$ resistors.

Comparator

- The functional diagram of a 555 Timer IC consists of two comparators: an Upper Comparator (UC) and a Lower Comparator (LC).

- Recall that a **comparator** compares the two inputs that are applied to it and produces an output.

- If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be $+V_{sat}$. This can be considered as **Logic High** ('1') in digital representation.

- If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be $-V_{sat}$. This can be considered as **Logic Low** ('0') in digital representation.

SR Flip-Flop

- Recall that a **SR flip-flop** operates with either positive clock transitions or negative clock transitions. It has two inputs: S and R , and two outputs: Q(t) and Q(t)'. The outputs, Q(t) & Q(t)' are complement to each other.

- The following table shows the **state table** of a SR flip-flop:

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	-

- Here, Q(t) & Q(t+1) are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive (negative) transition of clock signal is applied.

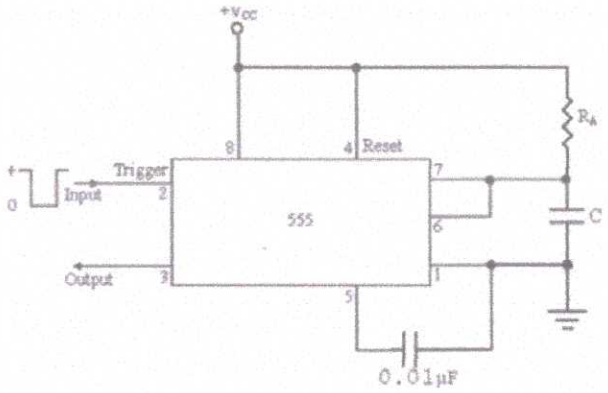
- The outputs of Lower Comparator (LC) and Upper Comparator (UC) are applied as **inputs of SR flip-flop** as shown in the functional diagram of 555 Timer IC.

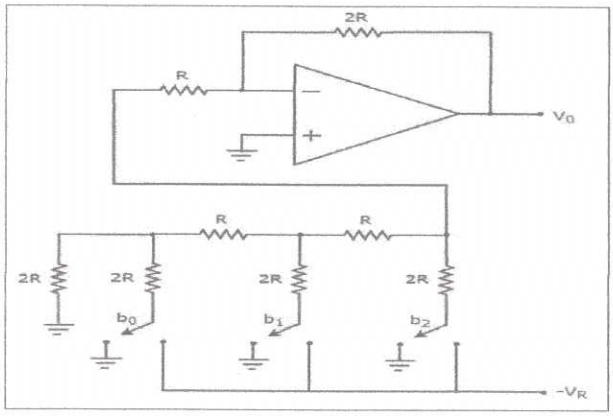
Transistors and Inverter

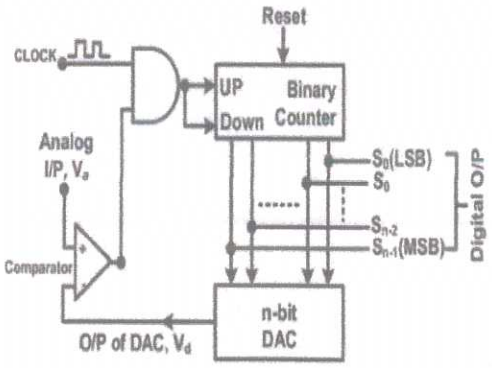
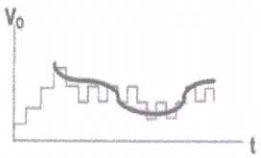
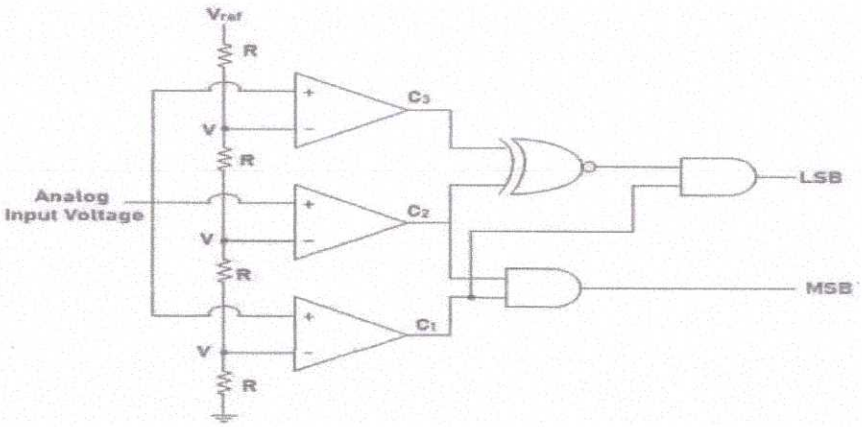
- The functional diagram of a 555 Timer IC consists of one npn transistor Q_1 and one pnp transistor Q_2. The npn transistor Q_1 will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.

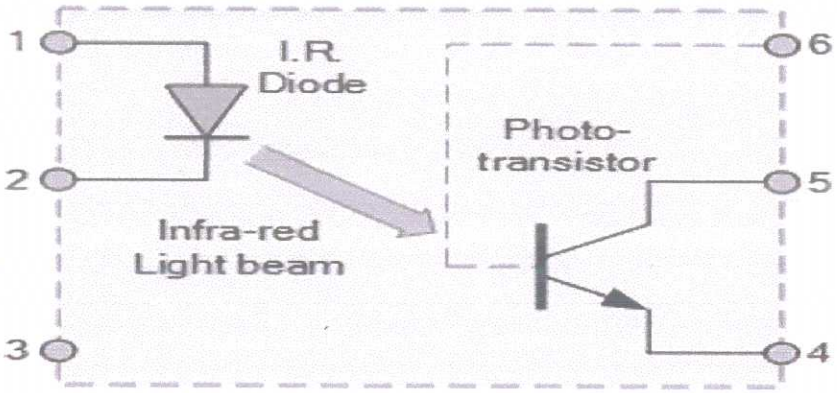
- The pnp transistor Q_2 is used as **buffer** in order to isolate the reset input from SR flip-flop and npn transistor Q_1.

- The **inverter** used in the functional diagram of a 555 Timer IC not only performs the inverting action but also amplifies the power level.

III. 8	**Monostable**  Initially when the output is low,the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through RA . When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high. Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC . After the time period, the upper comparator resets the FF, Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential The voltage across the capacitor as in fig (b) is given by $Vc = Vcc\ (1-e^{-t/RC})$ ..... (1) Therefore At $t = T$, $Vc = 2/3\ Vcc$ $2/3\ Vcc = Vcc(1-e^{-T/RC})$ or $T = RC \ln (1/3)$ Or $T = 1.1RC$ seconds ..... (2)	3 4	7	7
III. 9	**R-2R Ladder DAC** The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a R-2R ladder network in the inverting adder circuit.		7	7

	Thecircuit diagramof a 3-bit R-2R Ladder DAC is shown in the following figure –  Let the 3-bit binary input is b2 b1 b0 . Here, the bits b2 and b0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively. The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in above figure will be connected to the negative reference voltage, −VR when the corresponding input bits are equal to '1'. It is difficult to get the generalized output voltage equation of a R-2R Ladder DAC. But, we can find the analog output voltage values of R-2R Ladder DAC for individual binary input combinations easily.	4 3		
III. 10	**Counter type ADC:** A comparator is used at the input to compare input analog voltage with feedback reference voltage provided by DAC. An up/down counter is used to count the number of clock pulses applied through AND gate. When conversion started , counter is reset to zero and input analog voltage is applied to terminal of the comparator, when analog voltage is greater than feedback voltage provided by DAC, comparator o/p is logic 1 due to which clock pulses are applied to counter & counter will increase counting. When analog voltage is less than feedback voltage then o/p of comparator is logic 0 and counter will stop. At this time, o/p of counter will provide binary equivalent of i/p analog voltage.	3	7	7

	  Fig: Tracking The Analog Input	4		
III. 11	FLASH TYPE ADC It is the fastest ADC. In this type, number of comparator are connected in parallel to increase the speed of operation, hence also known as parallel comparator type ADC.  Figure below illustrates block diagram of Analog to Digital Converter (ADC) where Analog input is connected to all comparators so that the output is generated simultaneously. Reference Voltage (V_{ref}) is supplied to the Comparator through external source. The Digital output from the Comparators acts as input to Encoder. The Encoder converts the code from Comparator to Binary Code.	4 3	7	7

III. 12	**Opto-coupler** To provide electrical isolation between an input source and an output load using just light by using a very common and valuable electronic component called an **Opto-coupler**  Current from the source signal passes through the input LED which emits an infra-red light whose intensity is proportional to the electrical signal. This emitted light falls upon the base of the photo-transistor, causing it to switch-ON and conduct in a similar way to a normal bipolar transistor. The base connection of the photo-transistor can be left open (unconnected) for maximum sensitivity to the LEDs infra-red light energy or connected to ground via a suitable external high value resistor to control the switching sensitivity making it more stable and resistant to false triggering by external electrical noise or voltage transients. When the current flowing through the LED is interrupted, the infra-red emitted light is cut-off, causing the photo-transistor to cease conducting. The photo-transistor can be used to switch current in the output circuit. The spectral response of the LED and the photo-sensitive device are closely matched being separated by a transparent medium such as glass, plastic or air. Since there is no direct electrical connection between the input and output of an opto-coupler, electrical isolation up to 10kV is achieved.	3 4	7	7