

Scoring Indicators

COURSE NAME: Embedded System and Real time operating system

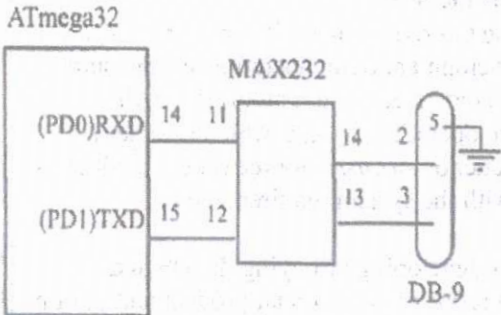
COURSE CODE :5131

QID: 2109230282

Revision:2021

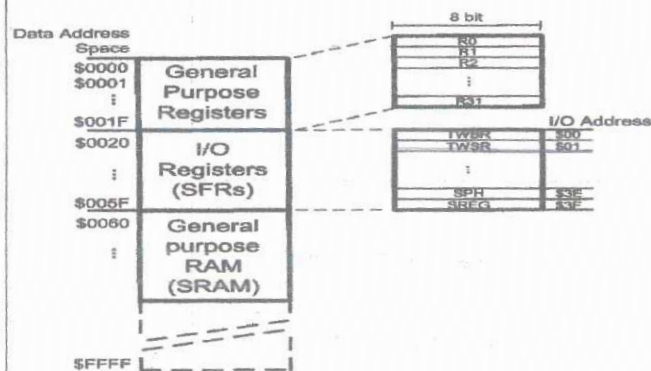
Q No	Scoring Indicators	Split score	Sub Total	Total score
I	PART A			9
I. 1	1.Consumer Electronics 2. Household appliances 3. Home automation and security 4. Telecom 5. Healthcare 6. Card Readers 7. Wearable devices	List any two: ½ marks each	1	
I. 2	Harvard Architecture	1	1	
I. 3	0xFF	1	1	
I. 4	DDRD=0xFF;	1	1	
I. 5	16 bit	1	1	
I. 6	Input pin	1	1	
I. 7	1s(high)	1	1	
I. 8	Kernel	1	1	
I. 9	Thread	1	1	
	PART B			24
II. 1	1.Data collection/Storage/Representation 2.Data Communication 3.Data (Signal)processing 4.Monitoring 5.Control 6.Application Specific User Interface	Any three: 1 mark each	3	
II. 2	DDRx (Data Direction Register): Configuring a given port as input or output PORTx (Port Output Pin): To write the data to the pins PINx (Port Input Pin): To read the data present at the pins.	1 1 1	3	

II. 3	<pre> #include <avr/io.h> //standard AVR header int main(void) { unsigned char temp; DDRB = 0x00; //Port B is input DDRC = 0xFF; //Port C is output while(1) { temp = PINB; PORTC = temp; } return 0; } </pre>	1 2	3																																					
II. 4	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2"></th> <th>AND</th> <th>OR</th> <th>EX-OR</th> <th>Inverter</th> </tr> <tr> <th>A</th> <th>B</th> <th>A&B</th> <th>A B</th> <th>A^B</th> <th>Y=~B</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>The following shows some examples using the C bit-wise operators:</p> <ol style="list-style-type: none"> 0x35 & 0x0F = 0x05 /* ANDing */ 0x04 0x68 = 0x6C /* ORing */ 0x54 ^ 0x78 = 0x2C /* XORing */ ~0x55 = 0xAA /* Inverting 55H */ 			AND	OR	EX-OR	Inverter	A	B	A&B	A B	A^B	Y=~B	0	0	0	0	0	1	0	1	0	1	1	0	1	0	0	1	1	0	1	1	1	1	0	1	Listing:2 Examples:1	3	
		AND	OR	EX-OR	Inverter																																			
A	B	A&B	A B	A^B	Y=~B																																			
0	0	0	0	0	1																																			
0	1	0	1	1	0																																			
1	0	0	1	1	0																																			
1	1	1	1	0	1																																			
II. 5	<p>Some of the most widely used sources of interrupts in the AVR are given below:</p> <ol style="list-style-type: none"> There are at least two interrupts set aside for each of the timers, one for overflow and another for compare match. Three interrupts are set aside for external hardware interrupts. Pins PD2, PD3 and PB2 are for external hardware interrupts INT0, INT1 and INT2, respectively. Serial communications USART has three interrupts, one for receive and two interrupts for transmit. The SPI (Serial Peripheral Interface) interrupt. The ADC. 	Any 3: 3 marks	3																																					
II. 6	<ul style="list-style-type: none"> To send data to LCD, Make pins RS=1 and R/W=0. Then put data on the data pins (D0-D7) and send a high-to-low pulse to the E pin to enable the internal latch of the LCD. After sending data wait for 100 microseconds to let the LCD module to write the data on the screen. 	3	3																																					

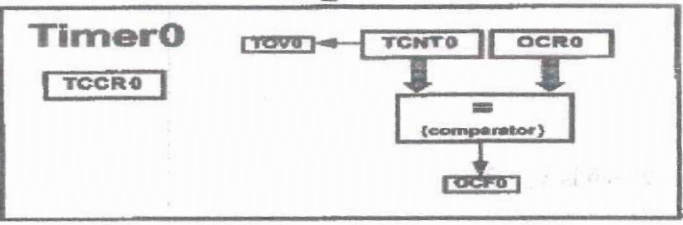
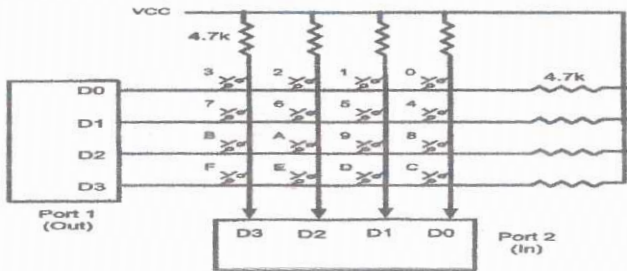
II. 7		3	3	
II. 8	<p>Hard Real-time</p> <ul style="list-style-type: none"> • Strictly adhere to the time constraints for a task . • Must meet the deadline for a task without any slippage. • Missing any deadline may produce catastrophic results for Hard Real-time system • Eg: Air bag Control System, Anti-lock brake system for vehicles <p>Soft Real-time:</p> <ul style="list-style-type: none"> • Doesn't guarantee meeting deadlines, but offer best effort to meet deadline • Missing deadlines for tasks are acceptable • Eg: Automatic Teller machine, Audio-video playback system 	1 ½	3	
II.9	<p>Multiprocessing</p> <ul style="list-style-type: none"> • <i>Multiprocessing</i> describes the ability to execute multiple processes simultaneously. • Systems which are capable of performing multiprocessing, are known as <i>multiprocessor</i> systems. • <i>Multiprocessor</i> systems possess multiple CPUs and can execute multiple processes simultaneously. <p>Multitasking</p> <ul style="list-style-type: none"> • The ability of an operating system to hold multiple processes in memory and switch the processor (CPU) from executing one process to another process is known as <i>multitasking</i>. • Multitasking creates the illusion of multiple tasks executing in parallel. • Multitasking involves the switching of CPU from executing one task to another. 	1 ½	3	

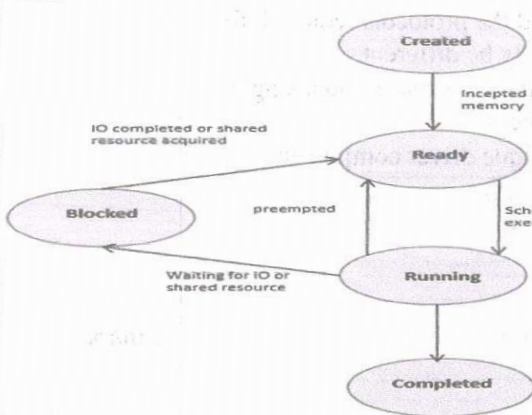
II.10	<p>1. Custom Developed or Off the Shelf</p> <ul style="list-style-type: none"> Depending on the OS requirement, it is possible to go for the complete development of an operating system suiting the embedded system needs or use an off the shelf. Readily available operating system, which is either a commercial product or an Open-Source product, which is in close match with the system requirements <p>2. Cost</p> <ul style="list-style-type: none"> The total cost for developing or buying the OS and maintaining it in terms of commercial product and custom build needs to be evaluated before taking a decision on the selection of OS. <p>3. Development and Debugging Tools Availability</p> <ul style="list-style-type: none"> The availability of development and debugging tools is a critical decision-making factor in the selection of an OS for embedded design. <p>4. After Sales</p> <ul style="list-style-type: none"> For a commercial embedded RTOS, after sales in the form of e-mail, on-call services, etc. for bug fixes, critical patch updates and support for production issues, etc. should be analyzed thoroughly. <p>5. Ease of Use</p> <ul style="list-style-type: none"> How easy it is to use a commercial RTOS is another important feature that needs to be considered in the RTOS selection 	Any three: 1 mark each	3																			
PART C																						
III	<table border="1" data-bbox="268 1218 975 1406"> <tr> <td style="text-align: center;">Bit</td> <td style="text-align: center;">D7</td> <td style="text-align: center;">D6</td> <td style="text-align: center;">D5</td> <td style="text-align: center;">D4</td> <td style="text-align: center;">D3</td> <td style="text-align: center;">D2</td> <td style="text-align: center;">D1</td> <td style="text-align: center;">D0</td> </tr> <tr> <td style="text-align: center;">SREG</td> <td style="text-align: center;">I</td> <td style="text-align: center;">T</td> <td style="text-align: center;">H</td> <td style="text-align: center;">S</td> <td style="text-align: center;">V</td> <td style="text-align: center;">N</td> <td style="text-align: center;">Z</td> <td style="text-align: center;">C</td> </tr> </table> <p>C - Carry flag S - Sign flag Z - Zero flag H - Half carry N - Negative flag T - Bit copy storage V - Overflow flag I - Global Interrupt Enable</p> <p>C-Carry flag</p> <ul style="list-style-type: none"> This flag is set whenever there is a carry out from the D7 bit. This flag bit is affected after an 8-bit addition or subtraction. <p>Z-Zero flag</p> <ul style="list-style-type: none"> This flag reflect the result of an arithmetic or logic operation If the result is 0 then Z=1 If the result is not = 0 then Z=0 <p>N-Negative flag</p> <ul style="list-style-type: none"> Binary representation of signed numbers uses D7 as the sign bit. Negative flag reflects the result of an arithmetic operation. If the D7 bit of the result is 0, then N=0 and the result is positive. If the D7 bit of the result is 1, then N=1 and the result is negative. <p>V-Overflow flag</p> <ul style="list-style-type: none"> This flag is set whenever the result of an signed number operation is too large . Overflow flag is used to detect errors in signed arithmetic operation <p>S-Sign flag</p> <ul style="list-style-type: none"> This flag is the result of exclusive ORing of N & V flags 	Bit	D7	D6	D5	D4	D3	D2	D1	D0	SREG	I	T	H	S	V	N	Z	C	2	7	7
Bit	D7	D6	D5	D4	D3	D2	D1	D0														
SREG	I	T	H	S	V	N	Z	C														

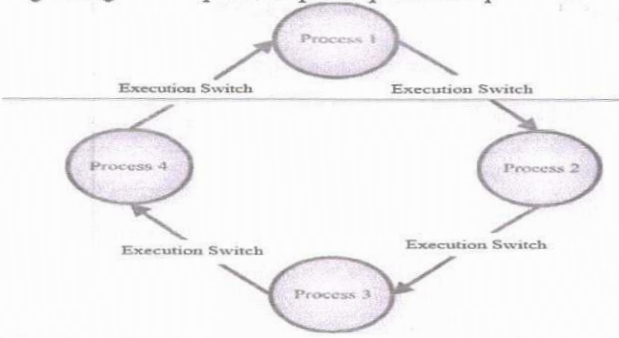
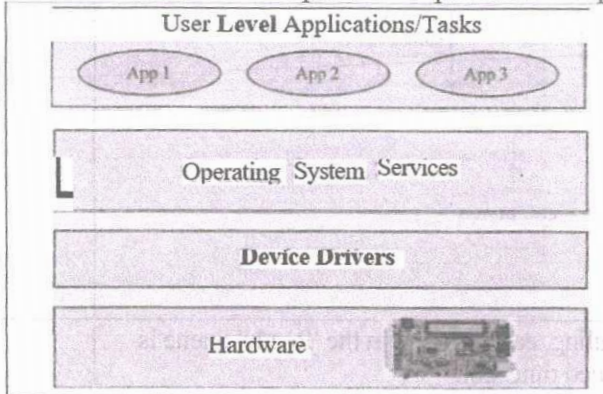
<p>H-Half carry</p> <ul style="list-style-type: none"> • If there is a carry from D3 to D4 during ADD or SUB operation, this bit is set, otherwise it is cleared. • This bit is used by instruction that performs BCD operation <p>T-Bit Copy Storage</p> <ul style="list-style-type: none"> • Used with BLD (bit load) and BST (bit store) instructions for loading and storing bit from one register to another. <p>I-Global Interrupt Enable</p> <ul style="list-style-type: none"> • Setting this bit enabled all the interrupt. • Resetting this disables all interrupts 		
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<p>IV.</p>  <p>Data memory composed of three parts: -</p> <ul style="list-style-type: none"> • GPRS • I/O memory • Internal data SRAM <p>GPRS</p> <ul style="list-style-type: none"> • It uses 32 bytes of data memory space. • They always take the address location \$00 - \$1F in the data memory space, regardless of the AVR chip number <p>I/O MEMORY(SFRs)</p> <ul style="list-style-type: none"> • functions of I/O memory are fixed by the CPU designer at the time of design. • it is used for control of the microcontroller or peripheral. • the AVR I/O memory is made of 8-bit registers. • it is used for specific functions such as status register, timers, serial communication etc. • all the AVR ha at least 64bytes of I/O memory locations <p>Internal data SRAM</p> <ul style="list-style-type: none"> • Internal data is widely used for storing data and parameters by AVR programmers and C compilers. • Generally, that is called <i>scratch pad</i>. • Each location of SRAM can be accessed by its address. • Each location is 8 bits wide. • Size of data SRAM can vary from chip to chip 	<p>4</p> <p>3</p>	<p>7</p> <p>7</p>
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V.	<pre> #include <avr/io.h> //standard AVR header int main(void) { DDRC = 0; //Port C is input DDRB = 0xFF; //Port B is output DDRD = 0xFF; //Port D is output unsigned char temp; while(1) { temp = PINC; //read from PINB if (temp < 100) PORTB = temp; else PORTD = temp; } return 0; } </pre>	Port configuration: 2 marks Logic: 5 marks	7	7
VI.	<p><u>Inverting Operator(~)</u></p> <pre> #include <avr/io.h> //standard AVR header int main(void) { DDRB = 0xFF; //Port B is output PORTB = 0xAA; while (1) PORTB = ~ PORTB; //toggle PORTB return 0; } </pre> <p><u>EX-OR Operator(^)</u></p> <pre> #include <avr/io.h> //standard AVR header int main(void) { DDRB = 0xFF; //Port B is output PORTB = 0xAA; while (1) PORTB = PORTB ^ 0xFF; return 0; } </pre>	3 ½ 3 ½	7	7
VII.	<pre> #include <avr/io.h> int main(void) { unsigned char x,y; unsigned char mybyte=0x42; DDRB=DDRC=0xFF; x=mybyte & 0x0F; PORTC=x 0x30; y=mybyte & 0xF0; y=y>>4; //shift right to lower 4 bits PORTD=y 0x30 } </pre> <p>Output: PORTC=0x32 PORTD=0x34</p>	Port Configuration:2 Logic :5	7	7

VIII.	<p>1. TCNTn Register (timer/counter)</p> <ul style="list-style-type: none"> In AVR, for each of the timers, there is a TCNTn (timer/counter) register. ATmega32 have TCNT0, TCNT1 and TCNT2. The TCNTn register is a counter. Upon reset, the TCNTn contains zero. It counts up with each pulse. The content of the timers/counters can be accessed using TCNTn. We can load a value into the TCNTn register or read its value. <p>2. TCCRn (timer/counter control register)</p> <ul style="list-style-type: none"> Each timer also has the TCCRn (timer/counter control register) register for setting modes of operation. For example, you can specify Timer0 to work as a timer or a counter by loading proper values into the TCCR0. <p>3. OCRn (output compare register) register</p> <ul style="list-style-type: none"> Each timer also has an OCRn (output compare register) register. The content of the OCRn is compared with the content of the TCNTn. When they are equal the OCFn (output compare flag) flag will be set. <p>4. TIFR (Timer/Counter Interrupt Flag Register)</p> <ul style="list-style-type: none"> Each timer has a TOVn (Timer Overflow) flag. When a timer overflows, its TOVn flag will be set. It's a part of TIFR (Timer/Counter Interrupt Flag Register) 	<p>Explanation of any two: 3 ½ marks each</p> <p>Figure: Optional</p>	7	7
IX.	<p>Scanning and identifying the key</p> <ul style="list-style-type: none"> A 4x4 matrix keyboard is connected to two ports. The rows are connected to an output port and the columns are connected to an input port. 	4	7	7

<p>XI.</p>	<p><u>Functions Of an Operating system</u></p> <ol style="list-style-type: none"> 1.Process management 2. Primary memory management. 3.File system management, 4. I/O system management, 5. Secondary storage management 6. Protection system 7. Interrupt handler 	<p>Listing:1 mark</p> <p>Explanation Of any 3: 6marks</p>	<p>7</p>	<p>7</p>
<p>XII.</p>	<p>The state at which a process is being created is referred as 'Created State'. The state, where a process is incepted into the memory and awaiting the processor time for execution, is known as 'Ready State'. 'Running state' is the state at which the process execution happens (execution of instructions). 'Blocked State/Wait State' refers to a state where a running process is <u>temporarily suspended from execution</u> and does not have immediate access to resources. A state where the process completes its execution is known as 'Completed State'.</p>  <pre> graph TD Created([Created]) -- "Incepted into the memory" --> Ready([Ready]) Ready -- "Scheduled for execution" --> Running([Running]) Running -- "preempted" --> Blocked([Blocked]) Blocked -- "IO completed or shared resource acquired" --> Ready Running -- "Waiting for IO or shared resource" --> Blocked Running --> Completed([Completed]) </pre>	<p>Transition Diagram:4 marks</p> <p>Explanation of each state:3marks</p>	<p>7</p>	<p>7</p>
<p>XIII.</p>	<ul style="list-style-type: none"> • In Round Robin scheduling, each process in the 'Ready' queue is executed for a pre-defined time slot. • The execution starts with picking up the first process in the 'Ready' queue (It is executed for a pre-defined time and when the pre-defined time elapses or the process completes (before the pre-defined time slice), the next process in the 'Ready' queue is selected for execution. • This is repeated for all the processes in the 'Ready' queue. • Once each process in the 'Ready' queue is executed for the pre-defined time period, the scheduler comes back and picks the first process in the 'Ready' queue again for execution. • The sequence is repeated. • The Round Robin scheduling is similar to the FCFS scheduling 			

	<p>with preemption.</p> <ul style="list-style-type: none"> • Preemption is added to switch the execution between the processes in the 'Ready' queue. • The 'Ready' queue can be considered as a circular queue in which the scheduler picks up the first process for execution and moves to the next till the end of the queue and then comes back to the beginning of the queue to pick up the first process. 	5	7	7
XIV.	<ul style="list-style-type: none"> • Device driver is a piece of software that acts as a <u>bridge between the operating system and the hardware.</u> • Device drivers are responsible for initiating and managing the communication with the hardware peripherals. • They are responsible for establishing the connectivity, initializing the hardware and transferring data. • An embedded product may contain different types of hardware components like Wi-Fi module, File systems, Storage device interface, etc. • The initialization of these devices and the protocols required for communicating with these devices may be different. • All these requirements are implemented in drivers and a single driver will not be able to satisfy all these. • Each class of hardware requires a unique driver component. 	5marks	7	7