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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, NOVEMBER - 2025

DIGITAL ELECTRONICS

[Maximum marks: 75] [Time: 3 Hours]

PART A

I. Answer all the following questions in one word or one sentence. Each question carries 1 mark.

(9 x 1 = 9 Marks)

		Module outcome	Cognitive level
1	Number system with base 16 is known as …….	M1.01	R
2	2's complement of 10110 is …….	M1.01	U
3	Name the fastest logic family.	M2.02	R
4	Total no of inputs in a Half Adder is …….	M2.04	U
5	When both inputs of a J-K flip-flop is HIGH, the output will ……..	M3.02	U
6	The logic circuits whose outputs at any instant of time depends only on the present input are called ……	M3.01	R
7	Mod 6 Asynchronous counter requires …….no of flipflops.	M4.02	U
8	How many natural states will there be in a 4- bit ripple counter?	M4.02	U
9	Full form of EEPROM is ……..	M4.04	R

PART B

II. Answer any eight questions from the following. Each question carries 3 marks.

(8 x 3 = 24 Marks)

		Module outcome	Cognitive level
1	Add the following numbers $(650E)_{16} + (8C1)_{16}$.	M1.01	A
2	State DeMorgans Theorem.	M1.04	R
3	Convert the given Gray code 01011 to Binary Code.	M1.02	U
4	Explain Half Adder circuit with Truth table & diagram.	M2.04	U
5	Draw the logic symbol and truth table of a D flip flop.	M3.02	U
6	Illustrate a 4 bit Serial in Serial Out Shift Register.	M3.03	U
7	Distinguish between Combinational and Sequential circuits.	M3.01	U
8	Draw the JK- Master slave flip flop.	M3.02	U
9	Differentiate between Synchronous & Asynchronous counters.	M4.01	U
10	Write short note on RAM.	M4.04	U

PART C

Answer all questions. Each question carries seven marks.

(6 x 7 = 42 Marks)

		Module outcome	Cognitive level
III	Illustrate the universal property of NAND gates.	M1.03	U
	OR		
IV	Minimize the following expression using K map. $F(a,b,c,d) = \sum m(1,3,5,7,9) + d(6,12,13)$	M1.04	A
V	Minimize the following expression using Kmap. $F(a,b,c,d) = \sum m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$	M1.04	A
	OR		
VI	Explain Binary Coded Decimal.	M1.02	U
VII	Explain the concept of parallel Adder.	M2.04	A
	OR		
VIII	With neat diagram and truth table explain a 4x1 MUX.	M2.04	A
IX	Illustrate a 3-to-8-line decoder.	M2.04	A
	OR		
X	Design a 1 to 4 Demultiplexer.	M2.04	A
XI	Explain the working of J-k Flip flop using NAND gates.	M3.02	U
	OR		
XII	With diagram and truth table, explain Ring Counter.	M3.04	U
XIII	Implement a mod-10 asynchronous counter using T FFs.	M4.02	A
	OR		
XIV	Write Short notes on ROM, PROM & EPROM.	M4.04	U

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