(39)

(14)

| Q No | SCORING INDICATORS<br><br>3131-COMPUTER ORGANISATION-<br>SET B | Split score | Sub Tota l | Total score |
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| | **PART A** | | | 9 |
| I. 1 | Program Counter (PC) | | 1 | |
| I. 2 | Redundant Array of Independent /Inexpensive Disks | | 1 | |
| I. 3 | Input | | 1 | |
| I. 4 | Small Computer System Interface | | 1 | |
| I. 5 | ALU | | 1 | |
| I. 6 | Memory Buffer Register | | 1 | |
| I. 7 | (Any two)<br>1. AX: This is the accumulator<br>2. BX: This is the base register.<br>3. CX: This is the counter register.<br>4. DX: This is the data register. | | 1 | |
| I. 8 | 1MB (2^20bytes) | | 1 | |
| I. 9 | Carry<br>Zero<br>Sign<br>Parity<br>Auxiliary Carry etc. Any two | | 1 | |
| | PART B | | | 24 |
| II. 1 | Computer Components<br>1.Input Unit<br>2.Output unit<br>3. Central Processing Unit<br>4.Memory<br><br>The Control Unit and the Arithmetic and Logic Unit constitute the Central Processing Unit<br><br>• Data and instructions need to get into the system --Input Unit<br>• The results is given out to the user --Output Unit<br>• Temporary storage of code and results is needed --Main memory | Listing (1)<br><br>Explanation:2 | 3 | |

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| II. 2 | • Erasable programmable read-only memory<br>• Erasure process can be performed repeatedly<br>• More expensive than PROM but it has the advantage of the multiple update capability | 3 | 3 | |
| II. 3 | Flat-Panel Display Monitor: In comparison to the CRT, a flat-panel display is a type of video display with less volume, weight, and power consumption. They can be hung on the wall or worn on the wrist.<br>Flat-panel displays are currently used in calculators, video games, monitors, laptop computers, and graphical displays. | Def:2<br>Applications :1<br>(2+1) | 3 | |
| II. 4 | • The basic interface for connecting peripheral devices to a PC is a small computer system interface.<br>• Based on the specification, it can typically respond up to 16 external devices using a single route, along with a host adapter.<br>• Small Computer System Interface is used to boost performance, deliver fast data transfer delivery and provide wider expansion for machines like CD-ROM drivers, scanners, DVD drives and CD writers. Small Computer System Interface is most commonly used for RAID, servers, highly efficient desktop computers, and storage area networks.<br>• The Small Computer System Interface has control, which is responsible for transmitting data across the Small Computer System Interface bus and the computers. | Any three points | 3 | |
| II. 5 | ADD (R3),R1<br>Executing this instruction requires the following actions:<br>1) Fetch the instruction.<br>2) Fetch the first operand.<br>3) Perform the addition<br>4) Load the result into R1. | 3 | 3 | |
| II. 6 | Features of hardwired control unit<br>• Hardwired control unit generates the control signals needed for the processor using logic circuits<br>• Hardwired control unit is faster when compared to microprogrammed control unit as the required control signals are generated with the help of hardwares<br>• Difficult to modify as the control signals that need to be generated are hard wired<br>• More costlier as everything has to be realized in terms of | Any three | 3 | |

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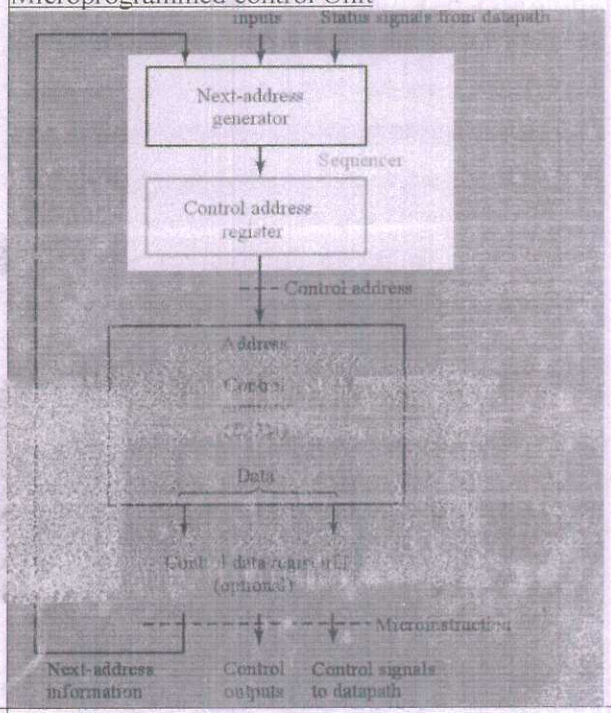
| | logic gates<br>• It cannot handle complex instructions as the circuit design for it becomes complex. | | | |
| II. 7 | MDR The Memory Data Register stores data that is being sent to, or received from, the memory along the bidirectional data bus.<br><br>MAR The Memory Address Register is used to store the address to access memory.<br><br>IR When memory is read, the data first goes to the MBR. If the data is an instruction it gets moved to the Instruction Register. | (1+1+1) | 3 | |
| II. 8 | Microprogrammed control Unit<br>  | | 3 | |
| II.9 | Data Segment register(DS)<br>Code Segment register(CS)<br><br>Stack Segment register(SS)<br>Extra Segment register(ES) | Any three (1+1+1) | 3 | |
| II.10 | Pentium features<br>• The Pentium is a 32-bit processor, | Any three | | |

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| | • It has a 32-bit address bus and a 64-bit data bus.<br>• This processor's data bus serves the on-chip caches, but not the 32-bit registers.<br>• The internal and external data buses are connected through the caches.<br>• processor consists of 8K byte code cache, 8K byte data cache.<br>• Translation Look-aside Buffer (TLB)<br>• Branch Trace Buffer (BTB)<br>• Integer pipelines U and V<br>• floating-point pipeline<br>• Microcode ROM<br>• and Control Unit (CU). | | 3 | |
| | PART C | | | 42 |
| III. | Features of Optical Disks<br>• Durability: Optical disks are less likely to degrade over time than other storage media, such as magnetic tape, HDDs, and SSDs. They are also resistant to most environmental threats, such as power surges and magnetic disturbances.<br>• Portability: Optical disks are portable.<br>• Inexpensive: Optical disks are inexpensive.<br>• Reliable storage: Optical disks are a reliable way to store data for long periods without degradation, making them useful for archival purposes.<br>• Capacity: Optical storage has a superior capacity compared to conventional magnetic-storage media.<br>• Recording characteristics: Optical storage has good recording characteristics, making it well-suited to memory-intensive applications.<br>• Data recording: Data is recorded on an optical disk by heating and melting a small spot on the disk with a high-powered laser beam.<br>• Data reading: A low-powered laser beam is used to read the disk by detecting the amount of light reflected. | Any four features<br>4 | 7 | |

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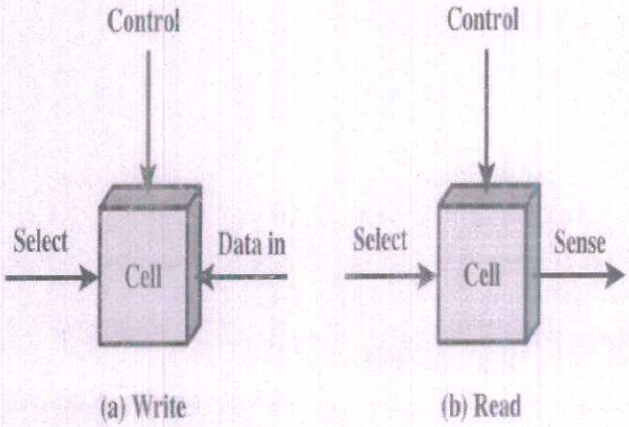
| | Examples: CD,DVD,Blu Ray DISC etc | Listing:3 | | |
| IV | Memory Cell Operation<br>  <br><br>(a) Write (b) Read<br>Figure 5.1 Memory Cell Operation<br>The basic element of a semiconductor memory is the memory cell. Although a varietyof electronic technologies are used, all semiconductor memory cells share certainproperties:<br>• They exhibit two stable (or semistable) states, which can be used to representbinary 1 and 0.They are capable of being written into (at least once), to set the state.They are capable of being read to sense the state.<br>Figure 5.1 depicts the operation of a memory cell. Most commonly, the cellhas three functional terminals capable of carrying an electrical signal. The selectterminal, as the name suggests, selects a memory cell for a read or write operation.<br>The control terminal indicates read or write. For writing, the other terminalprovides an electrical signal that sets the state of the cell to 1 or 0. For reading, thatterminal is used for output of the cell's state. The details of the internal organization,functioning, and timing of the | Fig-2<br>Expl-2 | 7 | |

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| | memory cell depend on the specific integratedcircuit technology used and are beyond the scope of this book, except for a briefsummary. For our purposes, we will take it as given that individual cells can beselected for reading and writing operations.<br><br>Synchronous DRAM (SDRAM)<br>• One of the most widely used forms of DRAM<br>• Exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states<br>• With synchronous access the DRAM moves data in and out under control of the system clock<br>  • The processor or other master issues the instruction and address information which is latched by the DRAM<br>  • The DRAM then responds after a set number of clock cycles<br>  • Meanwhile the master can safely do other tasks while the SDRAM is processing | 3 | | |
| V | Read only memory<br>• Non-volatile: ROM retains its contents even when the device's power is off.<br>• Read-only: Data stored in ROM can only be read from, not written to.<br>• Essential: ROM contains the instructions needed for a computer to start up and run its programs.<br><br>Programmable ROM (PROM)<br>• Less expensive alternative<br>• Non volatile and may be written into only once<br>• Writing process is performed electrically and may be performed by supplier or customer at a time later than the | 1<br><br>2 | | |

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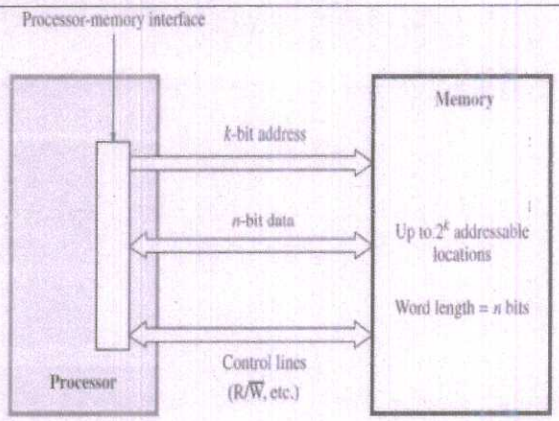
| | original chip fabrication<br>• Special equipment is required for the writing process<br>• Provides flexibility and convenience<br>• Attractive for high volume production runs<br>EPROM<br>• Erasable programmable read-only memory<br>• Erasure process can be performed repeatedly<br>• More expensive than PROM but it has the advantage of the multiple update capability<br>Flash Memory<br>• Intermediate between EPROM and EEPROM in both cost and functionality<br>• Uses an electrical erasing technology, does not provide byte-level erasure<br>Microchip is organized so that a section of memory cells are erased in a single action or "flash" | 2<br>2 | 7 | |
| VI |  <br>The connection between the processor and its memory consists of address, data, and control lines, as shown in Figure.<br>The processor uses the address lines to specify the memory location involved in a data transfer operation, and uses the data lines to transfer the data.<br>At the same time, the control lines carry the command indicating a Read or a Write operation and whether a byte or a word is to be transferred.<br>The control lines also provide the necessary timing information | 2<br>5 | 7 | |

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| | and are used by the memory to indicate when it has completed the requested operation.<br>When the processor-memory interface receives the memory's response, it asserts the MFC signal.<br>This is the processor's internal control signal that indicates that the requested memory operation has been completed.. | | | |
| VII | Direct Memory Access (DMA):<br>A special control unit may be provided to transfer a block of data directly between an I/O device and the main memory, without continuous intervention by the processor.<br><br>Control unit which performs these transfers is a part of the I/O device's interface circuit. This control unit is called as a DMA controller.<br>DMA controller performs functions that would be normally carried out by processor.<br>For each word, it provides the memory address and all the control signals.<br>To transfer a block of data, it increments the memory addresses and keeps track of the number of transfers.<br>DMA controller can transfer a block of data from an external device to the processor, without any intervention from the processor.<br><br>To initiate the DMA transfer, the processor informs the DMA controller of:<br>• Starting address,<br>• Number of words in the block.<br>• Direction of transfer (I/O device to the memory, or memory to the I/O device).<br><br>Once the DMA controller completes the DMA transfer, it informs the processor by raising an interrupt signal. | Def: 2<br><br>Working: 5 | 7 | |
| VIII | Memory-mapped I/O and programmed I/O are both methods for transmitting data between a CPU and peripheral devices, but they differ in several ways:<br><br>Memory-mapped I/O<br>In this method, the CPU treats I/O devices as computer memory and uses the same address space for both memory and I/O. This allows for faster response times and more direct access to I/O devices. Memory-mapped I/O is commonly used in modern computer systems because it's efficient and easy to implement. However, it can lead to conflicts between memory and I/O devices if not managed properly.<br>Programmed I/O<br>In this method, the CPU controls the entire I/O operation. Programmed I/O includes isolated I/O and port-mapped | (3.5+3.5) | 7 | |

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| | I/O. Isolated I/O offers more control over I/O operations and is useful for complex devices. Port-mapped I/O uses special CPU instructions for I/O operations, and is limited to one register for moving data. | | | |
| IX | Three Standard Interfaces<br>A standard interface used primarily on computer backplanes to connect interface cards and peripheral devices to the processor bus.<br>• A Universal Serial Bus (USB) is a common interface that allows the connection between devices and host controllers including a personal computer (PC). It connects peripheral devices including digital cameras, mice, keyboards, printers, scanners, media devices, external hard drives, and flash drives.<br>• PCI(Peripheral Component Interconnect) is often used for video display cards, network interfaces (e.g. Ethernet), and peripheral interfaces such as SCSI or USB.PCI card can be inserted into a PCI slot on a motherboard, providing additional I/O ports on the back of a computer.<br>• SCSI (Small Computer System Interface) is used to connect and communicate between computers and peripheral devices, such as hard disk drives, tape drives, CD/DVD drives, and scanners. SCSI was originally developed as both a protocol and a parallel physical interface. | Listing:1<br>2<br>2<br>2 | 7 | |
| X | **Keyboard**<br>The keyboard is the most frequent and widely used input device for entering data into a computer. Although there are some additional keys for performing other operations, the keyboard layout is similar to that of a typical typewriter. Generally, keyboards come in two sizes: 84 keys or 101/102 keys but currently keyboards with 104 keys or 108 keys are also available for Windows and the Internet.<br>Types of Keys<br>• Numeric Keys: It is used to enter numeric data or move the | 3 | | |

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| | cursor. It usually consists of a set of 17 keys.<br>• Typing Keys: The letter keys (A-Z) and number keys (09) are among these keys.<br>• Control Keys: These keys control the pointer and the screen. There are four directional arrow keys on it. Home, End, Insert, Alternate(Alt), Delete, Control(Ctrl), etc., and Escape are all control keys (Esc).<br>• Special Keys: Enter, Shift, Caps Lock, NumLk, Tab, etc., and Print Screen are among the special function keys on the keyboard.<br>• Function Keys: The 12 keys from F1 to F12 are on the topmost row of the keyboard.<br><br>**Scanner**<br><br>Scanner is an input device that functions similarly to a photocopier. It's employed when there's information on paper that needs to be transferred to the computer's hard disc for subsequent manipulation. The scanner collects images from the source and converts them to a digital format that may be saved on a disc. Before they are printed, these images can be modified.<br><br>**Video displays**<br><br>Monitors, also known as Visual Display Units (VDUs), are a computer's primary output device. It creates images by arranging small dots, known as pixels, in a rectangular pattern. The amount of pixels determines the image's sharpness. The two kinds of viewing screens used for monitors are described below.<br>Cathode-Ray Tube (CRT) Monitor: Pixels are minuscule visual elements that make up a CRT display. The higher the image quality or resolution, the smaller the pixels.<br>Flat-Panel Display Monitor: In comparison to the CRT, a flat-panel display is a type of video display with less volume, weight, and power consumption. They can be hung on the wall or worn on the wrist. | 2<br><br>2 | 7 | |
| XI | Microoperations for fetching a word<br><br>• CPU transfers the *address of the required information to MAR* from where it is transferred through Address Bus to Memory<br>• In the same time CPU uses it's control lines of memory bus to indicate that a *read operation* is required<br>• After issuing this request CPU waits until it receives a feedback from the memory indicating that the requested function has been completed<br>• This is done using another control signal on the memory bus. | | | |

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| | referred to as *Memory Function Completed* (MFC)<br>• The memory sets this signal to 1 to indicate that the contents of the specified location in the memory have been read and are available on the data lines of the memory bus and thus available for use inside the CPU<br>• This completes the memory operation.<br><br>**Example:** Assume that the address of the memory location to be accessed is in register R0 and data is to be loaded into register R1. Following sequence of operations are used .<br><br>1)MAR← [R0]<br><br>2)Read<br><br>3)Wait for MFC signal<br><br>4)R1 ←[MDR] | 7 | 7 | |
| XII | Principle of Pipelining<br>• Pipelining is the process of accumulating instruction from the processor through a pipeline.<br>• It allows storing and executing instructions in an orderly process. It is also known as pipeline processing.<br>• Pipelining is a technique where multiple instructions are overlapped during execution.<br>• Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure.<br>• Instructions enter from one end and exit from another end. Pipelining increases the overall instruction throughput.<br>• In pipeline system, each segment consists of an input register followed by a combinational circuit. The register is used to hold data and combinational circuit performs operations on it. The output of combinational circuit is applied to the input register of the next segment.<br>Types of Pipeline It is divided into 2 categories:<br>1. Arithmetic Pipeline | Definition:3<br><br>Types :2 | 7 | |

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| | 2. Instruction Pipeline<br><br>**Advantages of Pipelining**<br>1. The cycle time of the processor is reduced.<br>2. It increases the throughput of the system<br>3. It makes the system reliable.<br>**Disadvantages of Pipelining**<br>1. The design of pipelined processor is complex and costly to manufacture.<br>2. The instruction latency is more | 1<br><br>1 | | |
| XIII | • A multi-core processor is an integrated circuit with two or more processors connected to it for faster simultaneous processing of several tasks.<br>• When compared to single-core processors, a multicore processor has the potential of doing more tasks.<br>• Low energy consumption when doing many activities at once.<br>• Data takes less time to reach its destination since both cores are integrated on a single chip.<br>• With the use of a small circuit, the speed can be increased.<br>• Detecting infections with anti-virus software while playing a game is an example of multitasking.<br>• With the use of low frequency, it can accomplish numerous tasks at the same time.<br>• In comparison to a single-core processor, it is capable of processing large amounts of data. | Any seven points | 7 | |

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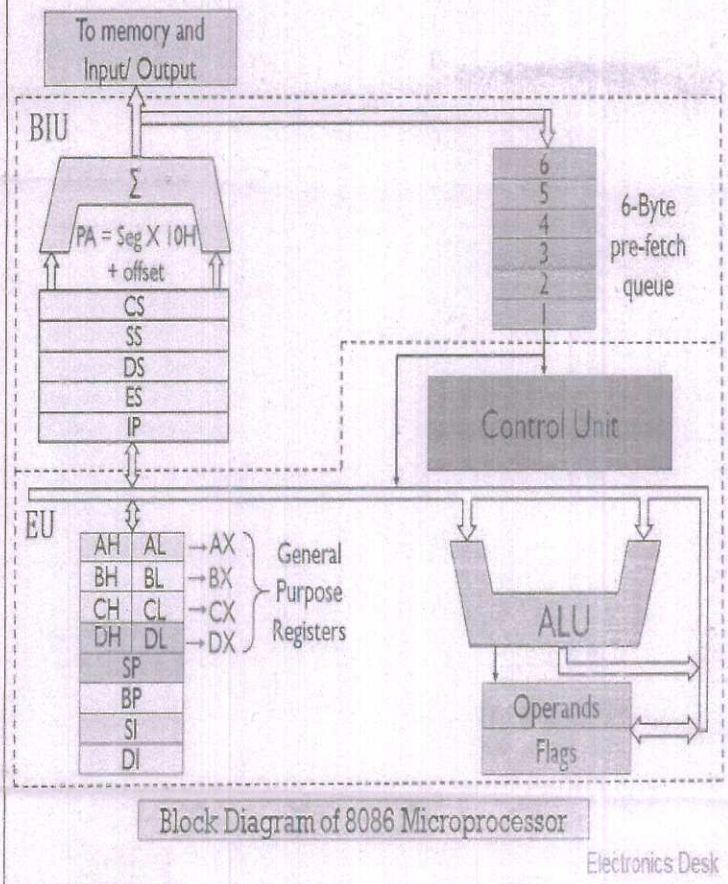
| XIV |  <br>Block Diagram of 8086 Microprocessor<br>Electronics Desk<br>8086 is a 16-bit microprocessor and was designed in 1978 by Intel. It has 20-bit address bus.<br>1 MB address in the memory.<br>The architecture of 8086 microprocessor is composed of 2 major units, the BIU i.e., Bus Interface Unit and EU i.e., Execution Unit. The figure shows the block diagram of the architectural representation of the 8086 microprocessor:<br>Bus Interface Unit (BIU)<br>The Bus Interface Unit (BIU) manages the data, address and control buses.<br>The BIU functions in such a way that it:<br>• Fetches the sequenced instruction from the memory,<br>• Finds the physical address of that location in the memory where the instruction is stored and<br>• Manages the 6-byte pre-fetch queue where the pipelined instructions are stored. | Fig(4)<br>Expla: ( 3) | 7 | |

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| | An 8086 microprocessor exhibits the property of pipelining the instructions in a queue while performing decoding and execution of the previous instruction. This saves the processor time of operation by a large amount. This pipelining is done in a 6-byte queue. Also, the BIU contains 4 segment registers. Each segment register is 16-bit. The segments are present in the memory and these registers hold the address of all the segments. These registers are as follows:<br><br>1.Code segment register: It is a 16-bit register and holds the address of the instruction or program stored in the code segment of the memory.<br><br>Also, the IP in the block diagram is the instruction pointer which is a default register that is used by the processor in order to get the desired instruction. The IP contains the offset address of the next byte that is to be taken from the code segment.<br><br>2. Stack segment register: The stack segment register provides the starting address of the stack segment in the memory. Like in stack pointer, PUSH and POP operations are used in this segment to give and take the data to/from it.<br><br>3. Data segment register: It holds the address of the data segment. The data segment stores the data in the memory whose address is present in this 16-bit register.<br><br>4. Extra segment register: Here the starting address of the extra segment is present. This register basically contains the address of the string data.<br><br>It is to be noteworthy that the physical address of the instruction is achieved by combining the segment address with that of the offset address.<br><br>6-byte pre-fetch queue: This queue is used in 8086 in order to perform pipelining. As at the time of decoding and execution of the instruction in EU, the BIU fetches the sequential upcoming instructions and stores it in this queue.<br><br>The size of this queue is 6-byte. This means at maximum a 6-byte instruction can be stored in this queue. The queue exhibits FIFO behavior., first in first out. | | | |