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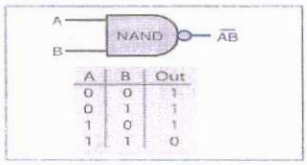
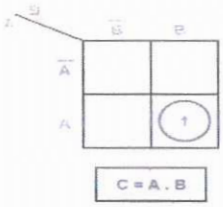
8

Scoring Indicators

Question Paper Set B

DIGITAL COMPUTER FUNDAMENTALS -TED (21) - 3134

Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			**9**
I. 1	$704_8 = 111\ 000\ 100_2$	1	1	
I. 2	0011	1	1	
I. 3	American Standard Code for Information Interchange	1	1	
I. 4	Eight	1	1	
I. 5		1	1	
I. 6		1	1	9
I. 7	n select lines and one out put	0.5 +0.5	1	
I. 8	A combinational logic circuit is one whose output solely depends on its current inputs. sequential circuits, on the other hand, are built using combinational circuits and memory elements called "flip-flops". These circuits generate output that depends on the current and previous states.	0.5 +0.5	1	
I. 9	PRESET and CLEAR	0.5 +0.5	1	
	PART B			24
II. 1	$EEEE_{16}$	3	3	3

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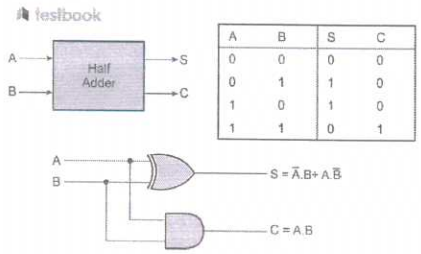
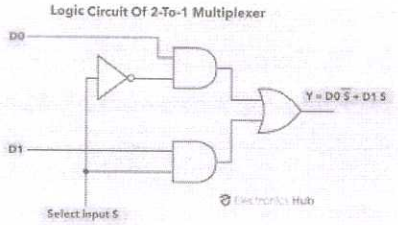
<table>
<tr><td>II.2</td><td>A parity bit is a check bit, which is added to a block of data for error detection purposes. It is used to validate the integrity of the data. The value of the parity bit is assigned either 0 or 1 that makes the number of 1s in the message block either even or odd depending upon the type of parity.</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>II.3</td><td>De Morgan's First Law :states that the complement of the product of two or more variables is corresponding to the sum of the complement of each variable.
Second Law: The complement of the sum of all the terms is equal to the product of the complement of each term.
(or write the Boolean equation)</td><td>1.5 + 1.5</td><td>3</td><td>3</td></tr>
<tr><td>II.4</td><td>X(X+Y) = XX + XY
= X(1+Y)
= X(1)
= X = RHS</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>II.4</td><td>
<table>
<tr><td>X</td><td>Y</td><td>Z</td><td>F</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>3</td><td>3</td><td>3</td></tr>
<tr><td>II.5</td><td>Starting from a true Boolean equation, another relation can be obtained by interchanging each OR sign with AND sign and each 1 with 0.
x+xy = x
duality is X.(X+Y) = X</td><td>1.5 + 1.5</td><td>3</td><td>3</td></tr>
<tr><td>II.6</td><td> 

<table>
<tr><td>A</td><td>B</td><td>Q</td></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table>
</td><td>1.5+1 .5</td><td>3</td><td>3</td></tr>
</table>

<table>
<tr>
<td>II.7</td>
<td> 

<table>
<tr><th>A</th><th>B</th><th>S</th><th>C</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
</table>
truth table 1
equation 1
figure 1</td>
<td>1+1+1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II.8</td>
<td> 

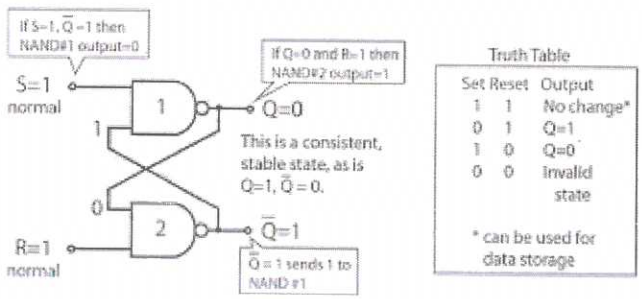
select input output
0 D0
1 D1</td>
<td>1.5+1.5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II.9</td>
<td><table>
<tr><th>Sr. No.</th><th>Parameter</th><th>Asynchronous counter</th><th>Synchronous counter</th></tr>
<tr><td>1.</td><td>Circuit complexity</td><td>Logic circuit is simple.</td><td>With increase in number of states, the logic circuit becomes complicated.</td></tr>
<tr><td>2.</td><td>Connection pattern</td><td>Output of the preceding FF, is connected to clock of the next FF.</td><td>There is no connection between output of preceding FF and CLK of next one.</td></tr>
<tr><td>3.</td><td>Clock input</td><td>All the FFs are not clocked simultaneously.</td><td>All FFs receive clock signal simultaneously.</td></tr>
<tr><td>4.</td><td>Propagation delay</td><td>P.D. = n * (td) where n is number of FF and td is p.d. per FF.</td><td>P.D. = n * (td)FF + (td)gate.
It is much shorter than that of asynchronous counter.</td></tr>
<tr><td>5.</td><td>Maximum frequency of operation</td><td>Low because of the long propagation delay.</td><td>High due to shorter propagation delay.</td></tr>
</table>
any three</td>
<td>1x3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II.10</td>
<td> 

figure 1.5
state table 1.5</td>
<td>1.5
+1.5</td>
<td>3</td>
<td>3</td>
</tr>
</table>

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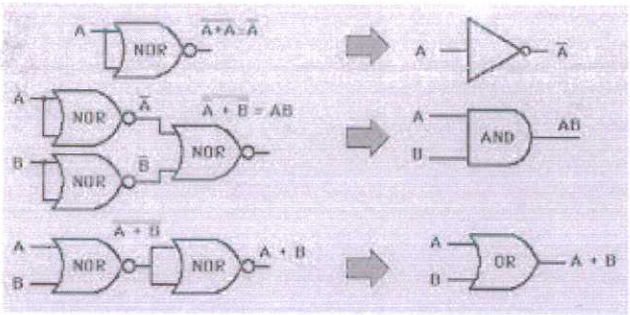
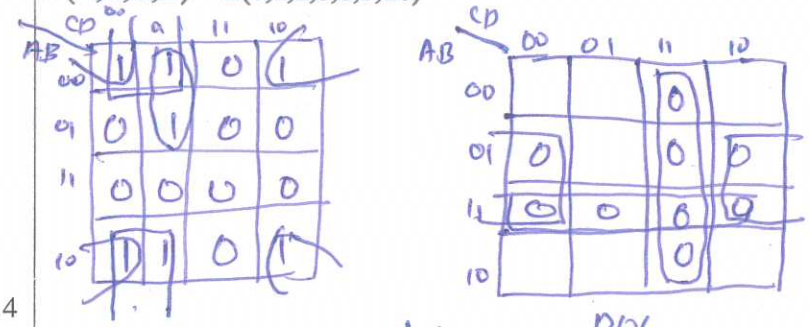
	III - PART C			42
III 1.	**a)** $375_8 = 3x8^2 + 7x8 + 5 = 253_{10}$ **b)** $ABCD_{16} = 1010\ 1011\ 1100\ 1101_2 = 125715_8$ c) $258_{10} = 100000010_2 = 102_{16}$	2+2+3	7	7
III 2a	ASCII is a 7-bit character set containing 128 characters. It contains the numbers from 0-9, the upper and lower case English letters from A to Z, and some special characters. The character sets used in modern computers, in HTML, and on the Internet, are all based on ASCII. A Gray code is an encoding of numbers so that adjacent numbers have a single digit differing by 1. The term Gray code is often used to refer to a "reflected" code, or more specifically still, the binary reflected Gray code.	2+2	4	7
III 2.b	**6 = 0110 , 7 = 0111** **0110 +** **0111** **----------** **1101 since the result is > 9 add 6 to the result** **0110** **-------** **10011 = BCD 0001 0011 = 13_{10}**	3	3	
III. 3		2+3+2	7	7
III.4	**F(A,B,C,D) = Σ(0,1,2,5,8,9,10)**  SOP = B'D' + B'C' + A'C'D POS F' = AB + CD + BD' F = $\overline{AB + CD + BD'}$ = $\overline{AB} \cdot \overline{CD} \cdot \overline{BD'}$ = $(\bar{A}+\bar{B}) \cdot (\bar{C}+\bar{D}) \cdot (B'+D)$ **K map – 2, grouping 2, SOP 1.5, POS 1.5**		2+ 2+ 1.5+ 1.5	7

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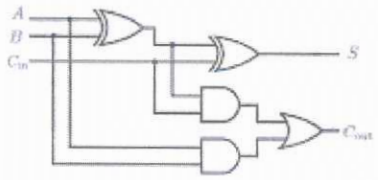
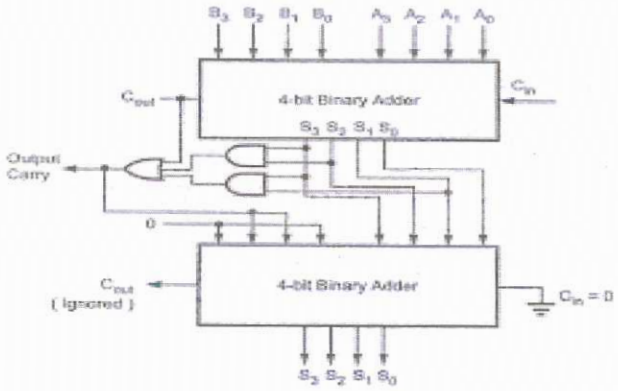
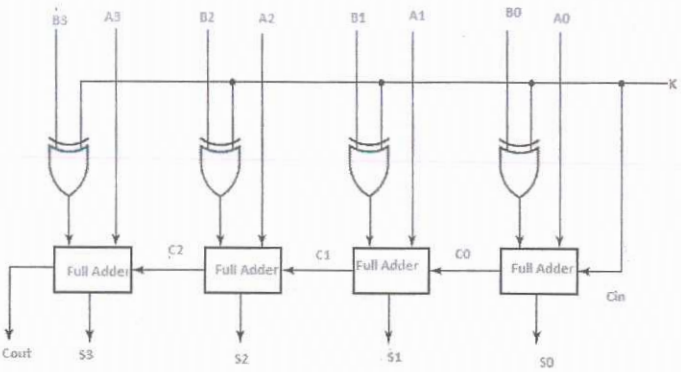
III.5	 **Inputs** / **Outputs** A B C_{in} | S C_{out} 0 0 0 | 0 0 0 0 1 | 1 0 0 1 0 | 1 0 0 1 1 | 0 1 1 0 0 | 1 0 1 0 1 | 0 1 1 1 0 | 0 1 1 1 1 | 1 1	4+3	7	7
III.6	 Fig. 3.32 Block diagram of BCD adder The AND -OR circuit produces c-out when the result of the first adder gives values greater than 1001. in that case, the second adder adds 6 to this result to produce BCD output **circuit 5 marks . Explanation 2 marks**	5 + 2	7	7
III.7	 When input K = 0, the circuit add two 4 bit values. The bits B3,B2,B1 and B0 are transferred to the second inputf of Full adders with out changing. So the circuit acts as an adder. When K = 1, the XOR gates complements the B inputs and Cin also becomes 1 , So the 2's complement of B3,B2,B1,B0 is added by the full adder. So it works as a subtractor.	4+3	7	7

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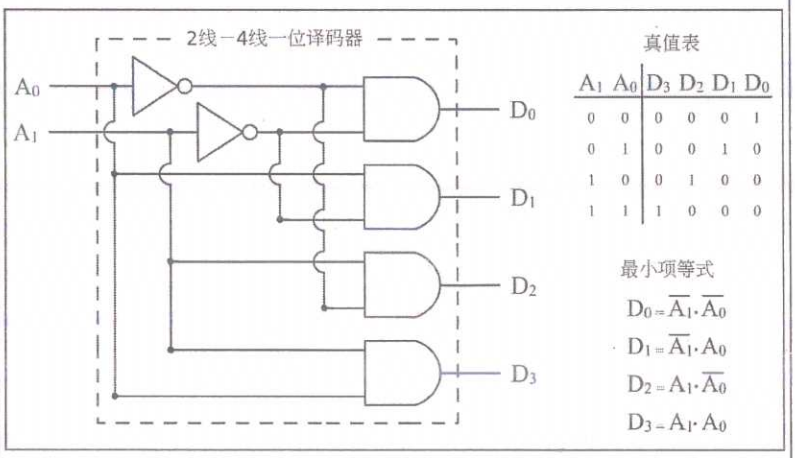
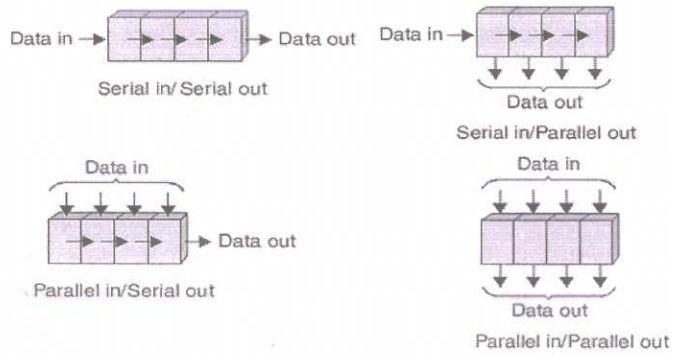
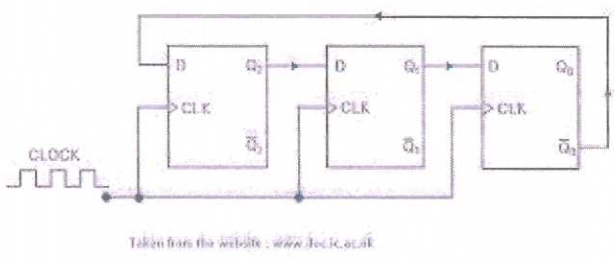
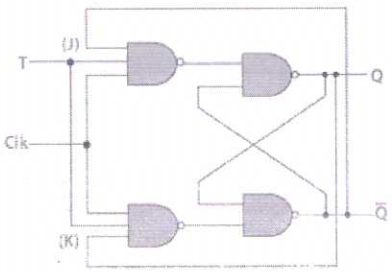
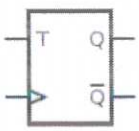
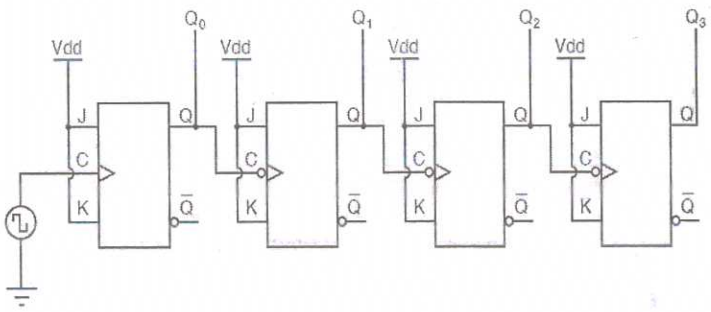
III.8	 **figure 5 marks explanation 2 marks**	5+2	7	7
III.9	 **figure 4 marks explanation 3 marks** The shift register, which allows serial input (one bit after the other through a single data line) and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register. The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register. The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register. The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register.	4+3	7	7
III. 10	 Taken from the website : www.doc-ic.ac.at	4 + 3	7	7

	A ring counter is a typical application of the Shift register. The ring counter is almost the same as the shift counter. The only change is that the output of the last flip-flop is connected to the input of the first flip-flop in the case of the ring c ounter but in the case of the shift resister it is taken as output. Except for this, all the other things are the same. No. of states in Ring counter = No. of flip-flop used **(figure 4 explanation 3)**			
III. 11	The T flip-flop is also called toggle flip-flop. It is a change of the JK flip-flop. The T flip flop is received by relating both inputs of a JK flip-flop. The T flip-flop is received by relating the inputs 'J' and 'K'. When T = 0, both AND gates are disabled.  T flip-flop component and truth table:  Figure 4 explanation 3	4+3	7	7

T	Q	Qnext	Comment
0	0	0	hold state (no clk)
0	1	1	hold state (no clk)
1	0	1	toggle
1	1	0	toggle

III. 12	A four-bit "up" counter  All J and K inputs are connected to VDD so for each clock input ,	4+3	7	7

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	the flip flop toggles. Input clock is given to first flop. The output of this is the LSB. The output of previous one act as the clock of the next flipflop. So second flipflop toggles on every 2nd clock, third flip flop toggles on every 4th clock and fourth one flips on every 8th clock. So ths will produce count sequence from 0000 to 1111 and repeats. **Figure 4 explanation 3**			

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DIGITAL COMPUTER FUNDAMENTALS

TED(21) - 3134

Mark Distribution

Module	Hours/ Module (hi)	Marks/ Module (hi/ H^{i}) * 123 (±5%)	Type of Questions							
			Part A		Part B		Part C		Total	
			No. of questions	Marks	No. of questions	Marks	No. of questions	Marks	No. of questions	Marks
1	8	23 (22-24)	3	3	2	6	2	14	7	23
2	11	32 (30-34)	2	4	4	12	2	14	10	28
3	12	34 (32-36)	2	1	2	6	4	28	7	36
4	12	34 (32-36)	2	1	2	6	4	28	7	36
Total	**43**	**123**	**9**	**9**	**10**	**30**	**12**	**84**	**31**	**123**

Cognitive Level Distribution

Cognitive Level	Marks	% of Marks
Remembering	5	4
Understanding	64	52
Applying	54	44
Total	123	100