TED (15) – 3042

(REVISION - 2015)

Reg. No. 15260496

Signature

THIRD SEMESTER DIPLOMA EXAMINATION IN ENGINEERING/ TECHNOLOGY — APRIL, 2017

DIGITAL ELECTRONICS

(Common for EL, EC and BM)

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer the following questions in one or two sentences. Each question carries 2 marks.

1. Identify Karnaugh map.
2. Define fan out.
3. Identify sequential logic circuit.
4. Tell about binary counter.
5. Memorize modulus of a counter. (5×2 = 10)

PART — B

(Maximum marks : 30)

II Answer *any five* questions from the following. Each question carries 6 marks.

1. State and explain De-Morgans theorem.
2. Subtract the given numbers using 2's complement method.
   (a) $(35)_{10}$-$(28)_{10}$ (b) $(39)_{10}$-$(48)_{10}$
3. Draw the circuit diagram and explain about TTL inverter.
4. Explain the operation of 1 : 4 De-multiplexer with logic diagram.
5. Understand Latches and flip flops.
6. Draw and explain about parallel in parallel out shift registers.
7. Differentiate between synchronous and asynchronous counters. (5×6 = 30)

Marks

PART C

(Maximum marks : 60)

(Answer *one full* question from each unit. Each full question carries 15 marks.)

UNIT – I

III (a) Convert the following decimal numbers into binary and hexa decimal. 8

(i) $(279)_{10}$ (ii) $(346)_{10}$ (iii) $(897)_{10}$ (iv) $(43)_{10}$

(b) Realize EX-OR gate and OR gate using NAND gate only. 7

OR

IV (a) Add the given binary numbers. 4

(i) 110110 + 101101 (ii) 1011011 + 111011

(b) Subtract the given numbers using 1's complement method. 4

(i) 1101 – 0111 (ii) 10110 – 1101

(c) Simplify the given expression using Karnaugh map. 7

$F = \Sigma\, m(0, 2, 3, 6, 10, 14) + d(4, 7)$

UNIT – II

V (a) Define the terms. 8

(i) Noise immunity (ii) Propagation delay

(iii) Current sourcing (iv) Fan in

(b) Draw the logic diagram and explain 4 : 1 multiplexer. 7

OR

VI (a) Design and implement a Full Subtractor. 8

(b) Draw and explain the working of a CMOS NAND gate. 7

UNIT – III

VII (a) Explain JK flip flop using NAND gates with logic diagram. 8

(b) Explain the working of Johnson counter. 7

OR

VIII (a) Draw and explain Serial-in Serial-out shift register. 8

(b) Explain D-flip flop with logic diagram and truth table. 7

UNIT – IV

IX (a) Explain mod-8 synchronous counter using JK flip flop. 8

(b) Draw and explain the working of weighted resistor digital to analog converter. 7

OR

X (a) Explain Successive Approximation type analog to digital converter. 8

(b) Draw and explain 3 bit up/down counter using JK flip flop. 7

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