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Govt Polytechnic College ,Perumbavoor

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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — OCTOBER, 2017

DIGITAL ELECTRONICS

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. List any two non-weighted code.
2. Identify ASCII code.
3. Define a half adder.
4. List any two types of flip-flops.
5. Define resolution of Digital to analog converter. $(5 \times 2 = 10)$

PART — B

(Maximum marks : 30)

II Answer any *five* of the following questions. Each question carries 6 marks.

1. Change the following hexadecimal numbers to binary.
   (i) 10A4 (ii) CF8E (iii) 9742 (iv) 3F.3A
2. Describe BCD code and Excess-3 code.
3. Define the terms in connection with logic gates.
   (i) Noise margin (ii) Propagation delay (iii) fan-out
4. Draw and explain a 1 × 4 De-multiplexer.
5. Describe the working of right shift register with figure.
6. Differentiate between synchronous and asynchronous counters.
7. List different types of ADC and DAC. $(5 \times 6 = 30)$

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Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks)

UNIT — I

III (a) Construct basic logic gates using NAND gates only. 8

(b) Compute the following binary arithmetic operation. 7

(i) 101010 × 11101 (ii) 1111001 × 10101

(iii) 100011 + 11001 (iv) 1010101 + 1111111

OR

IV Design a logic circuit by reducing the logic expression 15

$F = \Sigma m(0,1,2,3,4,7,8,9) + d(10,11,12,13,14,15)$ using K-Map.

UNIT — II

V (a) Explain the operation of 4 × 1 multiplexer with logic diagram. 8

(b) Draw and explain a full adder. 7

OR

VI (a) Draw and explain CMOS NAND gate. 8

(b) Explain half subtractor using NAND gates only with logic diagram. 7

UNIT — III

VII (a) Explain the working of Johnson counter. 8

(b) Discuss JK flip-flop using NAND gates with truth table. 7

OR

VIII (a) Draw and explain the working of serial - in serial - out shift register. 8

(b) Explain D flip-flop with its characteristic table. 7

UNIT — IV

IX (a) Implement mod - 8 synchronous counter using JK flip-flop. 8

(b) Draw and explain weighted resistor type DAC. 7

OR

X (a) Discuss counter type ADC with figure. 8

(b) Draw a 3 - bit up-down counter. 7

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