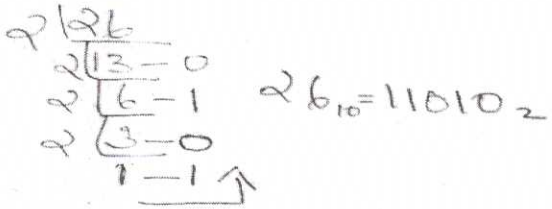
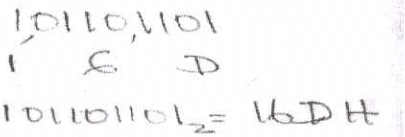
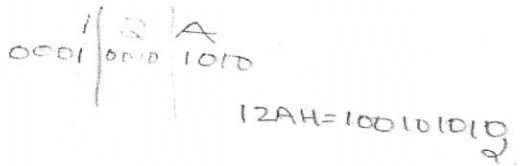
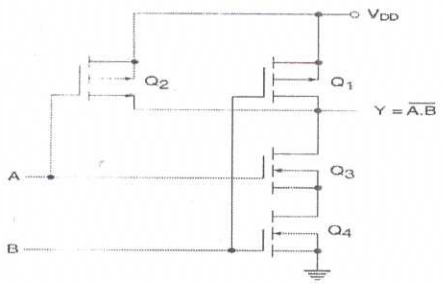
REVISION - 2015

COURSE TITLE - DIGITAL ELECTRONICS CODE - 3042.

Qst no	Scoring Indicator	Split up score	Sub Total	Total
I				
(1)	Excess-3 code, Gray code	2		
(2)	Emitter Coupled Logic	2		
(3)	Using Edge Trigerring, Using Master Slave Flipflops	2		
(4)	Difference between the actual analogue output and the ideal expected output when a given digital input is applied.	2		
(5)	Simplifying logic equations	2	10	10
II(1)	a) 	2		
	b) 	2	6	6
	c) 	2		
II(2)	CMOS NAND gate  Two P-channel MOSFETs (Q1 and Q2 are connected in parallel between VDD and the output terminal, and two N-channel MOSFETs (Q3 and Q4 are connected in series between ground and output terminal. For the output to be in a logic '0' state, it is essential that both the series-connected N-channel devices conduct and both the parallel-connected P-channel devices remain in the cut-off state. This is possible only when both the inputs are in a logic '1' state. When both the inputs are in a logic '0' state, both the	Fig3, exp-3	3+3	6

devices are conducting. which produces a logic '1' at the output. For the remaining two input combinations, either of the two N-channel devices will be nonconducting and either of the two parallel-connected P-channel devices will be conducting. We have either Q3 OFF and Q2 ON or Q4 OFF and Q1 ON. The output in both cases is a logic '1', which verifies the remaining entries of the NAND truth table.

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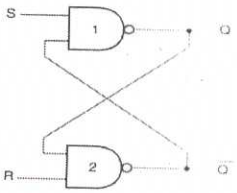
II(3)

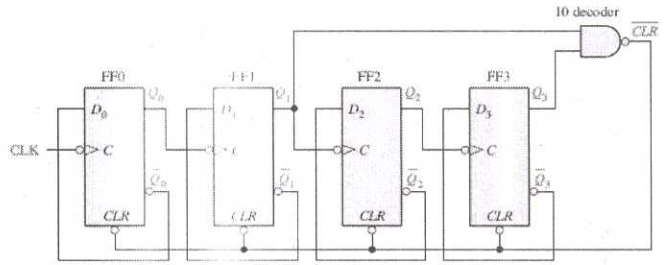
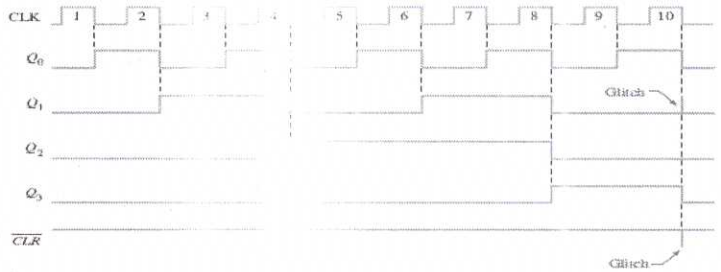
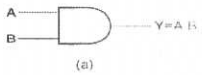
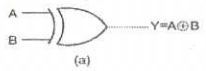
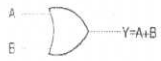


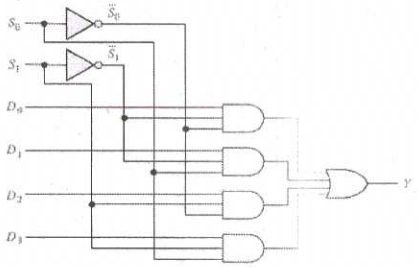
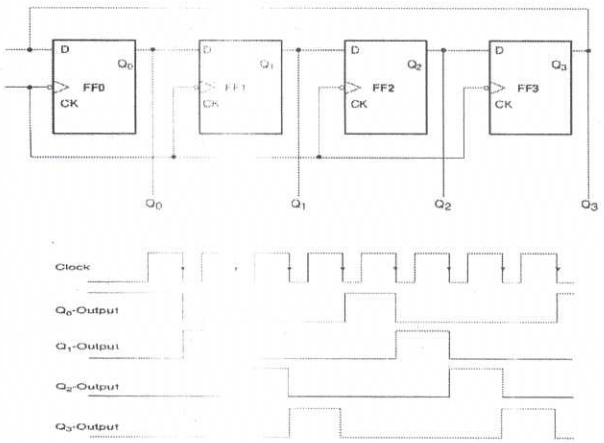
Operation Mode	S	R	Q_{n+1}
No change	1	1	Qn
SET	0	1	1
RESET	1	0	0
Forbidden	0	0	—

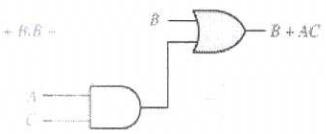
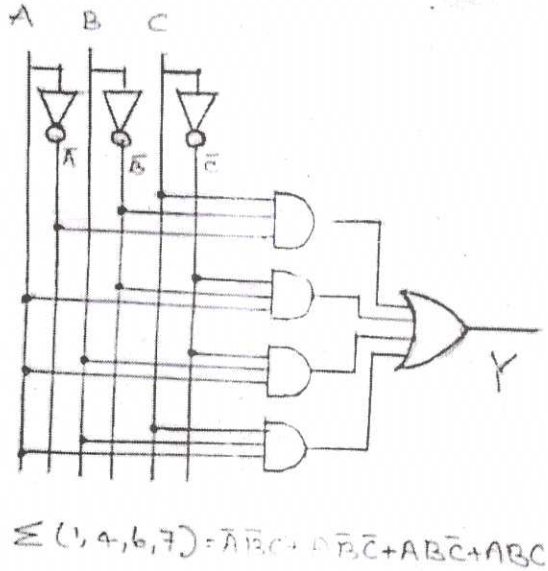
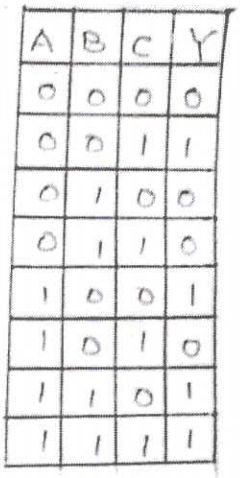
When R = S = 1, the Q output remains in its existing state. In the truth table, Qn represents the existing state and Qn+1 represents the state of the flip-flop after it has been triggered by an appropriate pulse at the R or S input.
Let us assume that Q = 0 initially. This '0' state fed back to one of the inputs of gate 2 ensures that Q = 1. The '1' state of Q fed back to one of the inputs of gate 1 along with S =1 ensures that Q = 0. Thus, R = S = 1 holds the existing stage. Now, if Q was initially in the '1' state and not the '0' state, this '1' fed back to one of the inputs of gate 2 along with R = 1 forces Q to be in the '0' state. The '0' state, when fed back to one of the inputs of gate 1, ensures that Q remains in its existing state of logic '1'. Thus, whatever the state of Q, R = S = 1 holds the existing state. when S = 0 and R = 1. This input combination forces the Q output to the '1' state. On similar lines, the input combination S=1 and R= 0 forces the Q output to the '0' state. When S = R = 0. This implies that both Q and Q outputs should go to the '1' state, as one of the inputs of a NAND gate being a logic '0' should force its output to the logic '1' state irrespective of the status of the other input. This is an undesired state as Q and Q outputs are to be the complement of each other. The input condition (i.e. R = S = 0) that causes such a situation is therefore considered to be an invalid condition and is forbidden.

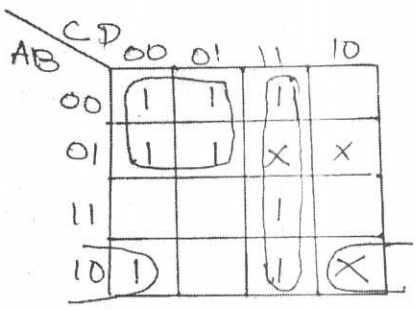
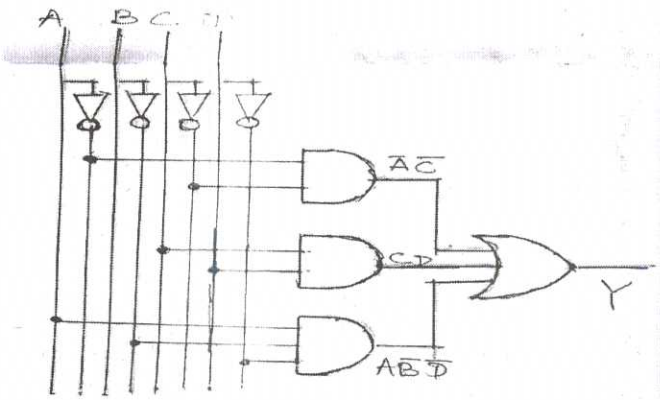
fig+truthtble-3,exp-3 | 3+3 | 6

2

II(4)	 	Ckt-3,timing diagram-3	3+3	6
II(5)	AND  A B Y 0 0 0 0 1 0 1 0 0 1 1 1 (b) EX:OR  A B Y 0 0 0 0 1 1 1 0 1 1 1 0 (b) OR  A B Y 0 0 0 0 1 1 1 0 1 1 1 1	Symbols 3x1=3, truth table 3x1=3	3+3	6

II(6)	 Data-Select Inputs S_1 S_0 Input Selected 0 0 D_0 0 1 D_1 1 0 D_2 1 1 D_3 A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on any one of the inputs to be switched to the output line. Multiplexers are also known as data selectors. The data output is equal to D0 only if S1 = 0 and S0 = 0: The data output is equal to D1 only if S1 = 0 and S0 = 1: The data output is equal to D2 only if S1 = 1 and S0 = 0: The data output is equal to D 3 only if S = 1 and S0 = 1: When these terms are ORed, the total expression for the data output is Y = D0 S1 S0 + D1 S1 S0 + D2 S1 S0 + D3 S1 S0	Fig-2,truth table-1,exp-3	2+1+3	6
II(7)	 Timing diagram of 1000 sequence ring counter A ring counter is obtained from a shift register by directly feeding back the true output of the output flip-flop to the data input terminal of the input flip-flop. If D flip-flops are being used to construct the shift register, the ring counter, also called a circulating register, can be constructed by feeding back the Q output of the output flip-flop back to the D input of the input flip-flop. If J-K flip-flops are being used, the Q and Q outputs of the output flip-flop are respectively fed back to the J and K inputs of the input flip-flop.	Fig-2,timing diagram-2,exp-2	2+2+2	6

III(a)	110011 − 101101 — 2's complement of 101101 is 010010 + 1 = 010011 110011 − 101101 is equal to 110011 + 010011 i.e. 110011 + 010011 = 1 000110 Since the Carry is '1' the answering tve and the result is 110	2s comp-2,add-d,sign-1	2+2+1=5	
III(b)	i) Apply the distributive law to the second and third terms in the expression, as follows: Y= AB + A(B + C) + B(B + C)=AB + AB + AC + BB + BC =AB + AB + AC + B + BC (BB = B = AB + AC + B + BC (AB + AB = AB =AB + AC + B (B + BC = B =B + AC (AB + B = B 	Simp-3,ckt-2	3+2=5	
III(c)	 $\Sigma(1,4,6,7) = \bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C} + ABC$ 	ckt-4,truth table-1	4+1=5	
				15

IV(a)	1. The Gray code is used in the transmission of digital signals as it minimizes the occurrence of errors. 2. The Gray code is preferred over the straight binary code in angle-measuring devices 3. The Gray code is used for labelling the axes of Karnaugh maps. 4. The use of Gray codes to address program memory in computers minimizes power consumption. 5. Gray codes are also very useful in genetic algorithms since mutations in the code allow for mostly incremental changes.	Any four points	4x1.5 =6	
IV(b)	 $Y = \bar{A}\bar{C} + CD + A\bar{B}\bar{D}$  	Map-3,exp-3,ckt-3	3+3+3=9	15

V(a)

A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in}$

$= \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) + A(\bar{B}\bar{C}_{in} + BC_{in})$

$= \bar{A}(A \oplus B)C_{in} + A(\overline{B \oplus C_{in}})$

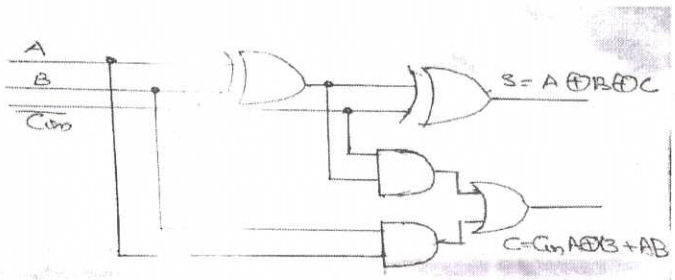
Let $X = B \oplus C_{in}$, Thus $\bar{X} = \overline{B \oplus C_{in}}$

So $S = \bar{A}X + A\bar{X} = A \oplus B \oplus C_{in}$

$C = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC$

$= C_{in}(A \oplus B) + AB(\overline{C_{in} + C_{in}})$

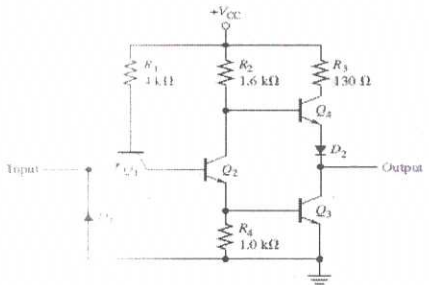
$= C_{in}(A \oplus B) + AB$



Truthtable-2,simplification-4,ckt-2

2+4+2=8

V(b)

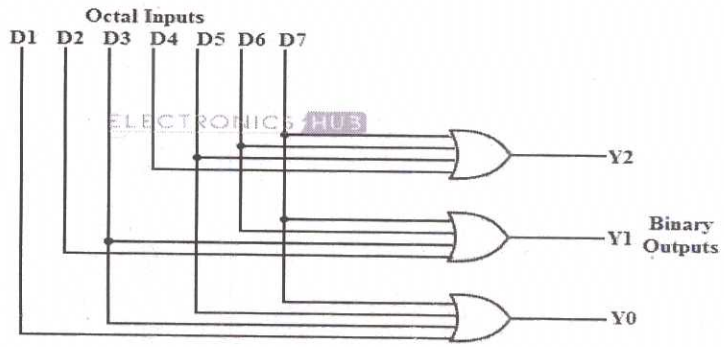


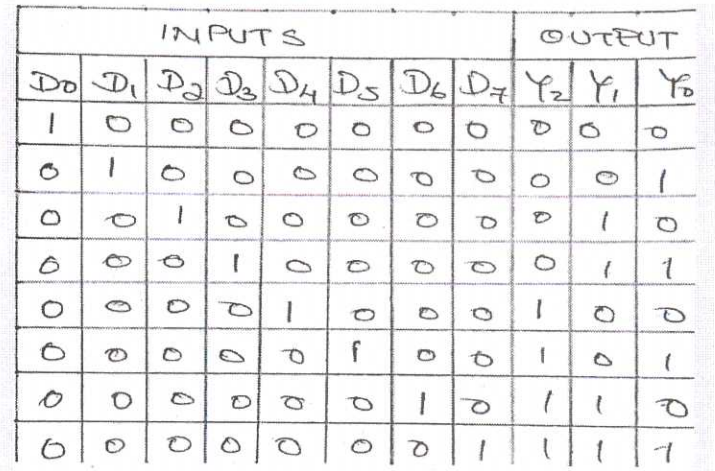
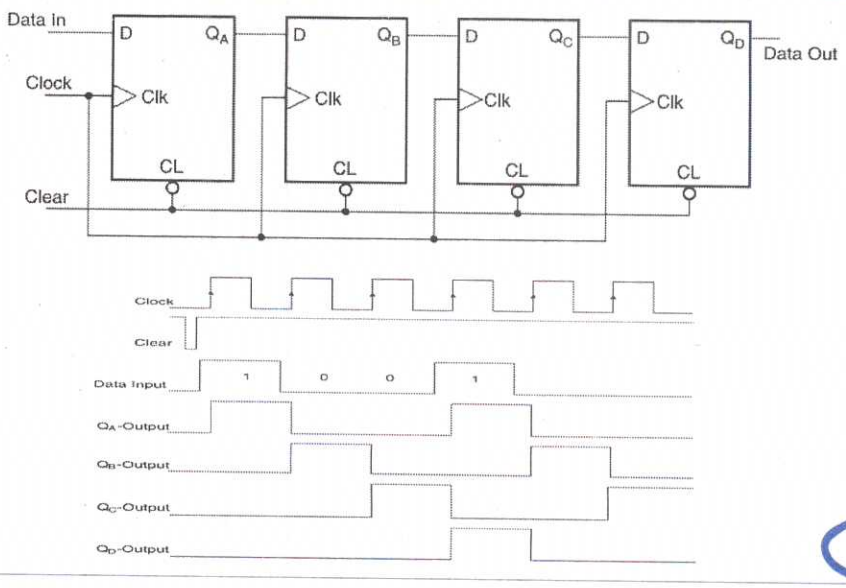
Q1 is the input coupling transistor, and D1 is the input clamp diode. Transistor Q2 is called a phase splitter, and the combination of Q3 and Q4 forms the output circuit often referred to as a totem-pole arrangement.

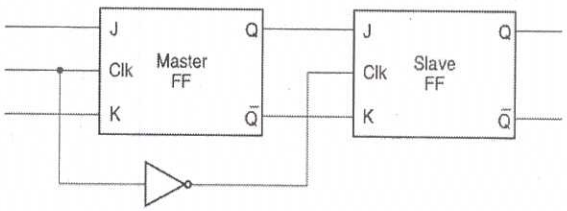
When the input is a HIGH, the base-emitter junction of Q1 is reverse-biased, and the base-collector junction is forward-biased. This condition permits current through R1 and the base-collector junction of Q1 into the base of Q2 , thus driving Q2 into saturation.

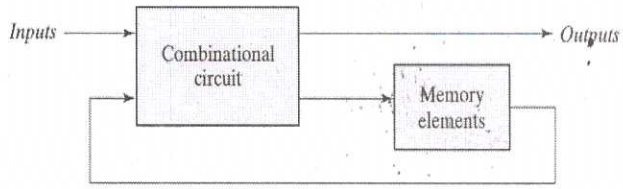
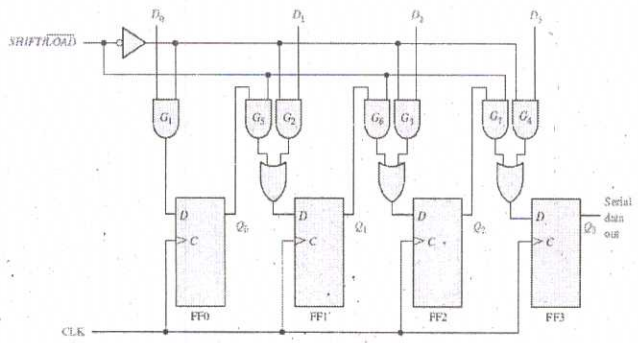
Ckt-3,exp-4

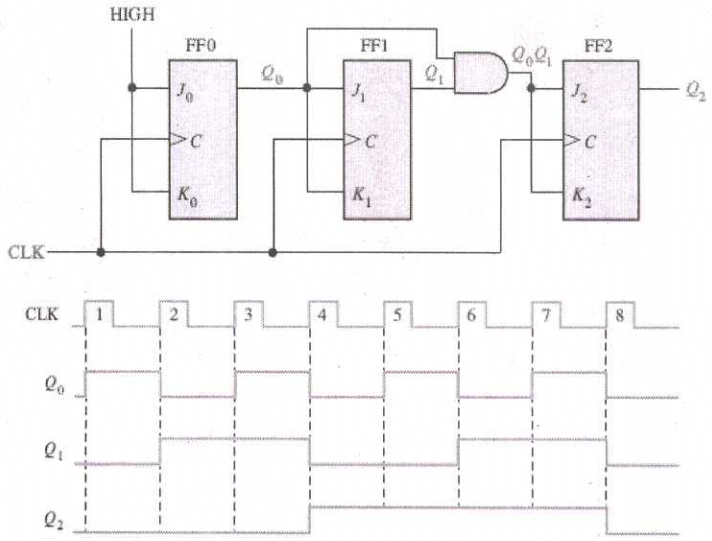
3+4=7

	As a result, Q3 is turned on by Q2 , and its collector voltage, which is the output, is near ground potential. Therefore, there is a LOW output for a HIGH input. At the same time, the collector of Q2 is at a sufficiently low voltage level to keep Q4 off When the input is LOW, the base-emitter junction of Q1 is forward-biased, and the base-collector junction is reverse-biased. There is current through R1 and the base-emitter junction of Q1 to the LOW input. A LOW provides a path to ground for the current. There is no current into the base of Q2 , so it is off. The collector of Q2 is HIGH, thus turning Q4 on. A saturated Q4 provides a low resistance path from VCC to the output; therefore, there is a HIGH on the output for a LOW on the input. At the same time, the emitter of Q2 is at ground potential, keeping Q 3 off. Diode D1 in the TTL circuit prevents negative spikes of voltage on the input from damaging Q1 . Diode D2 ensures that Q4 will turn off when Q2 is on (HIGH input).			15
VI(a)	Encoder An encoder converts an active input signal into a coded output signal. There are n input lines, only one of which is active. Internal logic within the encoder converts this active input to a coded binary output with m bits.  Y0 = D1 + D3 + D5 + D7 Y1 = D2 + D3 + D6 + D7 and Y2 = D4 + D5 + D6 + D7	Ckt-3,truth-2,exp-2	3+2+2=7	

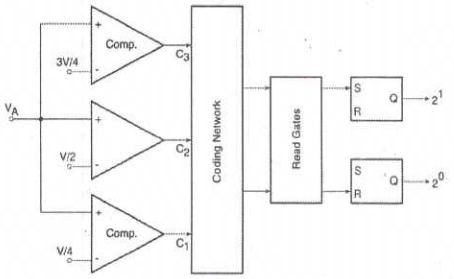
	 A three bit encoder or 8 to 3 encoder consists of 8 inputs and three logic output lines.At any time, only one of these eight inputs can be '1' in order to get the respective binary code. Eg if inputD5 is active then outputs of gates 1 and 3 are high then we get a binary code of 101			
VI(b)	i)Noise immunity. This is the ability to tolerate a certain amount of unwanted voltage fluctuation on its inputs without changing its output state.A measure of a circuit's noise immunity is called the noise margin. ii)Propagation delay tp . It is the time delay between the occurrence of change in the logical level at the input and before it is reflected at the output. It is the time delay between the specified voltage points on the input and output waveforms. iii) Fan-out. The fan-out is the number of inputs of a logic function that can be driven from a single output without causing any false output. It is a characteristic of the logic family to which the device belongs. iv) Fan-in . It is the number of inputs of a logic gate	4x2	8	15
VII (a)	 			

	A reset applied to the CLEAR input of all the flip-flops resets their Q outputs to 0s. The flip-flops shown respond to the LOW-to-HIGH transition of the clock pulses . During the first clock transition, the QA output goes from logic '0' to logic '1'.The outputs of the other three flip-flops remain in the logic '0' state as their D inputs were in the logic '0' state at the time of clock transition. During the second clock transition, the QA output goes from logic '1' to logic '0' and the QB output goes from logic '0' to logic '1', again in accordance with the logic status of the D inputs at the time of relevant clock transition. Thus, a logic '1' that was present at the data input prior to the occurrence of the first clock transition has reached the QB output at the end of two clock transitions. This bit will reach the QD output at the end of four clock transitions. A data bit present at the data input terminal at the time of the nth clock transition reaches the QD output at the end of the (n + 4)th clock transition. During the fifth and subsequent clock transitions, data bits continue to shift to the right, and at the end of the eighth clock transition the shift register is again reset to all 0s. Thus, in a four-bit serial-in serial-out shift register, it takes four clock cycles to load the data bits and another four cycles to read the data bits out of the register.	Ckt-3,timing diagram-2,exp-3	3+2+3=8	
VII (b)	 One way to get race around problem is to use a master–slave configuration. The first flip-flop is called the master flip-flop and the second is called the slave. The clock to the slave flip-flop is the complement of the clock to the master flip-flop. When the clock pulse is present, the master flip-flop is enabled while the slave flip-flop is disabled. As a result, the master flip-flop can change state while the slave flip-flop cannot. When the clock goes LOW, the master flip-flop gets disabled while the slave flip-flop is enabled. Therefore, the slave J -K flip-flop changes state as per the logic states at its J and K inputs. The contents of the master flip-flop are therefore transferred to the slave flip-flop, and the master flip-flop, being disabled, can acquire new inputs without affecting the output. As would be clear from the description above, a master slave flip-flop is a pulse-triggered flip-flop and not an edge-triggered one.	Fig-3,exp-4	3+4=7	15

VIII (a)	 A sequential logic circuit consists of a combinational circuit to which storage elements are connected to form a feedback path. The storage elements are devices capable of storing binary information. The binary information stored in these elements at any given time defines the state of the sequential circuit at that time. The sequential circuit receives binary information from external inputs that, together with the present state of the storage elements, determine the binary value of the outputs. These external inputs also determine the condition for changing the state in the storage elements. The outputs in a sequential circuit are a function not only of the inputs, but also of the present state of the storage elements. The next state of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states . There are two main types of sequential circuits, and their classification is a function of the timing of their signals. A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. The behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.	fig-2,exp-5	2+5=7	
VIII (b)	 For a register with parallel data inputs, the bits are entered simultaneously into their respective stages on parallel lines. There are four data-input lines, D0 , D1 , D2 , and D3 , and a SHIFT /LOAD input, which allows four bits of data to load in parallel into the register. When SHIFT /LOAD is LOW, gates G1 through G4 are enabled, allowing each data bit to be applied to the D input of its respective flip-flop. When a clock pulse is applied, the flip-flops with D = 1 will set and those with D = 0 will reset, thereby storing all four bits simultaneously. When SHIFT /LOAD is HIGH, gates G1 through G4 are disabled and gates G5 through G7 are enabled, allowing the data bits to shift	fig-4,exp-4	4+4=8	

	right from one stage to the next. The OR gates allow either the normal shifting operation or the parallel data-entry operation, depending on which AND gates are enabled by the level on the SHIFT /LOAD input.			15
IX(a)	 A synchronous counter is one in which all the flip-flops in the counter are clocked at the same time by a common clock pulse. First, assume that the counter is initially in the binary 0 state; that is, both flip-flops are RESET. When the positive edge of the first clock pulse is applied, FF0 will toggle and Q0 will therefore go HIGH. let's look at the input conditions of FF1. Inputs J1 and K1 are both LOW because Q0 , to which they are connected, has not yet gone HIGH. There is a propagation delay from the triggering edge of the clock pulse until the Q output actually makes a transition. So, J = 0 and K = 0 when the leading edge of the first clock pulse is applied. This is a no-change condition, and therefore FF1 does not change state. After CLK1, Q0 = 1 and Q1 = 0 . When the leading edge of CLK2 occurs, FF0 will toggle and Q0 will go LOW. Since FF1 has a HIGH (Q0 = 1) on its J1 and K1 inputs at the triggering edge of this clock pulse, the flip-flop toggles and Q1 goes HIGH. Thus, after CLK2, Q0 = 0 and Q1 = 1 When the leading edge of CLK3 occurs, FF0 again toggles to the SET state (Q0 = 1), and FF1 remains SET (Q1 = 1) because its J1and K1 inputs are both LOW (Q 0 = 0). After this triggering edge, Q0 = 1 and Q1 = 1 and so on.	Fig-3,timing-2,exp-3	3+2+3=8	

IX (b)



The simultaneous method of A/D conversion is based on using a number of comparators. The number of comparators needed for n-bit A/D conversion is 2 n −1. The analogue signal to be digitized serves as one of the inputs to each of the comparators. The second input for each of the comparators is a reference input, different for each comparator. The reference voltages to be used for comparators are in general V /2 n , 2V /2 n , 3V /2 n , 4V /2 n and so on. Here, V is the maximum amplitude of the analogue signal that the A/D converter can digitize, and n is the number of bits in the digitized output. The reference voltages for the three comparators will be V /4, V /2 and 3V /4. The output status of various comparators depends upon the input analogue signal VA .

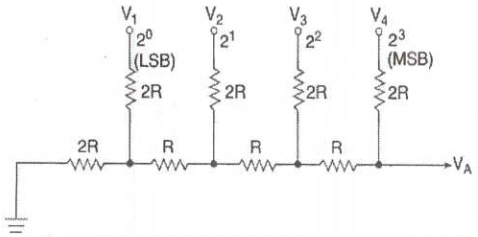
Advantage – extremely fast

Disadvantage – need more comparators for more bits

Input analogue voltage(v_a)	C_1	C_2	C_3	2^1	2^2
0 to $V/4$	LOW	LOW	LOW	0	0
$V/4$ to $V/2$	HIGH	LOW	LOW	0	1
$V/2$ to $3V/4$	HIGH	HIGH	LOW	1	0
$3V/4$ to V	HIGH	HIGH	HIGH	1	1

fig-3,exp-4 | 3+4=7 | 15

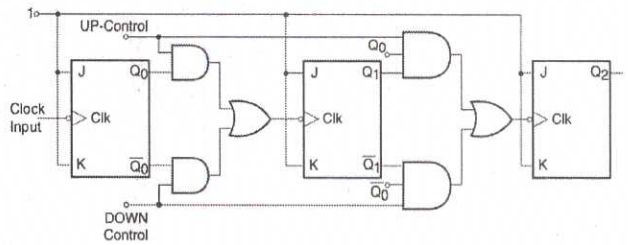
X(a)



The binary ladder, is a resistive network that produces an analogue output equal to the weighted sum of digital inputs. The ladder is made up of only two different values of resistor. This overcomes one of the drawbacks of the resistive divider network.

Output $V_A = \dfrac{V_1 \times 2^0 + V_2 \times 2^1 + V_3 \times 2^2 + V_4 \times 2^3}{2^4}$

Fig-3,exp-4 | 3+4=7

	The analogue output voltage in this case varies from 0 (for an all 0s input) to [(2 n − 1)/2 n]V (for an all 1s input). The LSB contribution to the analogue output is [1/(2 n − 1)]V . This is also the minimum possible incremental change in the analogue output voltage.			
X(b)	 An UP counter is one that counts upwards or in the forward direction by one LSB every time it is clocked. A four-bit binary UP counter will count as 0000, 0001, 0010, 0011, 0100, ..., 1101, 1110, 1111, 0000, 0001, and so on. A DOWN counter counts in the reverse direction or downwards by one LSB every time it is clocked. The four-bit binary DOWN counter will count as 0000, 1111, 1110, 1101, ..., 0100, 0011, 0010, 0001, 0000, 1111, and so on. The counter counts upwards when UP control is logic '1' and DOWN control is logic '0'.	fig-4,exp-4	4+4=8	15

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