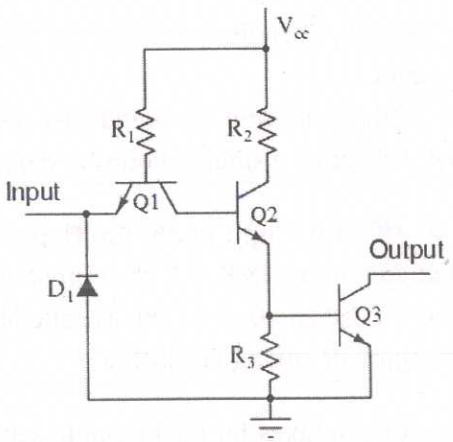
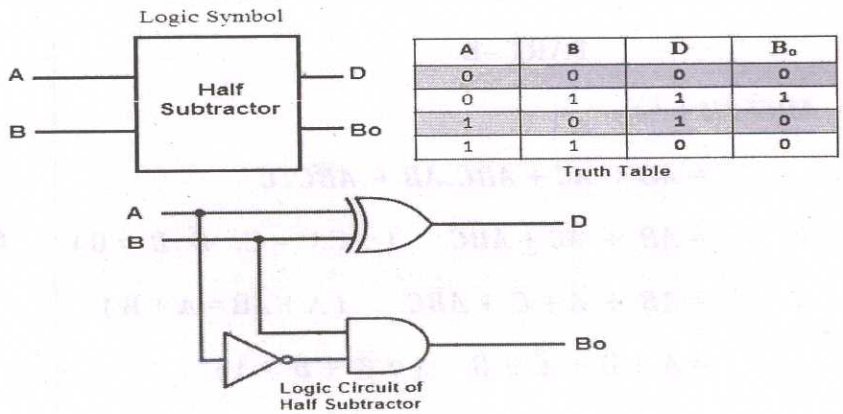
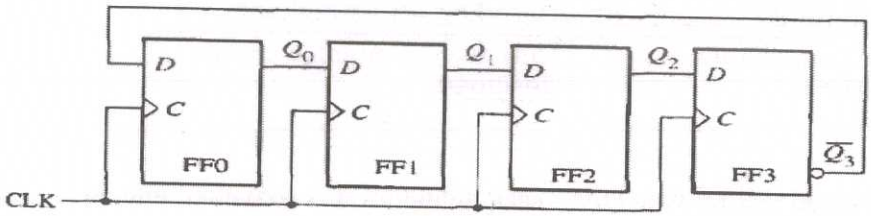
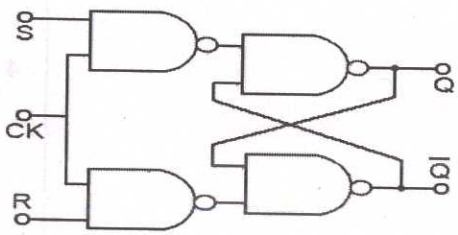
SCORING INDICATORS

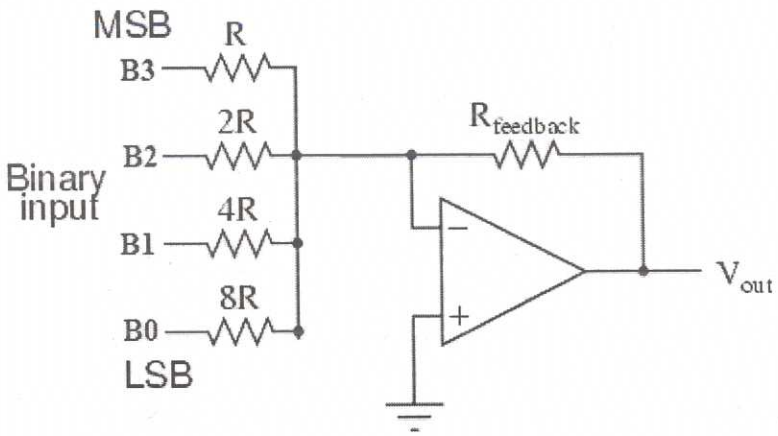
Subject: DIGITAL ELECTRONICS

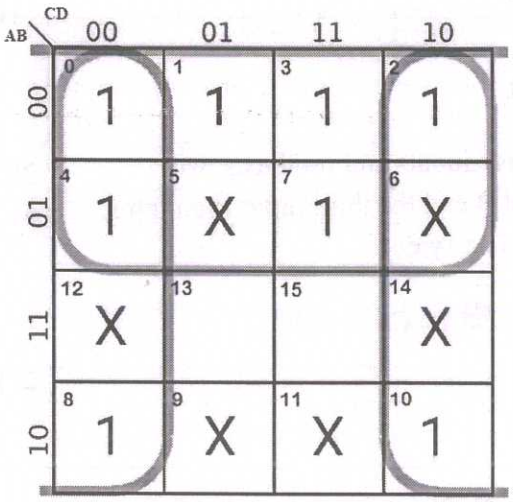
Code & Revision: 3042 (2015)

Qn. No.	Scoring Indicators	Split score	Total Score
I.	**PART – A**		
1.	**BCD code:** It is a type of binary representation for decimal values where each digit is represented by a fixed number of binary bits(usually 4 bits). Eg: $0)_D$ - $0000)_{BCD}$, $9)_D$ - $1001)_{BCD}$ (any one eg.)	1+1	2
2.	Combinational circuits – The output is discovered by the present state of the inputs. Does not store data. Sequential logic circuits - Both the present input and past state output are used to identify the output. Can store a small amount of data.	1+1	2
3.	**Race around condition** of **JK Flip Flop :** In **JK flip flop** as long as clock is high and the input conditions J&K = 1 the output changes or complements its output from 1–>0 and 0 –>1. This is called toggling output or uncontrolled changing or **racing condition**.	2	2
4.	Settling time represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value, after the change in digital input.	2	2
5.	1's complement of the binary number 110010 = 001101 2's complement of the binary number 110010 = 001110	1+1	2
II.	**PART –B**		
1.	$AB + \overline{AC} + A\bar{B}C(AB + C)$ $= AB + \overline{AC} + A\bar{B}C.AB + A\bar{B}C.C$ $= AB + \overline{AC} + A\bar{B}C$ $(\because C.C = C,\ \bar{B}.B = 0)$ $= AB + \bar{A} + \bar{C} + A\bar{B}C$ $(A + \bar{A}B = A + B)$ $= \bar{A} + B + \bar{C} + \bar{B}$ $(\because \bar{B} + B = 1)$ $= \bar{A} + \bar{C} + 1 = 1$	6	6

2.	The basic TTL inverter consists of three stages. A current steering input, a phase splitting stage and an output driver stage. The input stage transistor Q_1 performs a current steering function. The transistor is operated in either forward or reverse mode to steer current to or from the second stage transistor's base, Q_2. Second stage transistor, Q_2 in figure 1, is a phase splitter driving transistor to drive both halves of the pull up and pull down output stage. It allows the input condition to be produced in opposite phases that is Q_3 to be ON (LOW output) when input is HIGH and vice versa.  	3 + 3	6
3.	In half subtractor is used to perform subtraction of two binary digits. The two digits can be represented with A and B. These two digits can be subtracted and gives the resultant bits as difference and borrow. The expression for Difference = A ⊕ B, Borrow = A'B.  A | B | D | Bo 0 | 0 | 0 | 0 0 | 1 | 1 | 1 1 | 0 | 1 | 0 1 | 1 | 0 | 0	2(exp) + 1(LS) + 1(TT) + 2(fig)	6

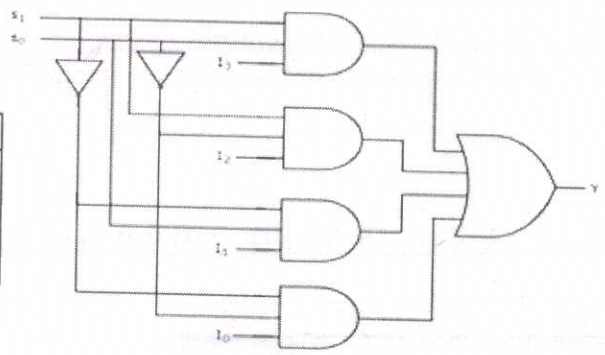
4.	A Johnson counter is a modified ring counter, where the inverted output from the last flip flop is connected to the input to the first. The register cycles through a sequence of bit-patterns. It can be implemented using D-type flip-flops (or JK-type flip-flops).  (a) Clock Q_0 Q_1 Q_2 Q_3 0 0 0 0 0 1 1 0 0 0 2 1 1 0 0 3 1 1 1 0 4 1 1 1 1 5 0 1 1 1 6 0 0 1 1 7 0 0 0 1 (b)	2 + 2 + 2	6
5.	SR flip – flop is a memory device and a binary data of 1 – bit can be stored in it. SR flip – flop has two stable states in which it can store data in the form of either binary zero or binary one. The S and R in SR flip – flop means 'SET' and 'RESET' respectively. If S =1 and R = 0 on clock pulse, then the SR flip – flop is said to be in SET state and the output of the SR flip – flop is SET to 1. If S =0 and R = 1 on clock pulse, then the SR flip – flop is said to be in RESET state and the output of the SR flip – flop is RESET to 0. If S=R= 0 then output remains the same as the previous state. When both in puts are at 1 then the FF will be in an undefined state.  Next-State Table S R Q(n+1) 0 0 Q 0 1 0 (reset) 1 0 1 (set) 1 1 Forbidden	2 + 2 + 2	6

6.	<table><tr><th>Synchronous Counter</th><th>Asynchronous Counter</th></tr><tr><td>All flip flops are triggered with same clock.</td><td>Different clock is applied to different flip flops.</td></tr><tr><td>It is faster.</td><td>It is slower</td></tr><tr><td>Design is complex.</td><td>I Design is relatively easy.</td></tr><tr><td>Decoding errors not present.</td><td>Decoding errors present.</td></tr><tr><td>Any required sequence can be designed</td><td>Only fixed sequence can be designed.</td></tr></table>	3 + 3	6
7.	In the weighted resistor type DAC, each digital level is converted into an equivalent analog voltage or current. It consists of parallel binary weighted resistor bank and a feedback resistor R. This DAC circuit uses weighted values of resistor like R, 2R, 4R, 8R.  	3 + 3	6
III.	**PART – C**		
a)	(i) 101001 – 110 = 100011 (ii) 1001011 ÷ 101 = 1111 (iii) $3024)_D = BD0)_H$ (iv) $91AE)_H = 1001000110101110)_B$ (answer 1 mark , steps 2 mark)	4 x 3	12

b)	In binary number system we only need to use 0 or 1 and which can be easily denoted by the ON (HIGH, denotes 1) and OFF (LOW, denotes 0) condition of a simple switch or two discrete voltage levels.	3	3
IV. a)	$F(A,B,C,D) = \sum(0,1,2,3,4,7,8,10) + d(5,6,9,11,12,14)$  $F = \bar{A} + \bar{D}$ (+ Draw the circuit diagram)	4 (kmap) + 4 (expression) + 4 (fig)	12
b)	Boolean expressions are simplified so that i) The size of the circuitry reduces and the overall speed increases. ii) Decreases the space requirement and power dissipation by reducing the number of logic gates used.	1.5 x 2	3
V. a)	A **multiplexer** is a combinational circuit that selects several analog or digital input signals and forwards the selected input into a single output line. A multiplexer of 2^n inputs has n selected lines, are used to select which input line to send to the output. 4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. $Y = I0\,\overline{S1}\,\overline{S0} + I1\,\overline{S1}\,S0 + I2\,S1\,\overline{S0} + I3\,S1\,S0$	2 + 1 (eqn) +	8

Truth table

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



2 (TT) + 3 (fig)

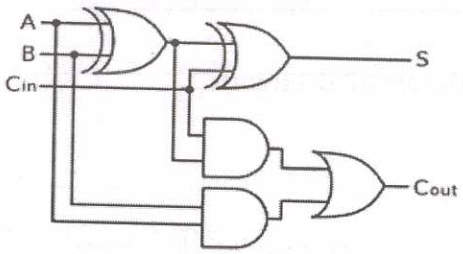
b)

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C_{IN}. The outputs are SUM and carry out.

Sum = A $\oplus$ B $\oplus$ C_{IN} $\quad$ C_{OUT} = (A $\oplus$ B) C_{IN} + AB

Full Adder Truth table

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



2(expln) + 2(TT) + 2(fig) + 1(expression)

7

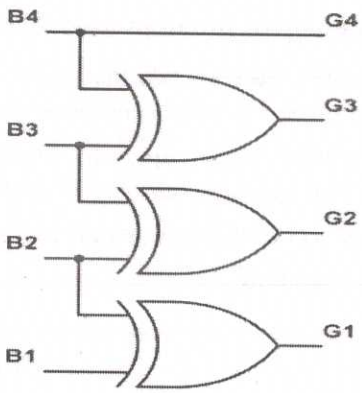
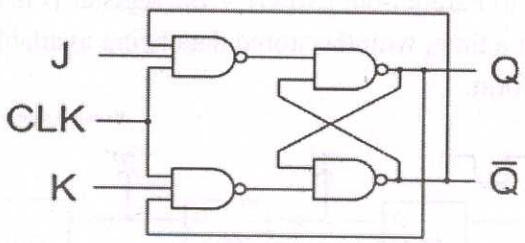
VI. a)

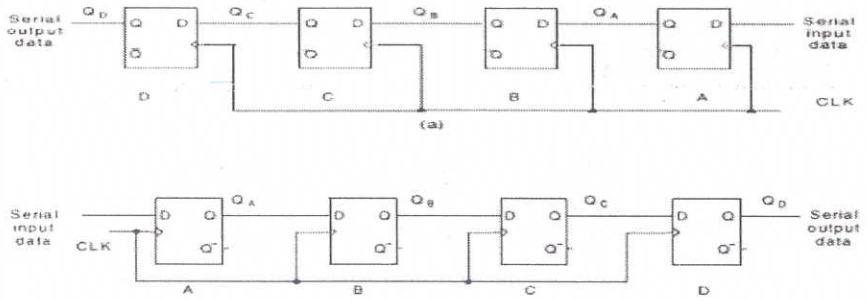
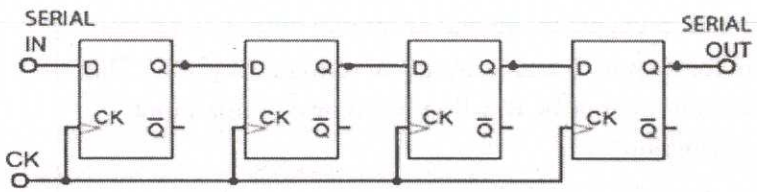
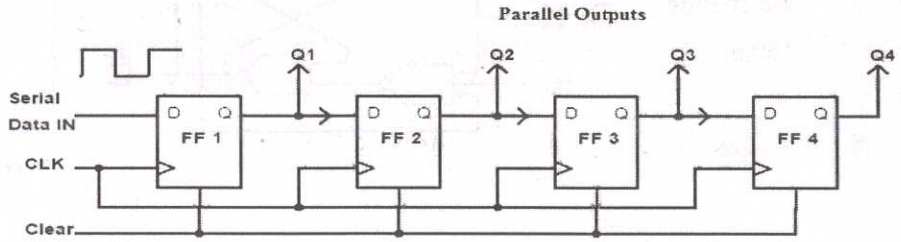
A code converter is a logic circuit that changes data presented in one type of binary code to another type of binary code. The logical circuit which converts the binary code to equivalent gray code is known as binary to gray code converter. The expressions can be obtained from the truth table using k- map simplification.

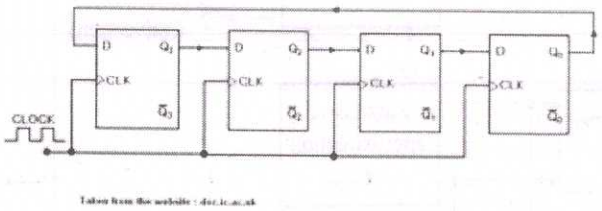
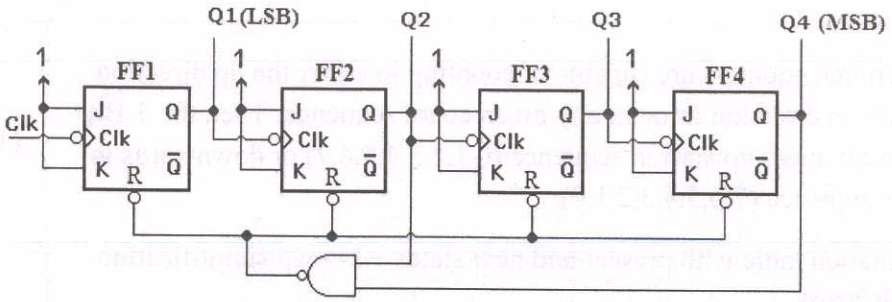
G4 = B4, G3 = B4 $\oplus$ B3, G2 = B3 $\oplus$ B1, G1 = B2 $\oplus$ B1

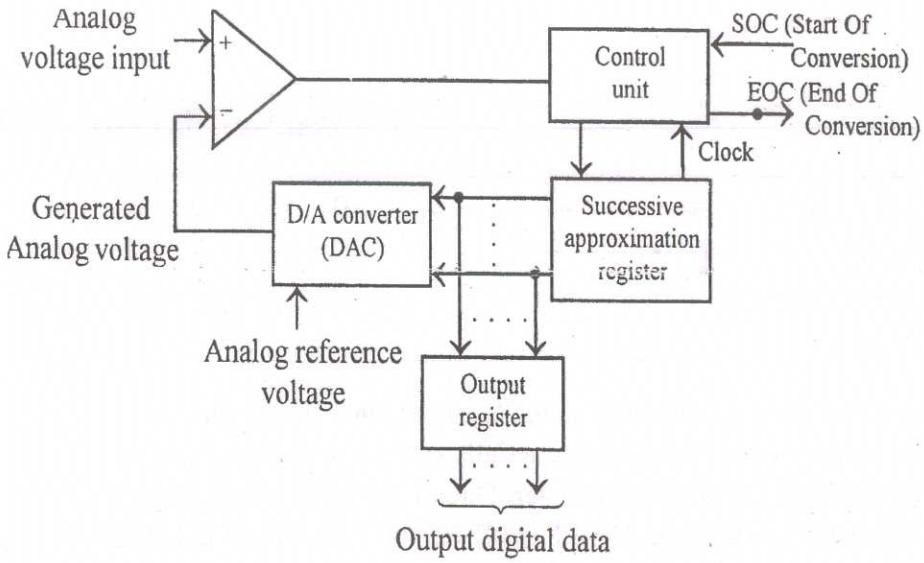
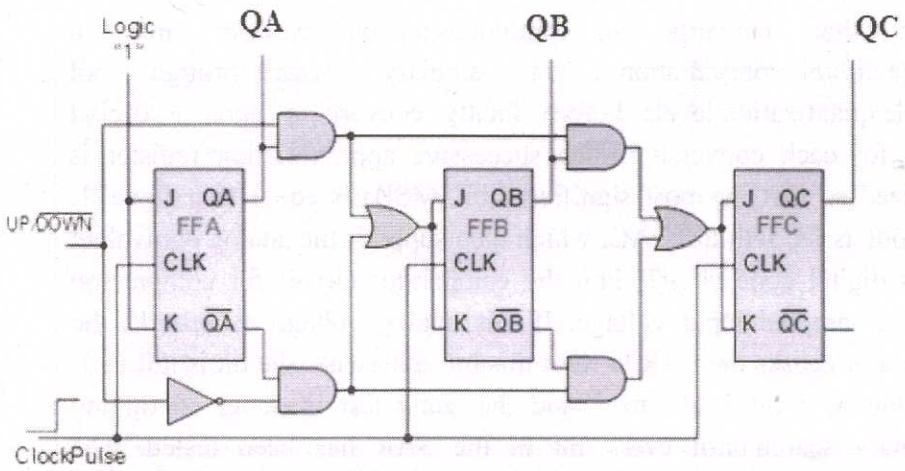
3 (exp) + (kmap 3

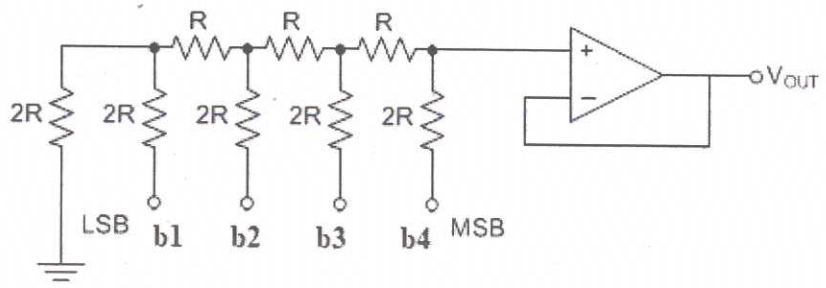
10

	<table><tr><th>Binary</th><th>Gray</th></tr><tr><td>0000</td><td>0000</td></tr><tr><td>0001</td><td>0001</td></tr><tr><td>0010</td><td>0011</td></tr><tr><td>0011</td><td>0010</td></tr><tr><td>0100</td><td>0110</td></tr><tr><td>0101</td><td>0111</td></tr><tr><td>0110</td><td>0101</td></tr><tr><td>0111</td><td>0100</td></tr><tr><td>1000</td><td>1100</td></tr><tr><td>1001</td><td>1101</td></tr><tr><td>1010</td><td>1111</td></tr><tr><td>1011</td><td>1110</td></tr><tr><td>1100</td><td>1010</td></tr><tr><td>1101</td><td>1011</td></tr><tr><td>1110</td><td>1001</td></tr><tr><td>1111</td><td>1000</td></tr></table> 	+ 4 (TT, Dig)	
b)	<table><tr><th></th><th>TTL</th><th>ECL</th><th>CMOS</th></tr><tr><td>Base Gate</td><td>NAND</td><td>OR/NOR</td><td>NAND/NOR</td></tr><tr><td>Fan-in</td><td>12-14</td><td>>10</td><td>>10</td></tr><tr><td>Fan-out</td><td>10</td><td>25</td><td>50</td></tr><tr><td>Power dissipation (mW)</td><td>10</td><td>175</td><td>0.001</td></tr><tr><td>Noise Margin</td><td>0.5V</td><td>0.16V (lowest)</td><td>1.5V (Highest)</td></tr><tr><td>Propagation Delay (ns)</td><td>10</td><td><3 lowest</td><td>15 Highest</td></tr><tr><td>Noise immunity</td><td>Very good</td><td>good</td><td>excellent</td></tr></table>	5	5
VII. a)	The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations.(+ explanation) <table><tr><th colspan="4">JK latch truth table</th></tr><tr><th>J</th><th>K</th><th>Q_{next}</th><th>Comment</th></tr><tr><td>0</td><td>0</td><td>Q</td><td>No change</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Reset</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Set</td></tr><tr><td>1</td><td>1</td><td>$\overline{Q}$</td><td>Toggle</td></tr></table> 	2 + 3 (TT) + 3 (fig)	8

b)	Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. The registers which will shift the bits to left are called "Shift left registers". The registers which will shift the bits to right are called "Shift right registers".  	3 + 2 + 2	7
VIII. a)	The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**. Shift registers operate in one of four different modes. Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.  Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.  	4 + 4	8

b)	A **ring counter** is a type of **counter** composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "**ring**" structure. (+ explanation)  Taken from the website : doc.ic.ac.uk Q_0 Q_1 Q_2 Q_3 1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 1	3 + 2 (fig) + 2 (TT)	7
IX. a)	An Asynchronous counter count using Asynchronous clock input. In asynchronous counter Flip-flops are serially connected together and the clock pulse ripples through the counter. Due to the ripple clock pulse, it's often called a ripple counter. Here J and K inputs of the FF are held high so that the output toggles for each clock pulse. The FF start counting from 0000 and the FF are reset after 1001. (Explanation and truth table)  	4 + 4	8
b)	A **successive approximation ADC** is a type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion. The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left as 1. Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested. The	3 + 4	7

	resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).  		
X. a)	Bidirectional counters are capable of counting in either the up direction or the down direction through any given count sequence. Then the 3-Bit counter advances upward in sequence (0,1,2,3,4,5,6,7) or downwards in reverse sequence (7,6,5,4,3,2,1,0). (+ excitation table with present and next states + k- map simplification for each state)  	3 (TT) + 2 (eqn) + 3 (fig)	8

b)	The following circuit diagram shows the basic 2 bit R-2R ladder DAC circuit using op-amp. Here only two values of resistors are required i.e. R and 2R. The R-2R resistor ladder network directly converts a parallel digital symbol/word into an analog voltage. Each digital input (b1, b2, b3 and b 4) adds its own weighted contribution to the analog output.	2	
	$V_{out} = -V_{ref}\left(b_3 \frac{1}{2} + b_2 \frac{1}{4} + b_1 \frac{1}{8} + b_0 \frac{1}{16} \right)$	+	
	(+ explanation)	2 (eqn)	
		+ 3 (fig)	7