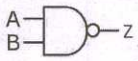
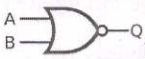
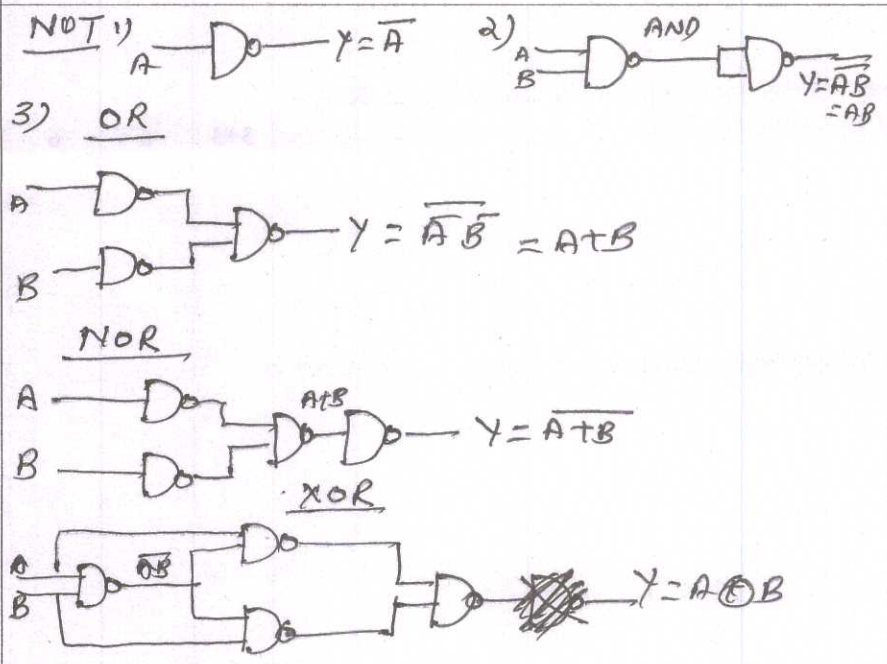
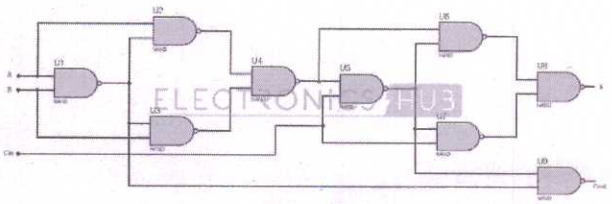
SCHEME OF VALUATION
(Scoring indicators)

A	**Revision : 2015** **Course Code:** 3042 **Course Title : DIGITAL ELECTRONICS**			
Q No.	**Scoring Indicator**	**Split up score**	**Sub Total**	**Total**
I	**PART -A**			
1	The radix of a number system indicates the number of unique symbols used in that system.	2	2	
2	 **NAND gate**  **NOR gate**	2	2	
3	**Fan**-in is a term that **defines** the maximum number of digital inputs that a single logic **gate** can accept.	2	2	
4	Data transfer ,data storage,,as ring counter and Johnson counter.	2	2	
5	Flash type, Dual slope and Successive approximation type.(any two)	2	2	
II	**PART B**			
1	**a) 1011-11 b) 1101101- 109 c)1101110.011-110.375**	**2x3 =6**		**6**
2		**Explanation3 + TRUTH TABLE**	Fig 3 **3**	**6**

A \ BC_{IN}	00	01	11	10
0	0	0	1	0
1	0	1	1	1

For Carry – out COUT

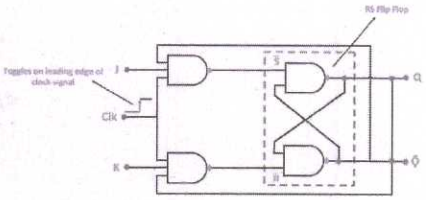
The simplified equation for COUT is COUT = AB + ACIN + BCIN



Full Adder using NAND Gates

Full adder is a simple 1 – bit adder. If we want to perform n – bit addition, then n number of 1 – bit full adders should be used in the form of a cascade connection.

5 . The **circuit diagram** of the JK Flip Flop is shown in the figure below.



Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\bar{Q}_0$ (toggles)

3+3 6

The S and R inputs of the RS bistable have been replaced by the two inputs called the J and K input respectively. Here J = S and K = R. The two input AND gates of the RS flip-flop is replaced by the two 3 inputs NAND gates with the third input of each gate connected to the outputs at Q and $\bar{Q}$. This cross coupling of the RS Flip-Flop is used to produce toggle action. As the two inputs are interlocked.

Operation.

- Initially, a short negative going pulse is applied to the clear input of all flip-flops. This will reset all the flip-flops. Hence, initially the o/ps are Q3Q2Q1Q0Q3Q2Q1Q0 =0000.
- But Q3Q3'=1 and since it is copied to J0J0 it is also equal to 1.
- J0J0 =1 and K=0.....initially.
- On the first negative edge of clock arrives at first f/f. o/p of Q0Q0 =1.
- after 1st –ve edge clock the o/ps of f/fs will be,

Q3Q2Q1Q0Q3Q2Q1Q0 =0001

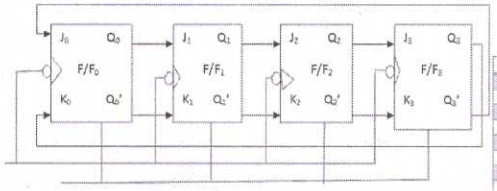
- On second –ve clock o/p of 2nd f/f will be 1 i.e Q1Q1 =1.
- Q3Q2Q1Q0Q3Q2Q1Q0 =0011
- Similarly for 3rd –ve edge clock,

  Q3Q2Q1Q0Q3Q2Q1Q0=0111
- For 4th –ve edge clock,

  Q3Q3Q2Q2Q1Q1Q0=1111Q0=1111 - Now as soon as 5th –ve edge is arrived o/p of 1st f/f becomes 0 i.e Q0Q0=0
  i.e Q3Q2Q1Q–0Q3Q2Q1Q–0 =1110 - This operation continues till the o/p is reached to zero o/p state. i.e Q3Q2Q1Q0Q3Q2Q1Q0 =0000

Logic diagram:-

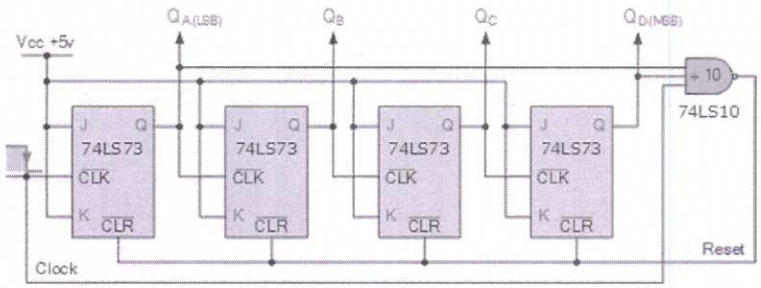
3+3 6



States	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

7.

Asynchronous Decade Counter



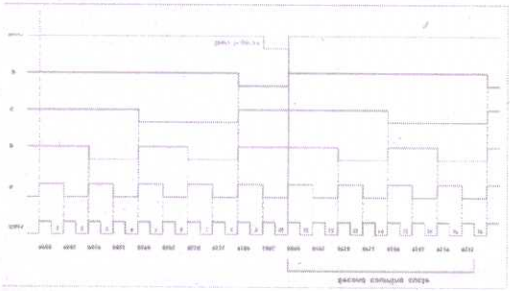
3+3 6

This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9). Both outputs QA and QD are now equal to logic "1". On the application of the next clock pulse, the output from the 74LS10 NAND gate changes state from logic "1" to a logic "0" level.

As the output of the NAND gate is connected to the CLEAR (CLR) inputs of all the 74LS73 J-K Flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10. As outputs QA and QD are now both equal to logic "0" as the flip-flop's have just been reset, the output of the NAND gate returns back to a logic level "1" and the counter restarts again

Input Pulses	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
0	0	0	0	0 (resets)

from 0000.



PART-C

III

a)

1) 11011+1101= 101000 2)10111.101+110111.01=1001110.111

3)1110-1001=0101 4)1010-1101=1101 (2's complement of answer)

2x4 8

1110+	1010+
0001	0011
1.0101 discard carry	1101

b) **DeMorgan's** Theory

DeMorgan's first **theorem** states that two (or more) variables NOR'ed together is the same as the two variables inverted (Complement) and AND'ed, while the second **theorem** states that two (or more) variables NAND'ed together is the same as the two terms inverted (Complement) and OR'ed.

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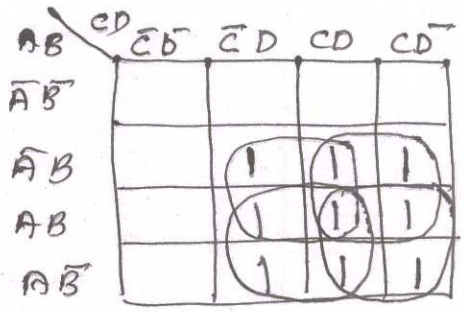

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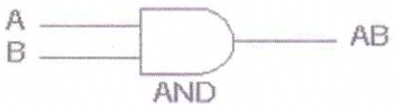
$Y = BD + BC + AD + AC$

(b)

Logic gates

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

AND gate



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB

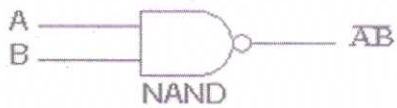
3x3

~~Circuit& wave form (2+2)~~

9

~~4~~

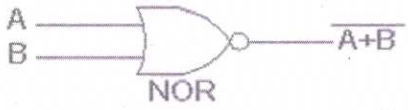
NAND gate



2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

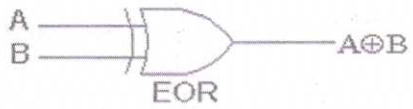
NOR gate



2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.
The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

EXOR gate



2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation

(b)

1) $A(\bar{A}+BC) = A\cdot\bar{A}+ABC$

$= \underline{ABC}$

2) $A(BC+\bar{B}C) = ABC+A\bar{B}C$

$= AC(B+\bar{B})$

$= AC$

3) $AAB(\bar{A}BC+BBC)$

$= AAB\cdot\bar{A}BC+AABBBC$

$= 0+ABBC = \underline{ABC}$

2X3 6

15

V(a)

TTL- Transistor Transistor Logic

- This logic family basic TTL gate has improvence over standard DTL gate.
- TTL gate has 3 different type of output configurations:
  1. open collector output
  2. totem pole output
  3. three state output (tristate)
- Totem pole provide less power dissipation, high speed of operation and high fanout
- Standard TTL series of logic families starts with 7404,74586 &74ALs161
- The other two families are for military and industrial application

  54-military

  84-industrial

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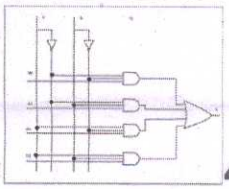
ECL- Emitter Coupled Logic

- ECL is based on use of current steering switch realised using differential transistor pair.
- ECL is fastest logic family among all and this is due to avoidance of saturation region for application
- Following are characteristics of ECL logic family
  1. Propagation rate is about 1 to 2ns
  2. Noise immunity and power dissipation is worst of all the logic families.
  3. High Level is 0.8V and Low Level 1.8V
  4. it has differential input amplifier, internal temperature and voltage compensated bias network; either follower output
- ECL gate provide both true as well as complemented outputs

4

(b)



4-to-1 Multiplexer

3

The 4X1 multiplexer comprises 4-input bits, 1- output bit, and 2-control bits. The four input bits are namely 0, D1, D2 and D3, respectively; only one of the input bit is transmitted to the output. The o/p 'q' depends on the value of control input AB. The control bit AB decides which of the i/p data bit should transmit the output. The following figure shows the 4X1 multiplexer circuit diagram using AND gates. For example, when the control bits AB =00, then the higher AND gate are allowed while remaining AND

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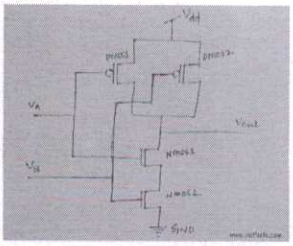
gates are restricted. Thus, data input D0 is transmitted to the output 'q"

VI(a)



The above drawn circuit is a 2-input CMOS NAND gate. Now let's understand how this circuit will behave like a NAND gate. The circuit output should follow the same pattern as in the truth table for different input combinations.

3

Case-1 : V_A – Low & V_B – Low

As V_A and V_B both are low, both the pMOS will be ON and both the nMOS will be OFF. So the output V_{out} will get two paths through two ON pMOS to get connected with V_{dd}. The output will be charged to the V_{dd} level. The output line will not get any path to the GND as both the nMOS are off. So, there is no path through which the output line can discharge. The output line will maintain the voltage level at V_{dd}; so, High.

Case-2 : V_A – Low & V_B – High

8

V_A – Low: pMOS1 – ON; nMOS1 – OFF

V_B – High: pMOS2 – OFF; nMOS2 – ON

pMOS1 and pMOS2 are in parallel. Though pMOS2 is OFF, still the output line will get a path through pMOS1 to get connected with V_{dd}. nMOS1 and nMOS2 are in series. As nMOS1 is OFF, so V_{out} will not be able to find a path to GND to get discharged. This in turn results the V_{out} to be maintained at the level of V_{dd}; so, High.

Case-3 : V_A – High & V_B – Low

5

V_A – High: pMOS1 – OFF; nMOS1 – ON

V_B – Low: pMOS2 – ON; nMOS2 – OFF

The explanation is similar as case-2. V_{out} level will be High.

Case-4 : V_A – High & V_B – High

V_A – High: pMOS1 – OFF; nMOS1 – ON

V_B – High: pMOS2 – OFF; nMOS2 – ON

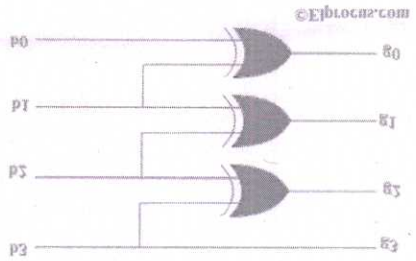
In this case, both the pMOS are OFF. So, V_{out} will not find any path to get connected with V_{dd}. As both the nMOS are ON, the series connected nMOS will create a path from V_{out} to GND. Since, the path to ground is established, V_{out} will be discharged; so, Low.

In all the 4 cases we have observed that V_{out} is following the exact pattern as in the ruth table for the corresponding input combination.

(b)

Binary to Gray Code Converter

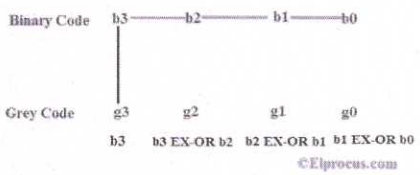
Binary code is a very simple representation of data using two values such as 0's and 1's, and it is mainly used in the world of the computer. The binary code could be a high (1) or low (0) value or else even a modify in value. Gray code or reflected binary code estimates the binary code nature that is arranged with on & off indicators, usually denoted with ones & zeros. These codes are used to look at clarity as well as error modification in binary communications The step by step gray code generation is shown below.



Binary to Gray Code Conversion Logic Circuit

This method uses an Ex-OR gate to perform among the binary bits. The following best example will be very useful for knowing the conversion of binary to gray. In this conversion method, take down the MSB bit of the present binary number, as the primary bit or MSB bit of the gray code number is similar to the binary number **Example of Binary to Gray Code Converter**

Let assume the Binary code digits be bo, b1, b2, b3 whereas the particular Gray Code can be attained based on the following concept.



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7 15

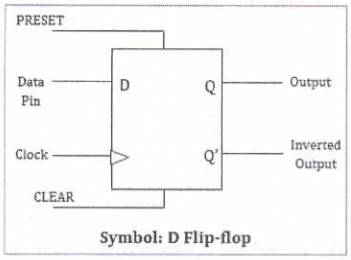
VII

(a)
VII

D Flip-flop:

D Flip-flops are used as a part of memory storage elements and data processors as well. D flip-flop can using NAND gate or with NOR gate. Due to its versatility they are available as IC packages. The major applications of D flip-flop are to introduce delay in timing circuit, as a buffer, sampling data at specific intervals. D flip-flop is simpler in terms of wiring connection compared to JK flip-flop. Here we are using **NAND gates** for demonstrating the D flip flop

Whenever the clock signal is LOW, the input is never going to affect the output state. The clock ha high for the inputs to get active. Thus, D flip-flop is a controlled Bi-stable latch where the clock signal i control signal. Again, this gets divided into **positive edge triggered D flip flop and negative edge trig flip-flop**. Thus, the output has two stable states based on the inputs which have been discussed below.



Symbol: D Flip-flop

4

Clock	INPUT	OUTPUT	
	D	Q	Q'
LOW	x	0	1
HIGH	0	0	1
HIGH	1	1	0

8

T Flip-flop:

The name T flip-flop is termed from the nature of toggling operation. The major applications of T flip-fl counters and control circuits. **T flip flop is modified form of** JK flip-flop making it to operate in toggli region.

Whenever the **clock signal is LOW, the input is never going to affect the output state**. The clock has high for the inputs to get active. Thus, T flip-flop is a controlled Bi-stable latch where the clock signal is control signal. Thus, the output has two stable states based on the inputs which have been discussed belo

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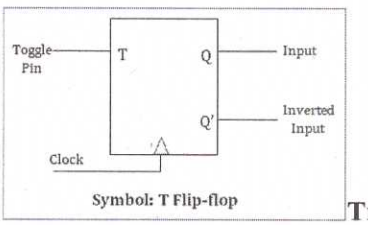

Symbol: T Flip-flop

Truth Table of T Flip Flop:

Clock	INPUT		OUTPUT	
	RESET	T	Q	Q'
X	LOW	X	0	1

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(b) A flip-flop is a bistable device. its output remains either low or high. The high state is 1 called SET state and Low called RESET state. JK flipflop is most versatile flipflop and most commonly used when descrete devices are used implement arbitary state machine. JK flipflop gate configuration is shown here with refined version of RS flipflop

3

JK flipflop has three inputs and two outputs. Outputs are complementary to each other.
when j = k = 0 and clk = 1; output of AND gates will be 0; when any one input of NOR gate is 0 output of NOR ga complement of other input, so output remains as previous output.

7

when j =0 k =1 and clk = 1; output of AND gate connected to K will be Q and corresponding NOR gate output w which RESETs the flipflop.

when j =1 k = 0 and clk = 1; output of AND gate connected to j will be Q' and corresponding NOR gate output w which the SETs the flipflop.

4

when j =1 k = 1 and clk = 1; Q output will toggle as long as CLK is high.Thus the output will be unstable creating around problem with this basic JK circuit. This problem is avoided by ensuring that the clock input is at logic "1" a very short time, or to produce a more sophisticated JK flip-flop circuit called a Master–slave flip-flop.

VIII (a)

Serial In Serial Out (SISO) shift registers are a kind of shift registers where both data loading as well as data retr to/from the shift register occurs in serial-mode. Figure 1 shows a n-bit synchronous **SISO shift register** sensitive positive edge of the clock pulse. Here the data word which is to be stored is fed bit-by-bit at the input of the firs flop. Further it is seen that the inputs of all other flip-flops (except the first flip-flop FF_1) are driven by the outpu preceding ones say for example, the input of FF_2 is driven by the output of FF_1. At last the data stored within the is obtained at the output pin of the n^{th} flip-flop in serial-fashion.

4

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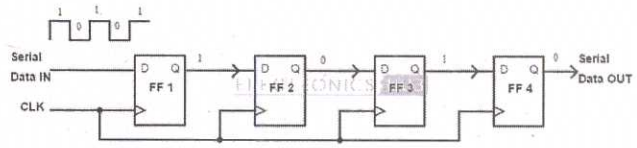

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(b) **Ring counter** is a type of counter composed of flip-flops connected into a shift register, with the output last flip-flop fed to the input of the first, making a "circular" or "ring" str

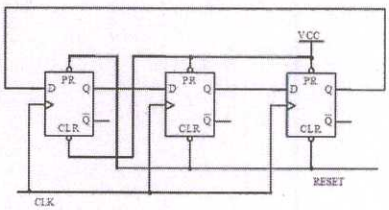
3 7

Straight ring counter

State Q0 Q1 Q2 Q3

IX (a)

0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
0	1	0	0	0



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Both Synchronous and Asynchronous counters are capable of counting "Up" o counting "Down", but their is another more "Universal" type of counter that can coun both directions either Up or Down depending on the state of their input contro pin a these are known as **Bidirectional Counters**.

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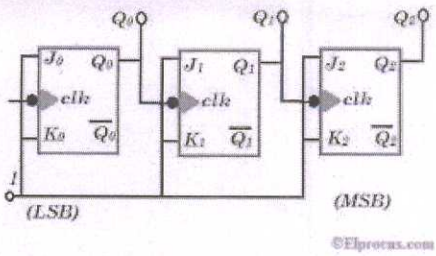
Bidirectional counters, also known as Up/Down counters, are capable of counting in direction through any given count sequence and they can be reversed at any point v their count sequence by using an additional control input as shown below.



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b)

SYNCHRONOUS CIRCUIT	ASYNCHRONOUS CIRCUIT
All the **State Variable** changes are synchronized with a universal clock signal.	The **State Variables** are not synchronized to change simulteneously and may change at anytime irrespective of each other to achieve the next **Steady Internal State**
Since all the Internal State changes are in the strict control of a master clock source they are less prone to failure or to a race condition and hence are more reliable.	Since there is no such universal clock source, the internal state changes as soon as any of the inputs change and hence are more prone to a race condition.
Timings of the internal state changes are in our control.	The changes in the internal state of an asynchronous circuit are not in our control.

3+3

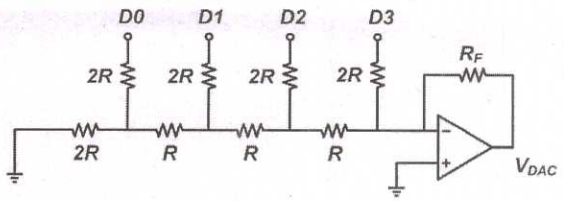
6

15

Xa)

basic four-bit R-2R voltage-mode DAC is shown in Figure 3. The digital code s
be applied to the inputs D3...D0, where D3 is the most significant bit (MSb) and D0 i
least significant bit (LSb).

As you can see, there are two different resistor values (R and 2R) in the ladder netwo



4

8

Circuit Operation

Now let's examine the circuit operation. Assume that D0 is connected to V_{REF} and the
bits are logic low; we obtain the circuit in Figure 5.

4

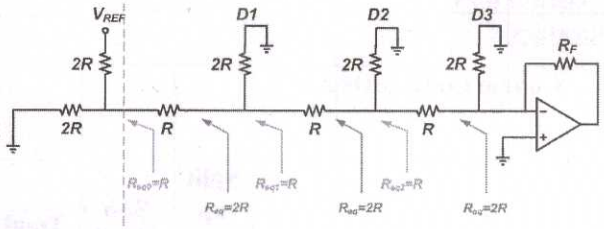


Figure 5

Applying the Thevenin theorem, we can model the circuitry to the left of the dashed line as shown in Fi

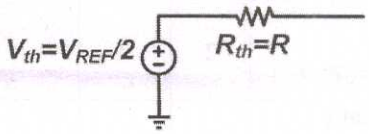


Figure 6

The Thevenin equivalent voltage is VREF divided by two, and the Thevenin equivalent resistance is equ

Now, we use this equivalent circuit and obtain the circuit in Figure 7.

b)

Flash Analog to Digital Converter

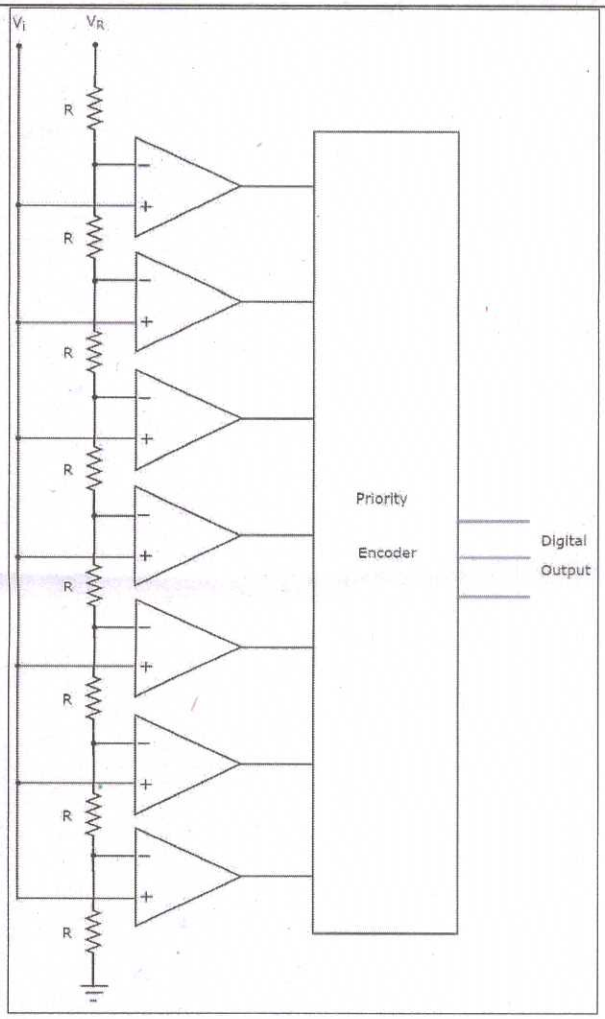
Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analo to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth, but they consu power and much bigger in size than other ADC architectures. A Flash converter requires a huge number comparators compared to other ADCs, especially as the resolution increases. A Flash converter requires comparators for an n-bit conversion.

3

7

15

4


V_i
V_R
R
R
R
R
R
R
R
Priority
Encoder
Digital
Output