

TED (15) -3131  
(Revision -2015)

**A20-00897**

Reg.No.....  
Signature.....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/  
COMMERCIAL PRACTICE – APRIL -2020.

**COMPUTER ARCHITECTURE**

(Maximum Marks :75)

[Time : 2.15 hours]

**PART-A**

Marks

**I.** Answer **any three** questions in one or two sentences. Each question carries 2 marks.

1. What is the significance of Accumulator.
2. Write about ROM.
3. Write any two example for optical memory.
4. Describe the process of instruction fetch.
5. What is the use of MBR.

(3x2=6)

**PART - B**

**II** Answer **any four** of the following questions . Each question carries 6 marks.

1. Describe about memory hierarchy.
2. Explain components of a magnetic disk drive.
3. Write short note on external devices.
4. List different flags in status registers.
5. Draw the state diagram for instruction cycle.
6. List and briefly explain the different type of parallel processor system.
7. Describe micro operation.

[4x6 =24]

**PART - C**

(Answer **any of the three units** from the following. Each full question carries 15 marks)

**UNIT I**

**III** (a) With figure explain Von Neumann machine architecture. (8)

(b) Explain the different bus used in the CPU. (7)

**OR**

**IV** (a) Explain cache memory and state the need of cache memory. (7)

(b) Explain the working of DRAM. (8)

**UNIT- II**

**V** (a) Distinguish between RAID 0, RAID 1, RAID 2. (8)

(b) Explain Digital Versatile Disk. (7)

**OR**

**VI** (a) List and explain I/O module function. (8)

(b) Describe DMA operation. (7)

**UNIT- III**

**VII** (a) Explain internal structure of the CPU with diagram. (8)

(b) List and explain the functions of control registers. (7)

**OR**

**VIII** (a) Draw and explain the data flow diagram for fetch cycle. (8)

(b) Explain instruction pipeline operation. (7)

**UNIT – IV**

**IX** (a) Explain the block diagram of hardwired implementation of control unit. (8)

(b) Briefly explain Indirect cycle. (7)

**OR**

**X** (a) Describe microprogrammed control unit. (8)

(b) Explain multiple processor organization. (7)

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