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(Revision - 2015)

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Reg. No……
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2020

COMPUTER ARCHITECTURE

[Maximum Marks: 75] [Time: 2.15 Hours]

PART-A

(Answer ***any three*** questions in one or two sentences. Each question carries 2 marks)

I. 1. Define cache memory.

2. Mention the involvement of processor in DMA transfer.

3. What is the purpose of MBR?

4. Define fetch overlap.

5. List four registers involved in fetch operation. (3 x 2 = 6)

PART-B

(Answer ***any four*** of the following questions. Each question carries ***6*** marks)

II 1. Explain memory hierarchy with neat diagram.

2. Compare SRAM and DRAM.

3. Draw external device block diagram and explain each part.

4. Explain multiple platter disk drive with neat diagram.

5. Write short note on Control Registers.

6. Explain Micro operation with neat diagram.

7. Draw hardwired implementation of control unit explain operation of each block. (4 x 6 = 24)

PART-C

(Answer ***any of the three units*** from the following. Each full question carries 15 marks)

UNIT – I

III (a) List and explain any four characteristics of Memory system. (8)

(b) Explain the structure of Von Neumann machine with neat sketch. (7)

OR

IV (a) Explain buses used to connect important components of computer with neat diagram. (7)

(b) List and explain the elements of cache design. (8)

UNIT – II

V (a) With neat diagram explain the read write mechanism of magnetic disk. (6)

(b) Explain RAID 0, RAID 1, RAID 2 with neat diagram. (9)

OR

VI (a) Explain interrupt driven I/O. (7)

(b) Briefly explain I/O module function. (8)

UNIT- III

VII (a) Explain the user visible registers. (8)

(b) Briefly explain the structure and function of processor. (7)

OR

VIII (a) Explain data flow in indirect cycle with neat diagram. (8)

(b) What is instruction pipelining? Explain two stage instruction pipelining. (7)

UNIT - IV

IX (a) Explain the micro operation involved in fetch and indirect cycle. (8)

(b) Draw the block diagram of a control unit and explain its inputs and outputs. (7)

OR

X (a) What is parallel processing? Explain Flynns classification. (7)

(b) Explain the micro programmed implementation of control unit. (8)
