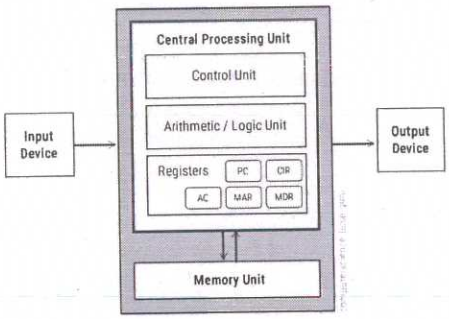
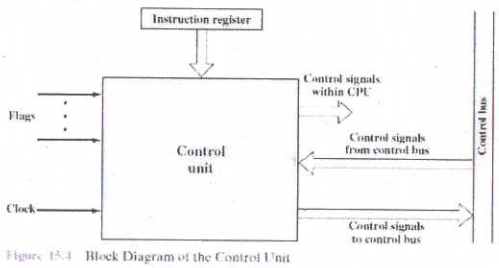
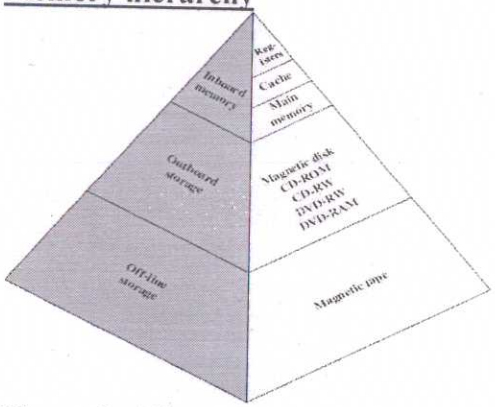
	COMPUTER ARCHITECTURE (3131)- Rev 2015 ANSWER KEY		
Q no	**Scoring Indicators**	**Split score**	**Total score**
I	**PART A**		
1	A bus is a communication pathway connecting two or more devices.	2 marks	2
2	Seektime: time taken to position the read write head at the desired track	2 marks	2
3	Instruction Cycle stages: Fetch, Execute, Interrupt, Indirect	4 stages, 2 marks	2
4	Microprogram: sequence of micro instructions	2 marks	2
5	Parallel processing: is a method of running two or more processors (CPUs) to handle separate parts of an overall task. Helps to reduce the amount of time to run a program.	2 marks	2
II	**PART B**		
1	Von- Neumann machine with neat diagram  • **Von Neumann machine,** the basic design of the modern computer referred to as the IAS (Institute for Advanced Studies) computer. • It is the prototype(model) of all subsequent general-purpose computers and execution occurs in a sequential fashion • The general structure of the IAS computer consists of 1. A **Main memory**, which stores both data and instructions. 2. An **Arithmetic and Logic Unit (ALU)** capable of operating on binary data. 3. A **Control unit**, which interprets the instructions in memory and causes them to be executed.	Fig 3marks, expln 3marks	6

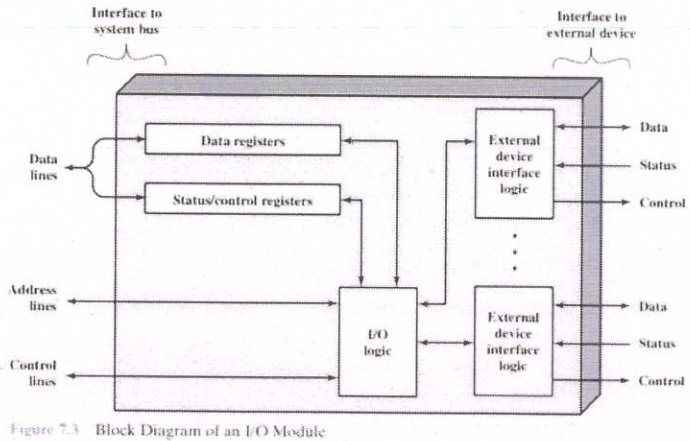
	• **Input and output (I/O)**		
2	Compare static RAM and dynamic RAM • Both static and dynamic RAMs are volatile; • A dynamic memory cell is simpler and smaller than a static memory cell. • Thus, a DRAM is more dense (smaller cells more cells per unit area) and less expensive than a corresponding SRAM. • DRAM requires the supporting refresh circuitry. • SRAMs are generally somewhat faster than DRAMs. • Because of these relative characteristics, SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory.	Any 4points, 6marks	6
3	Table 6.1 Physical Characteristics of Disk Systems **Head Motion** Fixed head (one per track) Movable head (one per surface) **Disk Portability** Nonremovable disk Removable disk **Sides** Single sided Double sided **Platters** Single platter Multiple platter **Head Mechanism** Contact (floppy) Fixed gap Aerodynamic gap (Winchester)	Any 3 points, 2marks each	6
4	**Direct Memory Access** • When large volumes of data are to be moved, a more efficient technique is required: direct memory access (DMA). • Direct Memory Access (DMA) allows devices to transfer data without using the participation of processor. • DMA involves an additional module on the system bus. The DMA module is capable of taking over control of the system from the processor. • It needs to do this to transfer data to and from memory over the system bus. • For this purpose, the DMA module must use the bus only when the processor does not need it, or it must force the processor to suspend operation temporarily.	6marks	6
5	**Instruction pipelining:** fetch the next instruction while the present one is being executed. ➢ Technique used to improve performance.	Expln 6marks	6

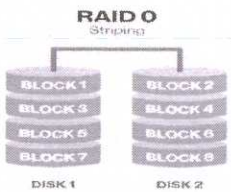
	Consider the instruction sequence as: • instruction fetch, • decode instruction, • fetch data, • execute instruction, • store result, • check for interrupt Consider it as an "assembly line" of operations. Then we can begin the next instruction assembly line sequence before the last has finished. Actually we can fetch the next instruction while the present one is being decoded. *This is pipelining.*		
6	**Control and status registers** The different registers under this category are: 1. **Program Counter (PC)** :contains address of next instruction .The processor updates the PC after each instruction fetch so that the PC always points to the next instruction to be executed. 2. **Instruction register (IR):** contains the recently fetched instruction.. The fetched instruction is loaded into an IR, where the opcode and operandsare interpreted. 3. **Memory Address Register(MAR):** contains memory address of instruction or data. The MAR connects directly to the address bus. 4. **Memory Buffer Register (MBR)** : contains a word of data read or written to memory.MBR connects directly to the data bus. 5. **Program Status Word (PSW)** : Contains status information.The PSW typically contains condition codes plus other status information.	Any 4, 6 marks	6
7	**Control unit**  Figure 15.4 Block Diagram of the Control Unit • The control unit directs operations within the processor. The execution of a program consists of	Expln 3marks, fig 3marks	6

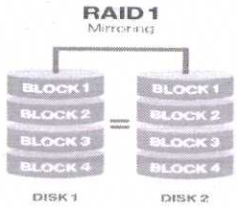
	operations involving the processor elements ALU, memory, and I/O modules. Control unit provides control and timing signals to control and coordinate the operations. • These operations consist of a sequence of micro-operations. The control unit performs two basic tasks: 1. **Sequencing**: The control unit causes the processor to step through a series of micro-operations in the proper sequence, based on the program being executed. 2. **Execution**: The control unit causes each micro-operation to be performed.		
	PART C		
III a	**Memory hierarchy**  **Hierarchy List** 1. Registers: The fastest, smallest, and most expensive type of memory consists of the registers internal to the processor. registers improve performance. 2. L1 Cache: 3. L2 Cache – Main memory is usually extended with a higher-speed, smaller cache. The cache is not visible to the programmer or to the processor. 4. Main memory : Main memory is the principal internal memory system of the computer. Each location in main memory has a unique address. – These above three forms of memory are volatile and employ semiconductor technology. – The semiconductor memory comes in a variety	Fig 3marks Expln 5marks	8

	of types, which differ in speed and cost. 5. Disk 6. Optical 7. Tape – Data are stored more permanently on external mass storage devices, of which the most common are hard disk and removable media, such as removable magnetic disk, tape, and optical storage.		
b	**Advanced Dram Types** 1. **Synchronous DRAM** ✓ One of the most widely used forms of DRAM is the synchronous DRAM (SDRAM). ✓ With synchronous access, the DRAM moves data in and out under control of the system clock. ✓ SDRAM exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states. ✓ The SDRAM performs best when it is transferring large blocks of data serially, such as for applications like word processing, spreadsheets, and multimedia. 2. **Rambus DRAM** ✓ RDRAM, developed by Rambus, has been adopted by Intel for its Pentium and Itanium processors. ✓ RDRAM chips are vertical packages, with all pins on one side. ✓ The chip exchanges data with the processor over 28 wires no more than 12 centimeters long. 3. **DDR SDRAM** ✓ **SDRAM is limited by** the fact that it can only send data to the processor once per bus clock cycle. ✓ A new version of SDRAM, referred to as double-data-rate SDRAM can send data **twice per clock cycle**, once on the **rising edge of the clock pulse**	Listing 1 mark Expln 1 ½ marks each	7

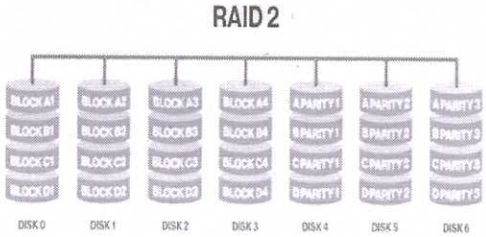
	and once on the falling edge. ✓ **There have been two generations of improvement to the DDR technology.** ✓ Theoretically, a DDR module can transfer data at a clock rate in the range of 200 to 600 MHz; a DDR2 module transfers at a clock rate of 400 to 1066 MHz; and a DDR3 module transfers at a clock rate of 800 to 1600 MHz. 4. **Cache DRAM** ✓ Cache DRAM (CDRAM), developed by Mitsubishi, integrates a small SRAM cache (16 Kb) onto a generic DRAM chip		
IV a	**Elements of bus design.** 1. Bus types 2. Method of arbitration 3. Timing 4. Bus width 5. Data transfer type ➢ **Bus types** • Bus lines can be separated into two generic types: 1. Dedicated : A dedicated bus line is permanently assigned either to one function or to a physical subset of computer components. 2. Multiplexed.:The method of using the same lines for multiple purposes is known as time multiplexing. ➢ **Method of arbitration** 1. Centralized scheme: In a centralized scheme, a single hardware device, referred to as a bus controller or arbiter, is responsible for allocating time on the bus. 2. Distributed scheme:In a distributed scheme, there is no central controller. Rather, each module contains access control logic and the modules act together to share the bus. ➢ **Timing** • Timing refers to the way in which events are coordinated on the bus. • Buses use either synchronous timing or asynchronous timing.	Correct listing and expln: 3marks each	9

	Synchronous timing: the occurrence of events on the bus is determined by a clock. Asynchronous timing: the occurrence of one event on a bus follows and depends on the occurrence of a previous event. ➢ **bus width: the no. of lines in the bus.** ➢ **data transfer type** • A bus supports various data transfer types. All buses support both write (master to slave) and read (slave to master) transfers.		
b	**Characteristics of computer memory system.** Table 4.1 Key Characteristics of Computer Memory Systems **Location** Internal (e.g. processor registers, main memory, cache) External (e.g. optical disks, magnetic disks, tapes) **Capacity** Number of words Number of bytes **Unit of Transfer** Word Block **Access Method** Sequential Direct Random Associative **Performance** Access time Cycle time Transfer rate **Physical Type** Semiconductor Magnetic Optical Magneto-optical **Physical Characteristics** Volatile/nonvolatile Erasable/nonerasable **Organization** Memory modules	Listing 2 marks, expln of any 5, 1 mark each	7
V a	I/O module structure  Figure 7.3 Block Diagram of an I/O Module functions 1. Control and timing 2. Processor communication 3. Device communication	Fig 3 marks Listing and expln 5 marks	8

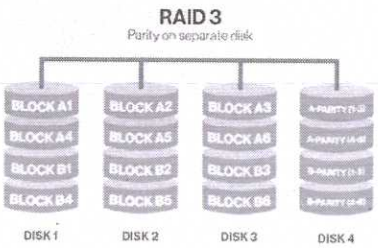
	4. Data buffering 5. Error detection		
b	**Interrupt driven I/O** • This technique is used to **overcome the limitation of programmed I/O.** • In interrupt driven I/O, instead of making the processor to verify the status of I/O module. **It is the responsibility of I/O module to intimate the processor by interrupt Signal.** • CPU responds to interrupt signals and stores the return address from the **program counter (PC)** into the memory stack and then the control branches to a **interrupt service routine (ISR)**. • ISR processes the required I/O Transfer after completion of executing interrupt routine CPU returns to previous program and continue what it was doing before.	Expln 7 marks	7
VI a	**Different RAID Levels** • RAID is arrays of disks that operate independently and in parallel. **RAID Level 0**  ➢ For RAID 0, the user and system data are distributed across all of the disks in the array. The data are *striped* across the available disks, but no redundancy of data. It offers the **best performance**, **but no fault tolerance**. Data are distributed across all of the disks in the array.	5 levels, 15 marks	15



- Also known as **disk mirroring**, this configuration consists of at **least two drives** that duplicate the storage of data. T**here is no striping.** Recovery from a failure is simple

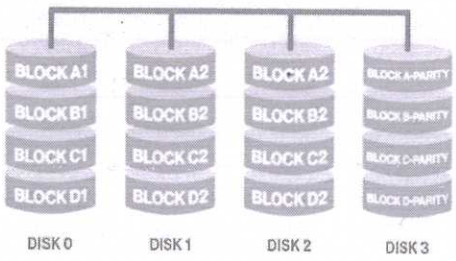


- RAID2 need two groups of disks. One group of disks are used to write the data, another group is used to write the error correction Codes.
- This uses Hamming error correction code (ECC), and stores this information in the redundancy disks.
- **RAID levels 2 and 3** make use of a **parallel access technique.**



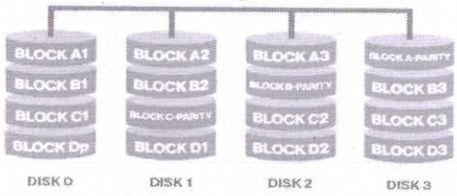
- RAID 3 is organized in a similar fashion to RAID2.The difference is that RAID 3 requires only a single redundant disk, no matter how large the disk array.
- RAID 3 employs parallel access, with data distributed in small strips. Instead of an error-correcting code, a simple parity bit is computed for the set of individual bits in the same position on all of the data disks.

RAID 4



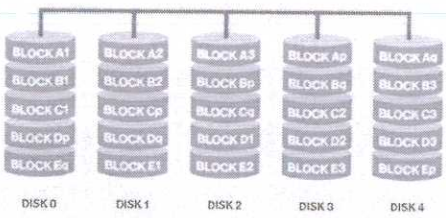
- RAID levels 4 through 6 make use of an independent access technique.
- In an independent access array, each member disk operates independently so that separate I/O requests can be satisfied in parallel.

RAID 5



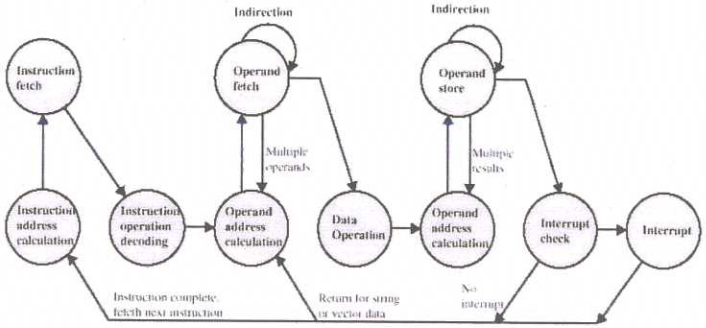
- RAID 5 consists of **block-level striping with distributed parity**
- RAID 5 is organized in a similar fashion to RAID 4.The difference is that RAID 5 distributes the parity strips across all disks.

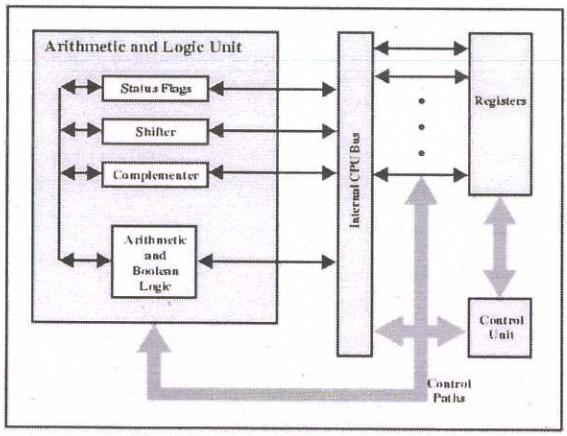
RAID 6

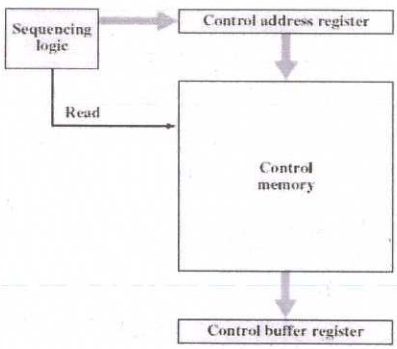


- Two different parity calculations are carried out and stored in separate blocks on different disks.
- RAID 6 is also more expensive because of the two extra disks required for parity.

VII a	• There are situations, called hazards, that prevent the next instruction in the instruction stream from executing during its designated cycle
	• There are three classes of hazards
	  • Structural hazard
	  • Data hazard
	  • Branch hazard
	• **Structural hazard**
	  • Resource conflicts when the hardware cannot support all possible combination of instructions simultaneously
	• **Data hazard**
	  • An instruction depends on the results of a previous instruction
	• **Branch hazard**
	  • Instructions that change the PC
		Defn and listing 2 marks, Expln 2 marks each	8

b	instruction cycle state diagram  An instruction cycle includes the following stages: • **Fetch**: Read the next instruction from memory into the processor. • **Execute**: Interpret the opcode and perform the indicated operation. • **Interrupt**: If interrupts are enabled and an interrupt has occurred, save the current process state and service the interrupt. • **Indirect Cycle :** o If the execution of an instruction involve one or more operands in memory, each of which has to be fetched from memory. So additional memory accesses are required if indirect addressing is specified.	Fig 4 marks, Expln 3 marks	7
VII I a	**User visible registers** • These are registers which can be referenced by machine language that processor executes. • They are categorized into the following **1. General purpose registers**	Defn and listing 2 marks Expln of each 1 ½ marks	8

	They can be used to different functions by the programmer - to store the operands or address of operands etc **2. Data registers** Used only to hold data and cannot be used to store an operand address. **3. Address registers** Used to hold addresses. This include Segment Registers, Index registers, Stack pointer **4. Condition codes** • Condition codes are a collection of individual bits set by the hardware according to the result of various arithmetic or logic operations. • The different conditions are carry out of an addition or a positive, negative or zero result , an overflow condition etc. • These condition codes can be collected into one or more registers. Usually they form a part of control registers and programmer cannot alter them.		
b	internal structure of CPU with a neat diagram  – The **ALU** does the actual computation or processing of data. – ALU operates only on data in the internal processor memory. So an **Internal Processor Bus** is needed to transfer data between various registers and ALU.	Fig 4marks Expln 3 marks	7

	– The **control unit** controls the movement of data and instructions into and out of the processor and controls the operation of the ALU. – A set of storage locations, called **registers.**		
IX a	**Micro programmed control unit** Block diagram includes: • Control memory: – Memory contains control words. ie the set of microinstructions is stored in the *control memory.* • control address register contains the address of the next microinstruction to be read. • When a microinstruction is read from the control memory, it is transferred to a *control buffer register.* • sequencing unit that loads the control address register and issues a read command.  Figure 16.3 Control Unit Microarchitecture	Fig 4 marks Expln 4marks	8
b	**Fetch cycle micro operations** The fetch cycle actually consists of three steps and four microoperations. 1. At the beginning of the fetch cycle, the address of the next instruction to be executed is in the program counter (PC); o The first step is to move that address to the memory address register (MAR).	Fetch cycle steps 3 marks, micro operations 4 marks	7

	2. The second step is to bring in the instruction. o The desired address in the MAR is placed on the address bus, the control unit issues a READ command on the control bus, and the result appears on the data bus and is copied into the memory buffer register (MBR). o We also need to increment the PC by the instruction length to get ready for the next instruction. 3. The third step is to move the contents of the MBR to the instruction register (IR). • Each micro-operation involves the movement of data into or out of a register. t1: MAR ← (PC) t2: MBR ←Memory PC ← (PC) + I t3: IR ← (MBR) where I is the instruction length.		
X a	• Flynn proposed the following categories of computer systems: 1. Single instruction, single data (SISD) stream 2. Single instruction, multiple data (SIMD) stream 3. Multiple instruction, single data (MISD) stream 4. Multiple instruction, multiple data (MIMD) stream	Listing and expln with all diagrams, 15 marks	15

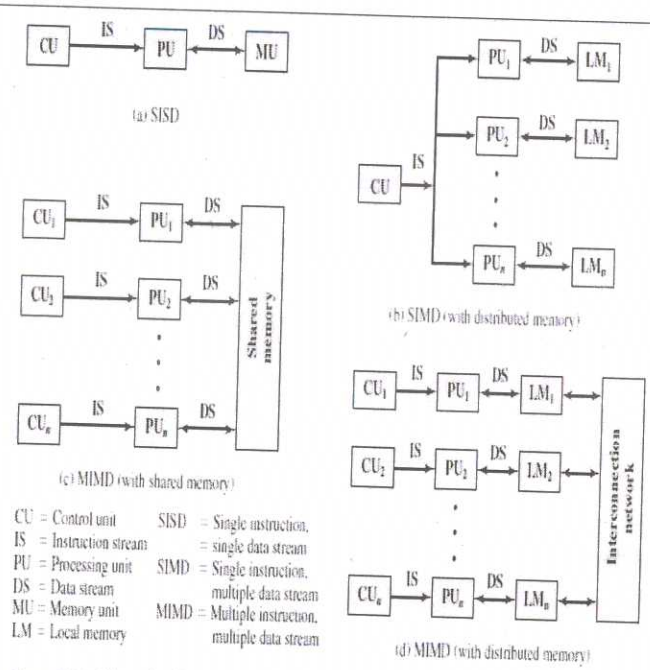


Figure 17.2 Alternative Computer Organizations

SISD

- SISD machines executes a single instruction on individual data values using a single processor.
- Based on traditional Von Neumann uniprocessor architecture, instructions are executed sequentially or serially, one step after the next.

SIMD

- An SIMD machine executes a single instruction on multiple data values simultaneously using many processors.
- SIMD architectures include vector and array processors.
- Each processing element has an associated data memory, so that each instruction is executed on a different set of data by the different processors.

MISD

- Single data is transmitted to a set of processors, each of which executes a different instruction sequence.

This structure is not commercially implemented

MIMD

- MIMD machines are usually referred to as **multiprocessors** or **multicomputers.**
- It may execute multiple instructions simultaneously, contrary to SIMD machines.
- Each processor must include its own control unit that will assign to the processors parts of a task or a separate task.
- It has two subclasses: Shared memory and distributed memory.