TED (15) – 3133

(REVISION — 2015)

Reg. No..

Signature ....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE — APRIL, 2018

DIGITAL COMPUTER PRINCIPLES

[*Time* : 3 hours

(Maximum marks : 100)

PART — A

(Maximum marks : 10)

Marks

I   Answer *all* questions in one or two sentences. Each question carries 2 marks.

1. Define binary codes.

2. Define minterm.

3. What is the function of an encoder ?

4. Define a flip-flop.

5. What is mean by resolution in DAC ?   (5×2 = 10)

PART — B

(Maximum marks : 30)

II   Answer any *five* of the following questions. Each question carries 6 marks.

1. Explain the behavior of universal gates with logic diagram and truth table.

2. Reduce the expression $F = A + B[AC+(B+C')D]$

3. Convert $(10110)_2$ to gray code and $(11011)_{gray}$ to binary.

4. Design a half adder with truth table, expressions and logic diagram.

5. Differentiate synchronous and asynchronous sequential circuits.

6. Explain the working of a T-flipflop with logic diagram and truth table.

7. Describe the working of R-2R DAC.   (5×6 = 30)

[151]

[P.T.O.

Marks

PART — C

(Maximum marks : 60)

(Answer *one* full question from each unit. Each full question carries 15 marks.)

UNIT — I

III (a) Convert the following :

     (i) 163.875_{10} to binary

     (ii) $4F7.A8_{16}$ to octal

     (iii) 2056_8 to decimal   9

  (b) Construct an EX-OR gate using NAND gate.   6

OR

IV (a) Explain about alpha numeric codes with examples.   9

  (b) Reduce the expression $F = (A + (BC)')' (AB' + ABC)$ using Boolean algebra.   6

UNIT — II

V (a) Design a full adder with minimum number of gates.   9

  (b) Reduce the expression $F(x,y,z) = \Sigma m(0, 1, 2, 3, 6)$ 6

OR

VI (a) Explain the working of a 4×1 Multiplexer with diagram.   8

  (b) Explain the working of a magnitude comparator.   7

UNIT — III

VII (a) Explain the working of JK Master slave flip flop with logic diagram.   9

  (b) Explain the working of 3 bit Johnson counter.   6

OR

VIII (a) Explain the working of a parallel in serial out shift register.   9

  (b) Explain the working of 4 bit ring counter.   6

UNIT — IV

IX (a) Explain the working of counter ramp type ADC with diagram.   9

  (b) Write notes on error correction codes.   6

OR

X (a) Draw a logic diagram to implement the Boolean function.

     $F1 = (AB + AC + BC)'$

     $F2 = AB + AC + A'B'C'$ in PLA   9

  (b) Write notes on the following DAC parameters.

     (i) Monotonicity   (ii) Setting time.   6