Scheme of Evaluation

Scoring Indicators

Code: 3133 **Digital Computer Principles** **Version: A**

Qn: No	Scoring Indicators	Split score	Sub total	Total score
I 1	The number of unique symbols used in that system	2	2	2
I 2	2^n	2	2	2
I 3	Serial in serial out, Serial in Parallel out, Parallel in Serial out, Parallel in parallel out	½ *4	2	2
I 4	Smallest change that can occur in an analog output as a result of a change in the digital input.	2	2	2
I 5	5	2	2	2
II 1	A BCD code is one ,in which the digits of a decimal number are encoded – one at a time –into groups of four binary digits. These codes combine the features of decimal and binary numbers. BCD equivalent of 653 is : 0110 0101 0011 XS-3 code is : 1001 1000 0110	Defn- 2 BCD- 2 XS-3- 2	2+2+2	6
II 2	Proof: LHS = AB + A'C + BC AB + A'C + BC (A+A') AB + A'C + BCA +BCA' AB (1+C) + A'C (1 +B) AB (1) + A'C (1) AB + A'C =RHS	6 marks	6	6
II 3	Minterm: Each one of the product terms in canonical SOP form is called minterm. A'+B'= A'(B+B') + B'(A+A') = A'B +A'B' +B'A + B'A' = A'B + A'B' + AB' + A'B' = A'B+A'B'+AB' = 01+00+10 = m1+m0+m2 = ∑m(0,1,2)	Defn : 2marks expansion 4 marks	2+4	6
II 4	A2=D4+D5+D6+D7 A1=D2+D3+D6+D7 A0=D1+D3+D5+D7	Truth table 3marks Logical expn: 3 marks	3+3	6

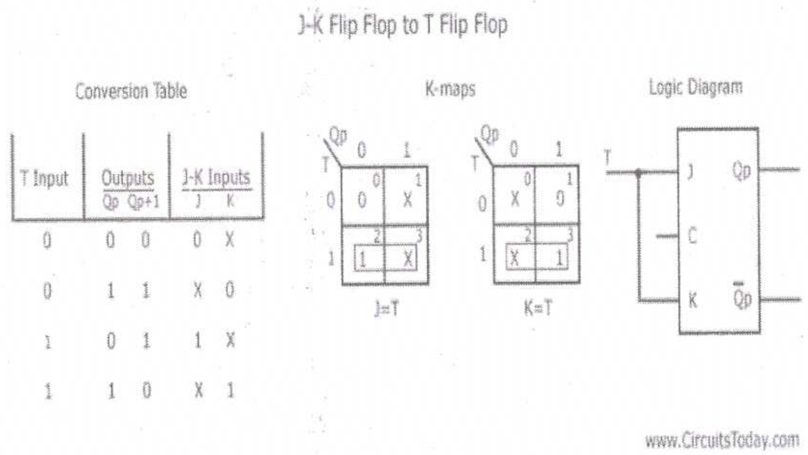
Scheme of Evaluation

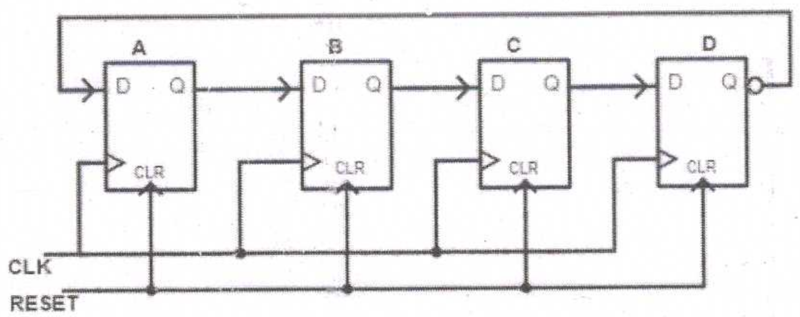
Scoring Indicators

Code: 3133 **Digital Computer Principles** **Version: A**

<table>
<tr><td></td><td>

Octal to binary encoder				
Octal input		Binary output		
		A_2	A_1	A_0
D_0	0	0	0	0
D_1	1	0	0	1
D_2	2	0	1	0
D_3	3	0	1	1
D_4	4	1	0	0
D_5	5	1	0	1
D_6	6	1	1	0
D_7	7	1	1	1

</td><td></td><td></td><td></td></tr>
<tr><td>II 5</td><td>


</td><td>6</td><td>6</td><td>6</td></tr>
<tr><td>II 6</td><td>


</td><td>Circuit design:4 marks

Truth table :2 marks</td><td>4+2</td><td>6</td></tr>
</table>

Scheme of Evaluation

Scoring Indicators

Code: 3133 **Digital Computer Principles** **Version: A**

Q_0	Q_1	Q_2	Q_3
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

II 7

BASIS FOR COMPARISON	PLA	PAL
Stands for	Programmable Logic Array	Programmable Array Logic
Construction	Programmable array of AND and OR gates.	Programmable array of AND gates and fixed array of OR gates.
Availability	Less prolific	More readily available
Flexibility	Provides more programming flexibility.	Offers less flexibility, but more likely used.
Cost	Expensive	Intermediate cost
Number of functions	Large number of functions can be implemented.	Provides the limited number of functions.
Speed	Slow	High

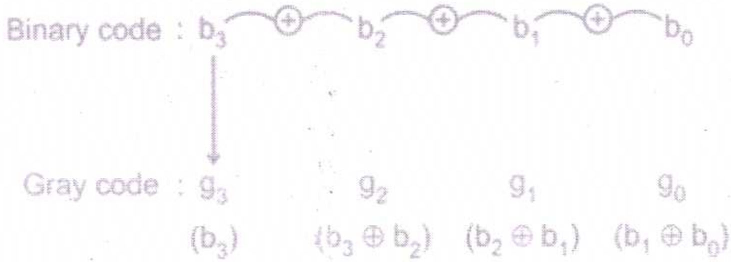
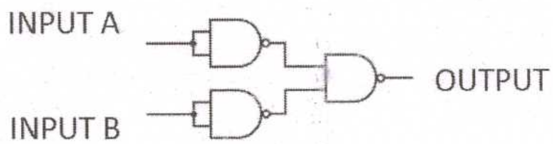
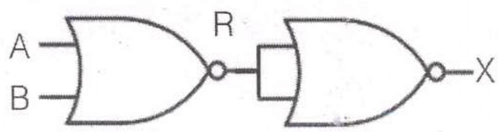
Any 3 points

3x 2marks | 3*2 | 6

Scheme of Evaluation

Scoring Indicators

Code: 3133 **Digital Computer Principles** **Version: A**

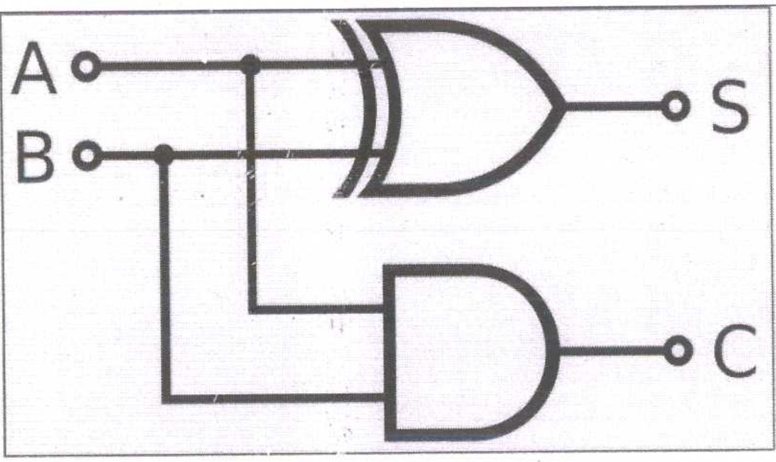
III a	Decimal :1271.65625 Octal : 2367.52 Binary : 10011110111,10101	3x 3marks	9	15
III b	1. Record the MSB of the binary as the MSB of the Gray code 2. Add the MSB of the binary to the next bit in binary, recording the sum and ignoring the carry,if any.this sum is the next bit of the gray code 3. Add the 2^{nd} bit of the binary to the third bit of the binary, the third bit to the fourth bit, and so on. 4. Record the successive sums as the successive bits of the gray code until all the bits of the binary number are exhausted. 	Procedure: 4marks, example : 2marks	6	
IVa	OR gate from NAND gates  **OR GATE USING NOR GATE** 	2x 4 marks	8	15
IV b	Hexadecimal : 79.D Octal : 171.64	2x3 ½ marks	7	

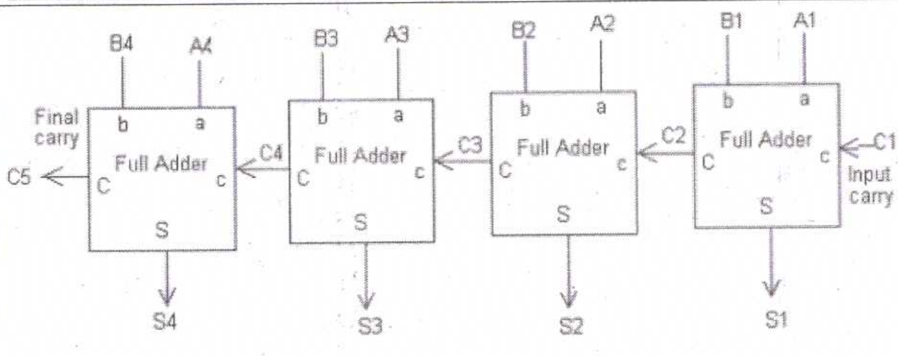
Scheme of Evaluation

Scoring Indicators

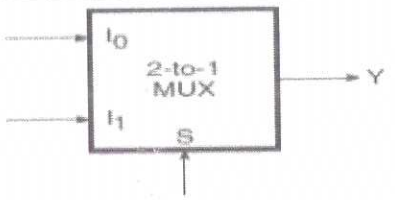
Code: 3133 **Digital Computer Principles** **Version: A**

<table>
<tr>
<td>V a</td>
<td>K map is a chart or a graph composed of an arrangement of adjacent cells, each representing a particular combination of variables in a sum or product term.

Minimised form : A’B’C + BD + AB + AD</td>
<td>Defn :2 marks Minimization 6 marks</td>
<td>8</td>
<td rowspan="2">15</td>
</tr>
<tr>
<td>V b</td>
<td>

INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1
</td>
<td>Logic circuit 3 marks, Truthtable 2marks, Explanation:2marks</td>
<td>7</td>
</tr>
<tr>
<td>VI a</td>
<td>
</td>
<td>Diagram : 5 marks

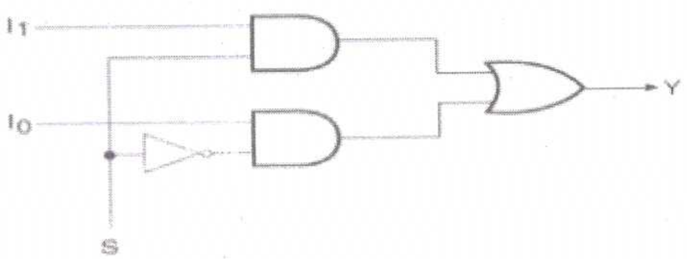
Explanation 3 marks</td>
<td>8</td>
<td>15</td>
</tr>
</table>

<table>
<tr>
<td>VI
b</td>
<td>


(a)

<table>
<tr><th>S</th><th>Y</th></tr>
<tr><td>0</td><td>I0</td></tr>
<tr><td>1</td><td>I1</td></tr>
</table>

(b)

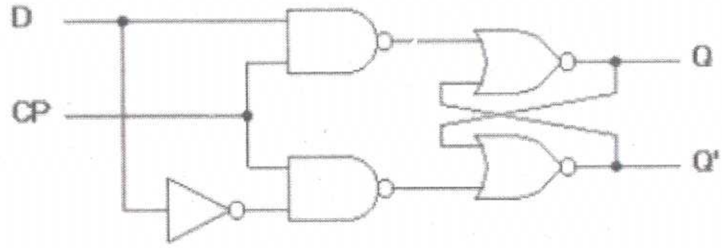


</td>
<td>Circuit diagram:4 marks, explanation :3 marks</td>
<td>7</td>
<td></td>
</tr>
</table>

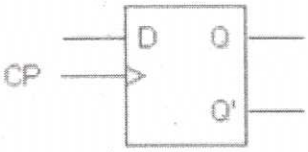
Scheme of Evaluation

Scoring Indicators

Code: 3133 **Digital Computer Principles** **Version: A**

<table>
<tr>
<td>VII
a</td>
<td>


(a) Logic diagram with NAND gates

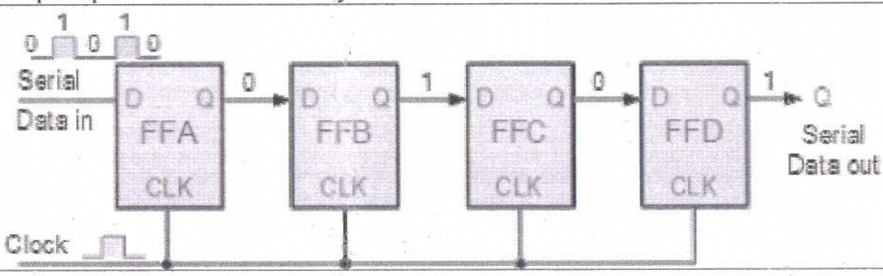


(b) Graphical symbol

<table>
<tr><th>Q D</th><th>Q(t+1)</th></tr>
<tr><td>0 0</td><td>0</td></tr>
<tr><td>0 1</td><td>1</td></tr>
<tr><td>1 0</td><td>0</td></tr>
<tr><td>1 1</td><td>1</td></tr>
</table>

(c) Transition table

Clocked D flip-flop

Flip flop is the basic memory element. It can store a 0 or 1.
</td>
<td>Logic ckt :3marks,Truth table :3 marks, explanation: 2 marks</td>
<td>8</td>
<td rowspan="2">15</td>
</tr>
<tr>
<td>VII
b</td>
<td>


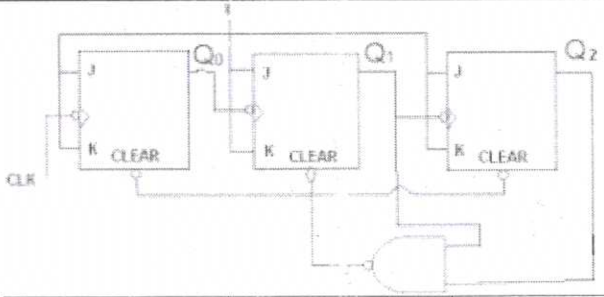
</td>
<td>Diagram : 4 marks, explanation : 3marks</td>
<td>7</td>
</tr>
<tr>
<td>VIII
a</td>
<td>Counter is a set of flipflops whose states change in response to pulses applied at the input to the counter.</td>
<td>Defn. 2 marks</td>
<td>8</td>
<td></td>
</tr>
</table>

Synchronous Counter	Asynchronous Counter
All flip flops are triggered with same clock.	Different clock is applied to different flip flops.
It is faster.	It is lower
Design is complex.	I Design is relatively easy.
Decoding errors not present.	Decoding errors present.
Any required sequence can be designed	Only fixed sequence can be designed.

Differences : 6 marks

(any 3 points)

VIII b



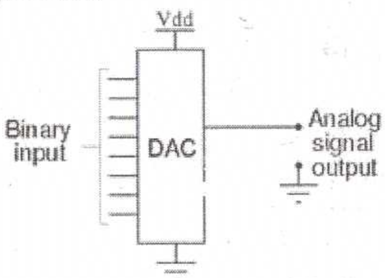
states	Q2	Q1	Q0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	0	0	0

Logic ckt:4 marks
Truth table :3 marks

Marks: 7 — Total: 15

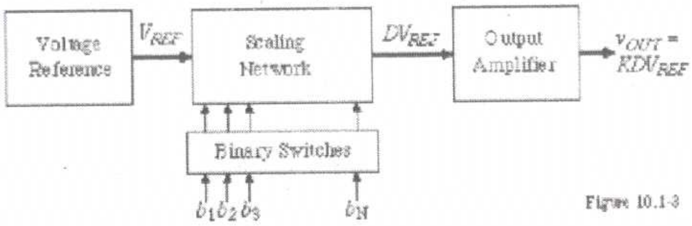
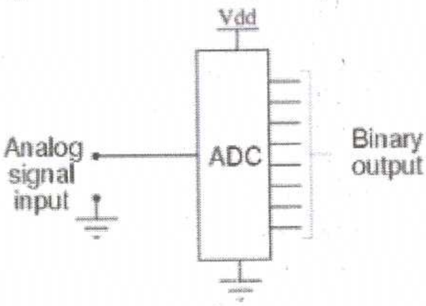
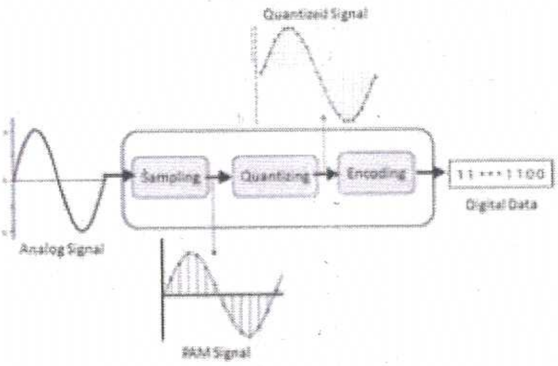
IX a

A digital-to-analog converter (**DAC**) is a device, usually consisting of a single chip, for converting binary or digital code into an analog signal.
A **DAC** device converts a fixed-point binary number, into voltage or pressure



Defn : 2marks
Block diag : 4marks
Explanation : 2 marks

Marks: 8

				
IX b	Accuracy: Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors. Monotonicity: A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristics is essential in control applications. Settling time: It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances.	2+2+3	7	15
X a	an analog-to-digital converter (ADC, A/D, or A-to-D) is a system that converts an analog signal, such as a sound picked up by a microphone or light entering a digital camera, into a digital signal   *Sampling and Holding : In the process of Sample and hold (S/H), the continuous signal will gets sampled and freeze (hold) the value at a steady level for a particular least period of time. It is done to remove*	Defn :2marks, block diagram :4 marks, explanation : 2marks	8	15

	variations in input signal which can alter the conversion process and thereby increases the accuracy. The minimum sampling rate has to be two times the maximum data frequency of the input signal **Quantizing:** It is the process in which the reference signal is partitioned into several discrete quanta and then the input signal is matched with the correct quantum. **Encoding:** Here; for each quantum, a unique digital code will be assigned and after that the input signal is allocated with this digital code.			
X b	**ROM** - Read-Only Memory, is used to store "permanent" copies of data. ROM retains its contents even when the computer is turned off. ROM is referred to as being *nonvolatile* • PROM: – Programmable ROM – User can store programs only once. – User can make micro code program can be made that are needed mostly. – The process of making program in PROM is called 'Burning'. – Example: CD-R • EPROM: – Erasable PROM – Information can be removed by ultra violet rays. – Information can be re-write after removing previous information. – It is cheaper than PROM because it is re-useable. – Example: CD(RW)	Defn : 3 marks, compariso n : 4 marks(any 3 points)	7	