TED (15) 3133

(Revision-2015)

N20-00887

Reg.No.....

Signature.....

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/
MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER-2020

DIGITAL COMPUTER PRINCIPLES

[Maximum marks: 75] (Time: 2.15 Hours)

PART – A

(Answer any ***three*** questions in one or two sentences. Each question carries 2 marks)

I. (1). Define base or radix of a number system.

(2). Write the number of cells or squares in an n-variable K-map.

(3). List basic types of shift registers.

(4). Define resolution of DAC.

(5). Write the number of address inputs in a 32x4 memory. (3 x 2 = 6)

PART – B

(Answer any ***four*** of the following questions. Each question carries 6 marks)

II. (1). Define BCD code. Express the decimal number 653 in BCD and XS-3 code.

(2). Prove that AB + A'C +BC = AB = + A"C

(3). Define minterm. Expand A'+B' to minterms.

(4). Write the truth table and logic expression for octal to binary encoder.

(5). Show how a J-K flip-flop can be concerted to a T flip-flop.

(6). Design a 4 bit Ring counter using D.flip-flop.

(7). Write any three comparison between PAL and PLA. (4 x 6= 24)

PART – C

(Answer ***any of the three units*** from the following. Each question carries 15 marks)

UNIT –I

III. (a). Convert the hexadecimal number 4F7.A8 to Decimal, Octal and Binary. (9)

(b). Explain with an example the procedure for converting a binary code to a Gray code. (6)

OR

IV. (a). Show how an OR gate is implemented by NAND gate and NOR gate. (8)

(b). Convert the binary number 1111001.1101 to Hexadecimal and Octal. (7)

UNIT-II

V. (a). Define k-map. Obtain the minimal SOP expression for $\sum m(2,3,5,7,9,11,12,13,14,15)$ (8)

(b). Draw a logic circuit for half adder and explain its operation. (7)

OR

VI. (a). Draw the block diagram for 4 bit parallel binary adder and explain its operation. (8)

(b). Draw the logic circuit for a 2 input multiplexer and explain its operation. (7)

UNIT-III

VII. (a). Define flipflop. Explain the operation of D-flip flop with truth table and logic diagram. (8)

(b). Explain the operation of a 4-bit Serial –in Serial –out shift register with proper diagram. (7)

OR

VIII. (a). Define counter. Differentiate between synchronous and asynchronous counters. (8)

(b). Design a mode-6 asynchronous counter. (7)

UNIT-IV

IX. (a). Define DAC. Draw the block diagram of a 4-bit DAC and explain the operation. (8)

(b). Define Accuracy, Setting time and Monotonicity of DAC. (7)

OR

X. (a). Define ADC. With logic diagram, explain the operation of an ADC. (8)

(b). Define ROM. Compare PROM and EPROM. (7)