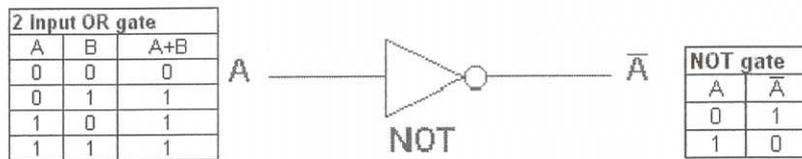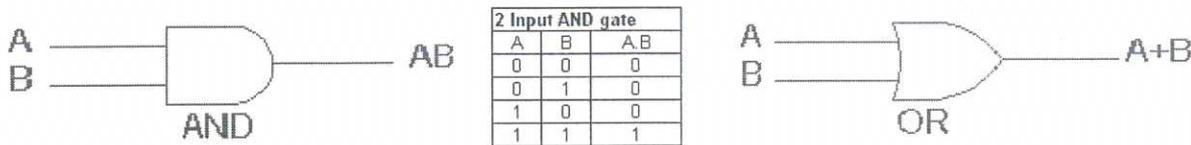I

1 Weighted code-Binary/octal/Hexadecimal,   Un-weighted code -Gray code   1+1=2

2. Parity code, Hamming code   1+1=2

3. SOP,-Sum Of Product/AND-OR Logic ,POS-Product of Sum/OR-AND Logic   1+1=2

4. Synchronous/Asynchronous (parallel/Series)   1+1=2

5. PLA-Programmable Logic Array is a family of PLD. Both AND and OR planes

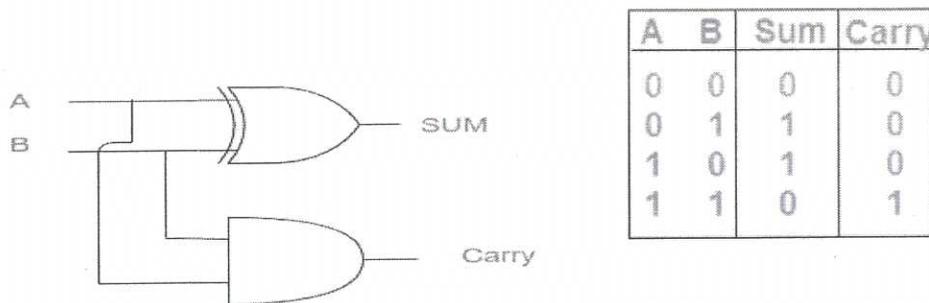are programmable.   1+1=2

II

1. Convert (10110)gray = (11011)binary , 9A5C = (115134)octal,   3*2=6
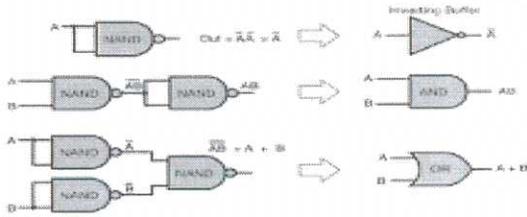
(126)decimal=(1111110)Binary

2

2 Input AND gate

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

2 Input OR gate

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate

A	$\overline{A}$
0	1
1	0

1*6=6

3

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

With basic explanation   2+2+2=6

4

with little explanations   3+2+1=6

5
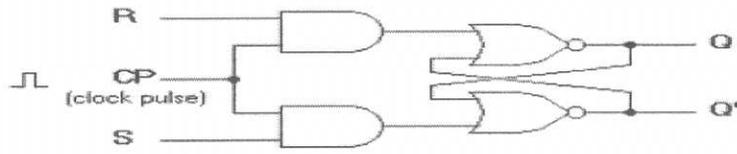
(a) Logic diagram

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

(b) Truth table

Clocked SR flip-flop

Or any suitable truth table with   3+2+1=6

6.
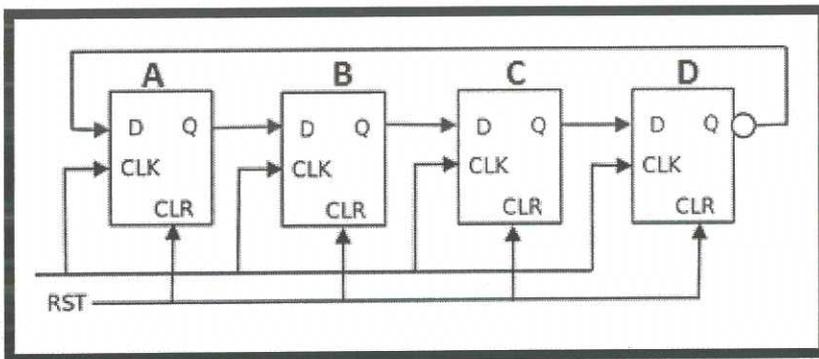
Q_A	Q_B	Q_C	Q_D
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

4+2=6

7.

ROM (Read only memory)	RAM (Random Access memory)
This is found particularly in the bios. This is very small, slow, BUT NON-VOLATILE	Found in computer RAM. This is the main memory of our computer and is very fast, large, BUT VOLATILE

III (a)

$$\overline{A\ B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A}\ \overline{B}$$

Truth Table to prove De Morgan's Theorem:-

A	B	$\overline{A}$	$\overline{B}$	A+B	A·B	$\overline{A+B}$	$\overline{A}·\overline{B}$	$\overline{A·B}$	$\overline{A}+\overline{B}$
0	0	1	1	0	0	1	1	1	1
0	1	1	1	1	0	0	0	1	1
1	0	0	0	1	0	0	0	1	1
1	1	0	0	1	1	0	0	0	0

Theorem 4+Proof4=8

III(b)

   Y=C'   steps 4+Result 3 =7

IV (a)   Explanations for each   2.5*4=10

IV(b)   Substrand 001110   1s compliment 110001   2scompliment 110010

      110101 +

      110010
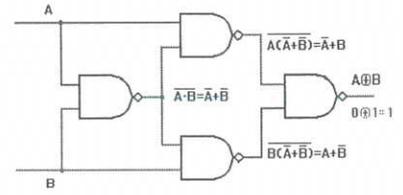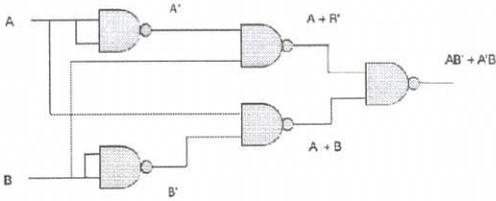   _____

      1100111   Discard carry   result=100111   method-3+Result-2=5

V(a)

0	1	0	X
0	1	0	1
0	1	0	1
0	X	0	1

            Y=C'D+CD'   mapping-5+result-5=10

V(b)

Any one diagram or suitable- 5

VI(a)
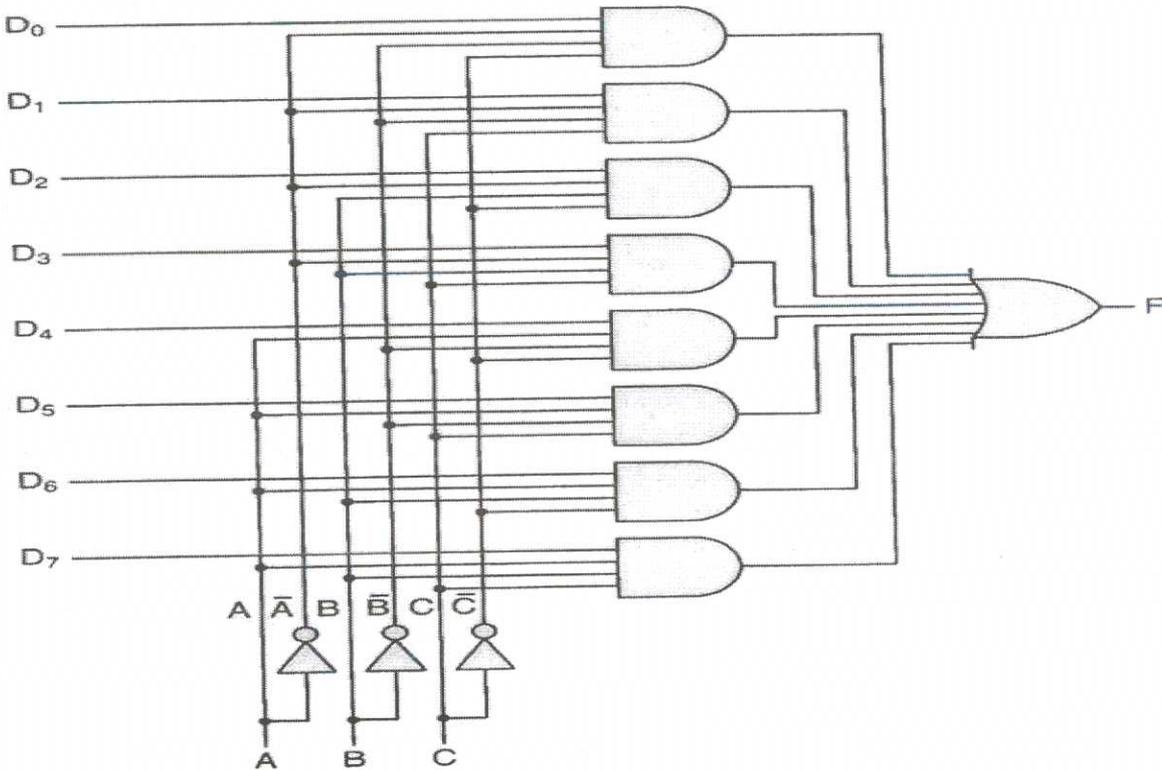
A	B	C	Y
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Logic diagram -6 Truth table 2=8

VI(b)

(a)
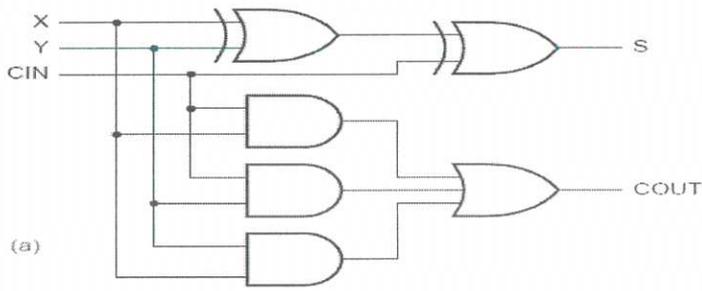
X	Y	CIN	S-sum	COUT-Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic diagram 4+Truth table 3=7

VII(a)
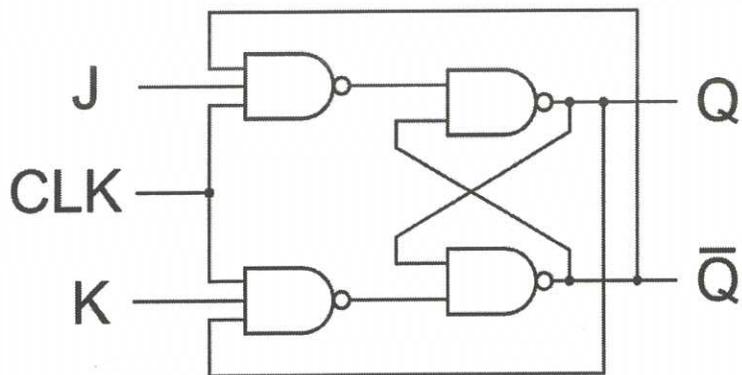
Truth Table

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

Logic diagram 4+Truth table 2+Explanations 2=8

VII(b)

(a)
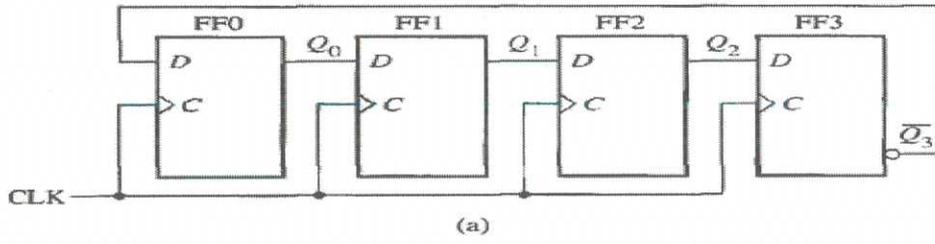
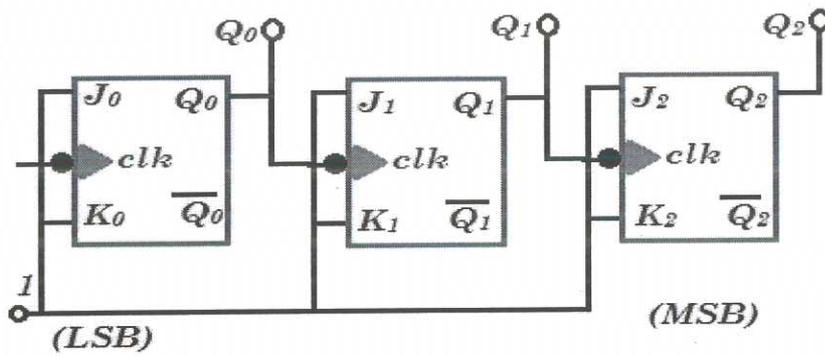| Clock	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

(b)

Diagram 4+Table 3=7

VIII(a)

☐ Serial In Serial Out shift register(SISO)
☐ Serial In parallel Out shift register(SIPO)
☐ Parallel In Serial Out shift register(PISO)
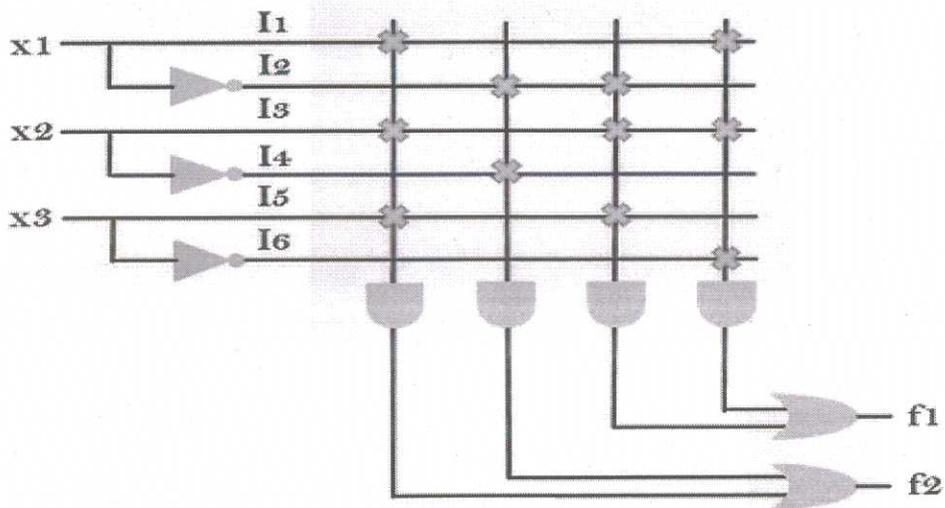☐ Parallel In parallel Out shift register(PIPO)

2 +3*2 =8marks

VIII(b)

©Elprocus.com

Clock pulse	Q2	Q1	Q0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

Diagram 4+Table3=7

IX(a)
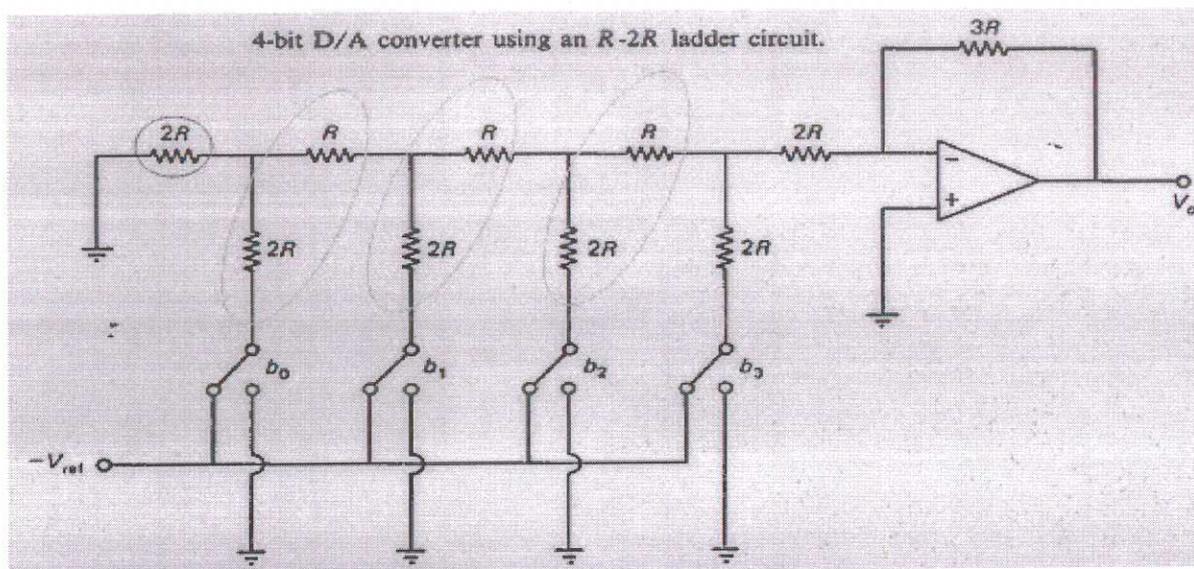

$$f_1 = x_1 x_2 x'_3 + x'_1 x_2 x_3$$
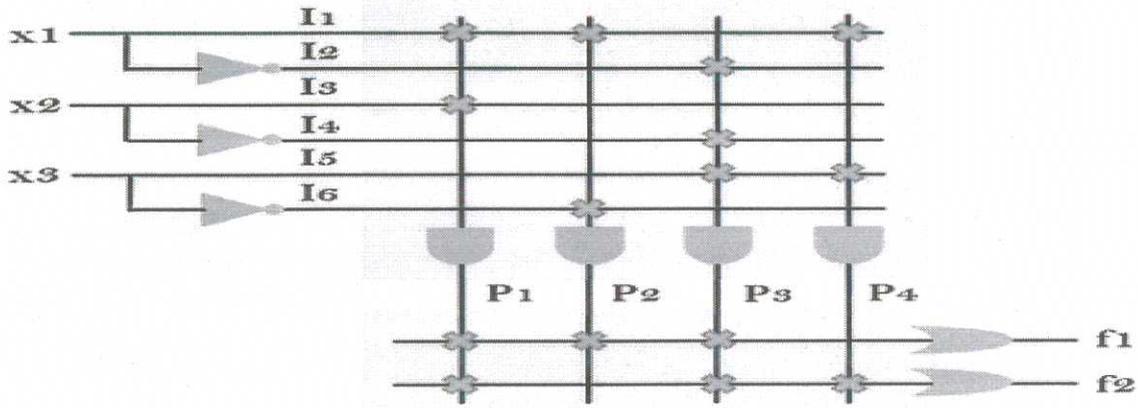$$f_2 = x'_1 x'_2 + x_1 x_2 x_3$$

Programmable Array Logic

Diagram 5+Explanation 3=8

IX(b)

4-bit D/A converter using an R-2R ladder circuit.

Circuit diagram 4+Explanations 3=7

X(a)

$$f_1 = x_1x_2 + x_1x'_3 + x'_1x'_2x_3$$
$$f_2 = x_1x_2 + x'_1x'_2x_3 + x_1x_3$$

Programmable Logic Array

Diagram 6+ Result 4=10

X(b)

- **Accuracy**

- The Accuracy of a DAC is the difference between output practical analog output to the ideal expected output for a given digital input.

- **Monotonicity**

- The Digital to Analog Converter is said to be monotonic if its analog value is either increasing or equal to previous value for an LSB change in input digital signal.

2.5*2=5