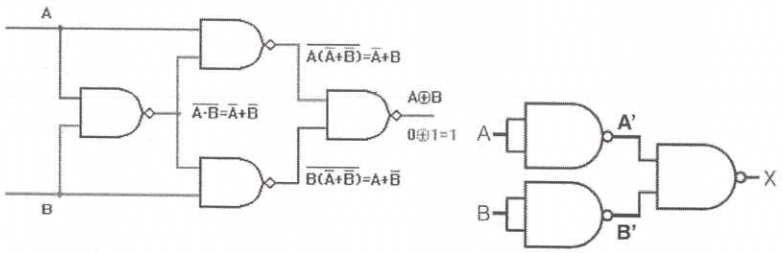
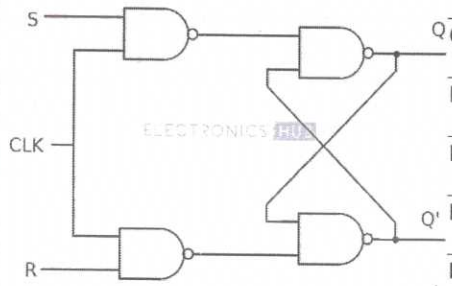
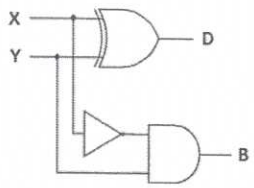
SCHEME OF VALUATION
(Scoring indicators)

A	**Revision : 2015** **Course Code: 3133** **Course Title : DIGITAL COMPUTER PRINCIPLES**			
Qst. No.	**Scoring Indicator**	**Split up score**	**Sub Total**	**Total**
	PART-A			
I. 1	XS-3code, gray code	1+1	2	
2	An encoder is a device whose inputs are decimal digits and/or alphabetic characters and whose outputs are the coded representation of those inputs.	2	2	
3	• Synchronous Circuit • Asynchronous Circuit	1+1	2	
4	The resolution of a DAC is defined as the smallest change that can occur in an analogue output as a result of a change in the digital input. The resolution of a DAC is also defined as the reciprocal of the number of discreet steps in the full scale output of the DAC.	2	2	
5	• Static RAM (SRAM) • Dynamic RAM (DRAM) • Synchronous Dynamic RAM (SDRAM) (any 2)	1+1	2	10
	PART-B			
II. 1		4+2	6	
2 a)	The binary coded decimal (**BCD**) is a type of binary **code** used to represent a given decimal number in an equivalent binary form. Its main advantage is that it allows easy conversion to decimal digits for printing or display and faster calculations. The most common **BCD code** is the 8421 **BCD code**.			
b)	Excess-3, also called XS3, is a non-weighted code used to express decimal number-s. It is another important binary code. It is particularly significant for arithmetic operations as it overcomes the shortcomings encountered while using the 8421 BCD code to add two decimal digits whose sum exceeds 9. This code is used in some old computers.	3+3	6	

3	Y= A + B'C = A(B+B')(C+C') + B'C(A + A') = AB + AB'(C+C') + B'CA + B'CA' = ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C	6	6	
4	 (+ Explanation)	2+2 +2	6	
5	D = AB' + BA' = A ◯ B and b = A'B  	4+2	6	

CLOCK	S	R	Q
LOW	X	X	Q_0
HIGH	0	0	Q_0
HIGH	0	1	0
HIGH	1	0	1
HIGH	1	1	?

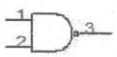
INPUTS		OUITPUTS	
A	B	d	b
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	1

6		6	6	

Sr. No.	Combinational circuits	Sequential circuits
1.	In combinational circuits, the output variables are at all times dependent on the combination of input variables.	In sequential circuits, the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.
2.	Memory unit is not required in combinational circuits.	Memory unit is required to store the past history of input variables in the sequential circuit.
3.	Combinational circuits are faster in speed because the delay between input and output is due to propagation delay of gates.	Sequential circuits are slower than the combinational circuits.
4.	Combinational circuits are easy to design.	Sequential circuits are comparatively harder to design.
5.	Parallel adder is a combinational circuit.	Serial adder is a sequential circuit.

7	In modern life, electronic equipment is frequently used in different fields such as communication, transportation, entertainment, etc. Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) are very important components in electronic equipment. Since most real world signals are analog, these two converting interfaces are necessary to allow digital electronic equipments to process the analog signals. Take the audio signal processing as an example, ADC converts the analog signal collected by audio input equipment, such as a microphone, into a digital signal that can be processed by computer. The computer may add sound effect such as echo and adjust the tempo and pitch of the music. DAC converts the processed digital signal back into the analog signal that is used by audio output equipment such as a speaker.	6	6	30
	PART-C			
III a	Law 1 : $(A + B)' = A'B'$ This law states that the compliment of sum of variables is equal to the product of their individual components. Law 2 : $(AB)' = A' + B'$ This law states that the compliment of the product of variables is equal to the sum of their individual components 1) $((AB)' + A' + AB))' = (AB)''.A''.(AB)'$ $=AB.A.(AB)'$ $= AB.(AB)'$ $= 0$ 2) $((A+B')(C+D'))'$ Compliment the entire function = $(A+B')(C+D')$	4+2 +2	8	

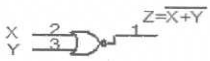
	Change ANDs to ORs and ORs to ANDs =A.B' + C.D' Compliment the entire variables = A'.B +C'.D.			
b	The advantage of performing subtraction by the complement method is reduction in the hardware . Instead of having separate digital circuits for addition and subtraction, only adding circuits are needed. That is, subtraction is also performed by adders only. Instead of subtracting one number from the other, the complement of the subtrahend is added to the minuend. 1) 110000+ 101011 (2's compliment of the subtrahend) 1,011011 (ignore the carry) Ans = 011011 2) 001001+ 011000 (2's compliment of the subtrahend) 100001 (no carry, so the answer is –ve and take the 2's compliment) Ans = -011111	2 + 2.5 +2.5	7	15
IV a	1) F A 5 . 1 6————0110 1111 0001 1010 0101 = 111110100101.00010110 2) 1,0110.0101 1 6 . 5 = 16.5 3) 32.24 3X8^1 + 2X8^0 + 2X8^-1 + 4X8^-2 = 24 + 2 + 0.25 + 0.0625 = 26.3125	2x4	8	

Qst. No.	Scoring Indicator	Split up score	Sub Total	Total
4)	8|895 8|111 7 8|13 7 8|1 5 0 1 = 1577			
IV b.	2 Input NAND Gate NAND Gate  TRUTH TABLE	3.5+ 3.5	7	

INPUTS		OUTPUT
X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

2 Input NOR Gate

NOR Gate



TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

15

V a.

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

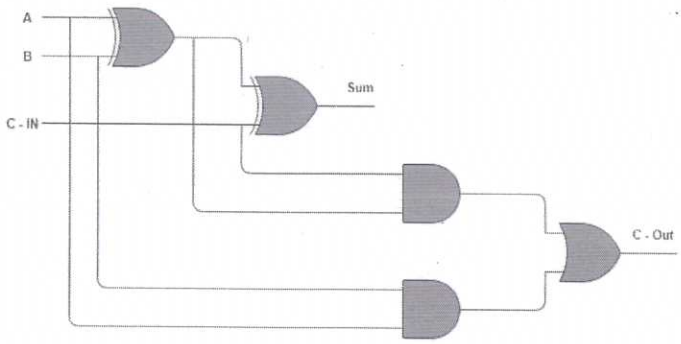
2+3

+3 8

S= A'B'C-IN + A'BC-IN' + AB'C-IN' + ABC-IN = A ○ B ○ C-IN

And C-Out = A'BC-IN + AB'C-IN + ABC-IN' + ABC-IN

= AB + (A ○ B)C-IN = AB + AC-IN + BC-IN



b

A *Karnaugh map* (*K-map*) is a pictorial method used to minimize Boolean expressions without having to use Boolean algebra theorems and equation manipulations. A *K-map* can be thought of as a special version of a truth table . Using a *K-map*, expressions with two to four variables are easily minimized. 2+5 7

Advantages of k map:

It gives a visual method of logic simplification.

It is a fast method for simplifying expressions upto four variables

Suitable for both POS and SOP reduction

K-map simplification does not demand for the knowledge of Boolean algebraic theorems

The disadvantage of k map :

It is not suitable for computer reduction. 15

It is not suitable when the number of variables involved exceed four.

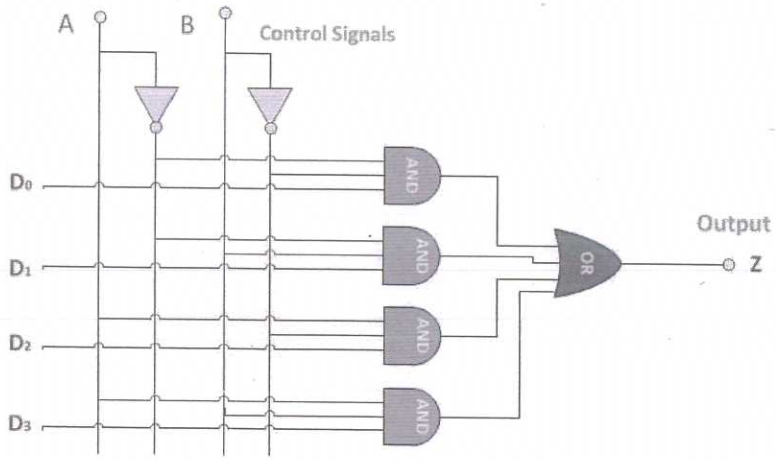
VI a

In 4:1 MUX, there will be 4 input lines and 1 output line. And to control which input should be selected out of these 4, we need 2 selection lines.

Thus, it is evident from the diagram below that D0, D1, D2 and D3 are the input lines and A, B are the two selection lines. The combination of binary numbers given as a selection line will determine the output of the MUX.

2+4 +2

8



Four – To – One Multiplexer

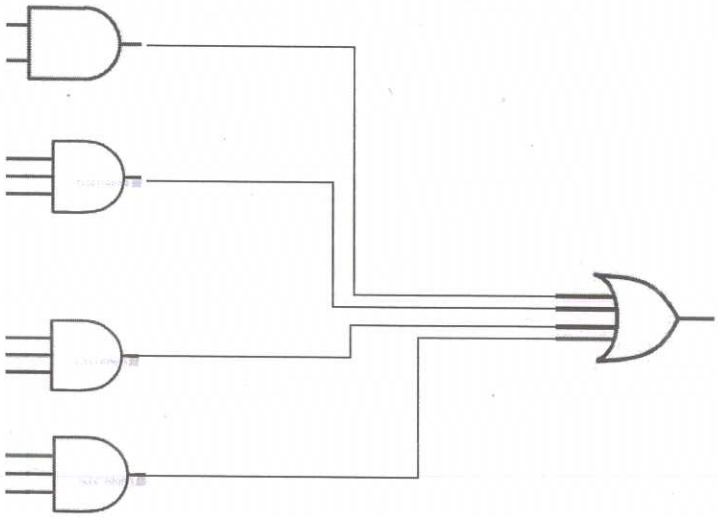
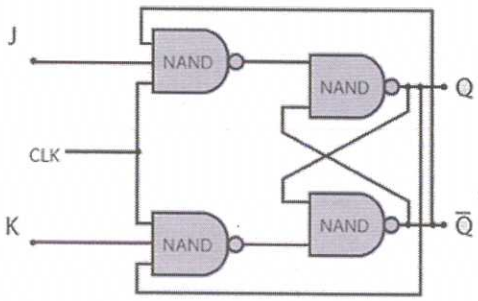
Select inputs		Output
A	B	Z
0	0	D0
0	1	D1
1	0	D2
1	1	D3

b

AB \ CD	00	01	11	10
00	0	1 1	3	2
01	4 1	5 X	7 1	6
11	12	13 1	15 X	14 X
10	8	9	11	10 1

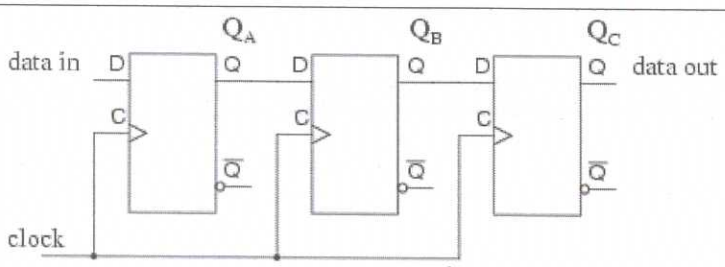
5+2

7

VII a	Z = BD + A'BC' + A'C'D + ACD'   Truth Table (plus explanation)	3+2 +3	8	15

J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

b



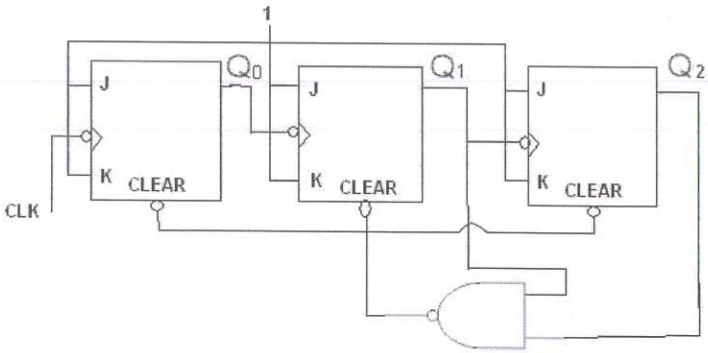
Serial-in, serial-out shift register using type "D" storage elements

(plus explanation)

4+3 | 7 | 15

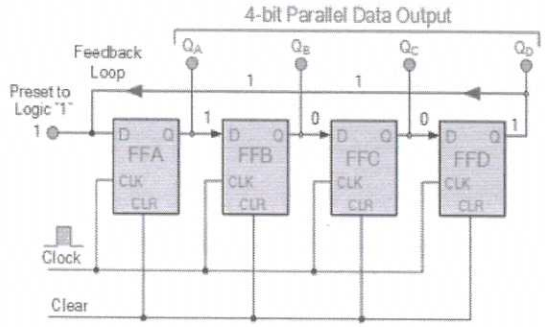
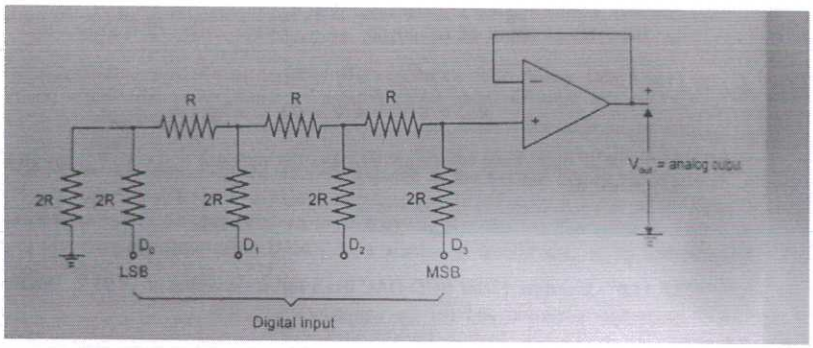
VIII

a

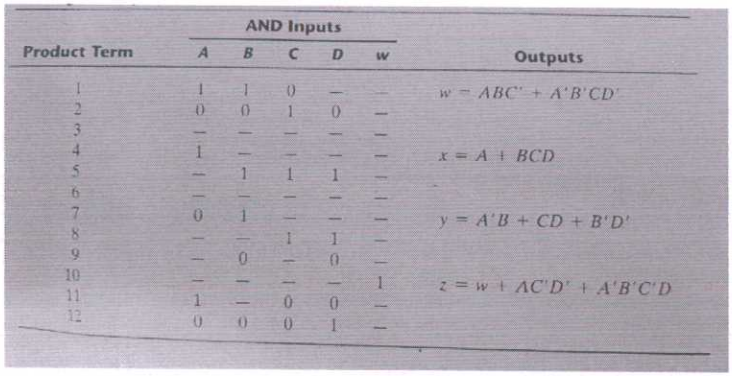


4+4 | 8

Clock	State			R
	Q_3	Q_2	Q_1	
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	1 ↓ 0	1 ↓ 0	0 ↓ 0	1 0
7	0	0	1	0

b	**4 bit Ring Counter**  30/10/2019 Prepared By Ms. K. D. Pate, SCOE, Kopargaon (plus explanation)	4 +3	7	15
IX a	 	4+4	8	

Clock Cycle	Q_A	Q_B	Q_C	Q_D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
.	.	.	.	.
.	.	.	.	.

b	**PROM :** Short for programmable read-only memory, a memory chip on which data can be written only once. Once a program has been written onto a PROM, it remains there forever. Unlike RAM, PROMs retain their contents when the computer is turned off. The difference between a PROM and a ROM (read-only memory) is that a PROM is manufactured as blank memory, whereas a ROM is programmed during the manufacturing process. To write data onto a PROM chip, you need a special device called a PROM programmer or PROM burner. The process of programming a PROM is sometimes called burning the PROM. **EPROM :** Acronym for erasable programmable read-only memory, and pronounced ee-prom, EPROM is a special type of memory that retains its contents until it is exposed to ultraviolet light. The ultraviolet light clears its contents, making it possible to reprogram the memory. To write to and erase an EPROM, you need a special device called a PROM programmer or PROM burner. **EEPROM :** Short form of electrically erasable programmable read-only memory. EEPROM is a special type of PROM that can be erased by exposing it to an electrical charge. Like other types of PROM, EEPROM retains its contents even when the power is turned off. Also like other types of ROM, EEPROM is not as fast as RAM.	7	7	15
X a	 AND Inputs Product Term | A | B | C | D | w | Outputs 1 | 1 | 1 | 0 | – | – | $w = ABC' + A'B'CD'$ 2 | 0 | 0 | 1 | 0 | – 3 | – | – | – | – | – 4 | 1 | – | – | – | – | $x = A + BCD$ 5 | – | 1 | 1 | 1 | – 6 | – | – | – | – | – 7 | 0 | 1 | – | – | – | $y = A'B + CD + B'D'$ 8 | – | – | 1 | 1 | – 9 | – | 0 | – | 0 | – 10 | – | – | – | – | 1 | $z = w + AC'D' + A'B'C'D$ 11 | 1 | – | 0 | 0 | – 12 | 0 | 0 | 0 | 1 | –	4x2	8	
b	One type of error correction code is the hamming code. To transmit four data bits, three parity bits located at positions 2^0, 2^1, and 2^2 are added to make a 7 bit code word which is then transmitted. The word format would be as shown below. $D_7\ D_6\ D_5\ P_4\ D_3\ P_2\ P_1$ Where D bits are the data bits and the P bits are parity bits. P_1 is set to a 0 or 1 so that it establishes even parity over bits 1,3, 5 and 7. P_2 is set to a 0 or 1 to establish even parity over bits 2, 3, 6 and 7. P_4 is set to a 0 or 1 to establish even parity over bits 4,5, 6 and 7.			

	At the receiving end ,the message received in Hamming code is decoded to see if any errors have occurred. Bits 1, 3, 5, 7 bits 2, 3, 6, 7 and bits 4, 5, 6, 7 are all checked for even parity.If there is an error the error bit can be located by forming a 3 bit binary number out of the three parity checks and the error bit is then corrected by complementing it.			