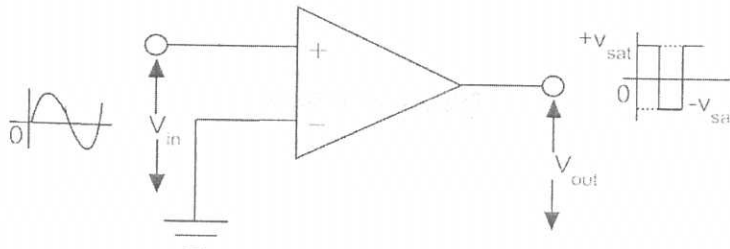


SCHEME OF VALUATION

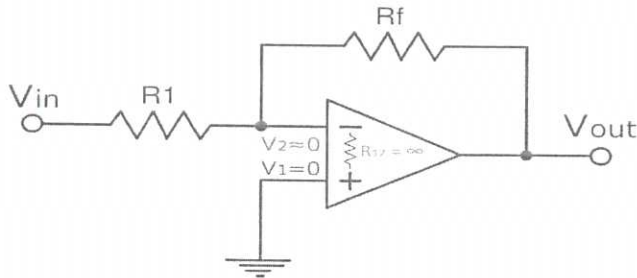
(Scoring Indicators)

Q.No	Scoring Indicator	Split up score	Sub total	Total
Revision.2015 <span style="float: right;">Course code :4042</span>				
<b>LINEAR INTEGRATED CIRCUITS</b>				
I	<b>PART A</b>			
1)	$A_v = 1 + (R_f/R_i)$		2	
2)	It is defined as the rate of change of o/p voltage with respect to time. $S = dV_o/dt$ Unit is volt per microseconds	2x1	2	
3)			2	
4)	It operates from a wide range of power supplies ranging from + 5 Volts to + 18 Volts . Sinking or sourcing 200 mA of load current. It has a high current output; the output can drive TTL. It has a temperature stability.	(any two) 2x1	2	
5)	O/p V of 7905 is -5v and 7812 is +12v	2x1	2	10
II	<b>PART B</b>			
1)	<ol style="list-style-type: none"> <li>1. Infinite voltage gain</li> <li>2. Infinite input impedance</li> <li>3. Zero output impedance</li> <li>4. Infinite bandwidth</li> <li>5. Zero input offset voltage (i.e., exactly zero out if zero in).</li> <li>6. Infinite bandwidth</li> <li>7. Infinite CMRR</li> <li>8. Infinite slew rate</li> <li>9. Zero input noise</li> </ol>	6X1	6	
2)	For opamps the gain will be very high such that we can consider it as infinite for calculation purposes.			
		3		

Gain =  $V_o/V_{in}$

As gain is infinite,  $V_{in} = 0$

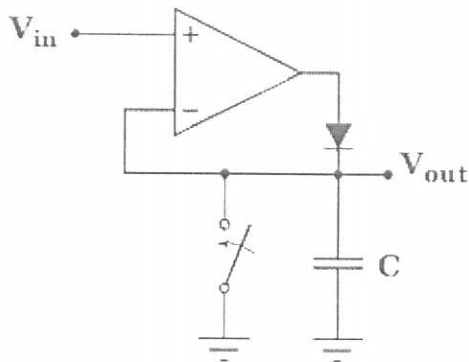
- $V_{in} = V_2 - V_1$



In the above circuit  $V_1$  is connected to ground, so  $V_1 = 0$ . Thus  $V_2$  also will be at ground potential.

- $V_2 = 0$ . This is the virtual ground concept.

3)



assume the switch is open and if

$V_{out} < V_{in}$  the op amp output  $V'$  is positive so that the diode conducts and the capacitor charges to the input value at that instant as it forms a voltage follower circuit.

When  $V_{out} > V_{in}$ , op amp output  $V'$  is negative and the diode becomes reverse biased. Thus the capacitor charges to the most positive value of input.

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6

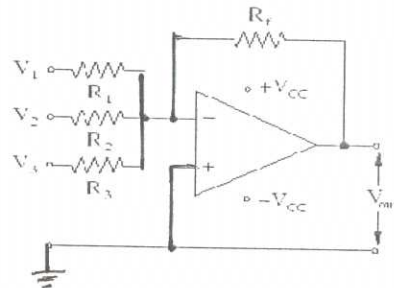
Dia(3  
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6  
Exp(3  
)

4)

- Here the input voltages  $V_1, V_2, V_3$  are given in to adder circuit.

This is an inverting summing amplifier because output is the sum of inputs with a sign change



3

To construct a non inverting adder, you can cascade one inverting amplifier with unity gain along with this circuit.

For that consider  $R_1=R_2=R_3=R_f=R$

Then the Output of this adder circuit is given by  $-(V_1+V_2+V_3)$ .

- Consider the current flowing through the input resistors are

$$I_1 = \frac{V_1}{R}$$

$$I_2 = \frac{V_2}{R}$$

$$I_3 = \frac{V_3}{R}$$

- Then by Kirchof's current law, the current flowing through feedback resistor  $R_f$  is given by the sum of these 3 currents.

$$I_K = I_1 + I_2 + I_3$$

$$= \frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}$$

$$= \frac{1}{R} (V_1 + V_2 + V_3)$$

- This current will flows through the feedback resistor  $R_f$ , because the point 'K' acts as *virtual* ground point. So the voltage drop at  $R_f$  is given by

$$V_O = -I_K R$$

$$= -\frac{1}{R} (V_1 + V_2 + V_3) R$$

$$= -(V_1 + V_2 + V_3)$$

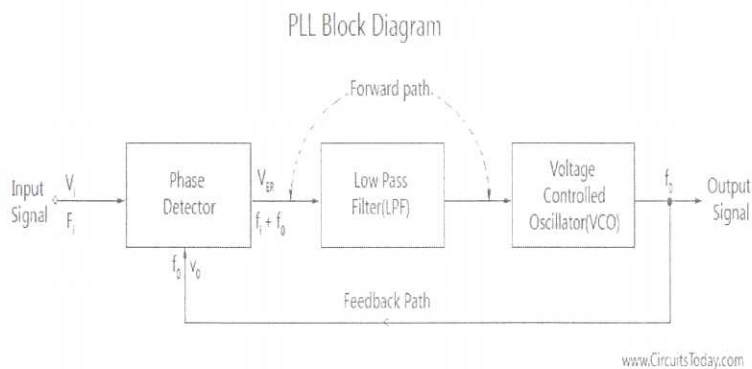
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6

- -ve sign is due to the op amp connected in inverting mode.
- This circuit is called a summing ‘amplifier’ because it can provide gain. By adjusting the value of Rf the gain can be changed.
- Then the output becomes

$$V_O = -\frac{R_F}{R} (V_1 + V_2 + V_3)$$

5)



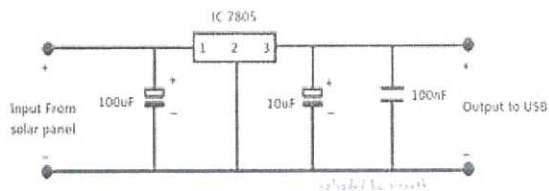
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he phase locked loop consists of a phase detector, a voltage control oscillator and, in between them, a low pass filter is fixed. The input signal ‘Vi’ with an input frequency ‘Fi’ is conceded by a phase detector. Basically the phase detector is a comparator which compares the input frequency  $f_i$  through the feedback frequency  $f_o$ . The output of the phase detector is  $(f_i + f_o)$  which is a DC voltage. The out of the phase detector, i.e., DC voltage is input to the low pass filter (LPF); it removes the high frequency noise and produces a steady DC level,

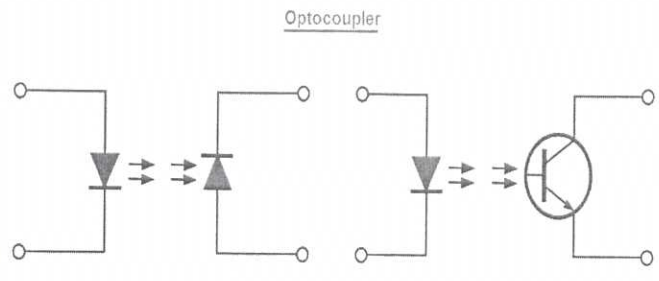
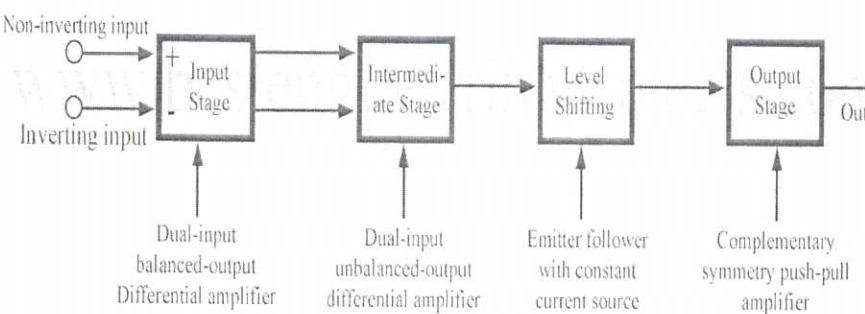
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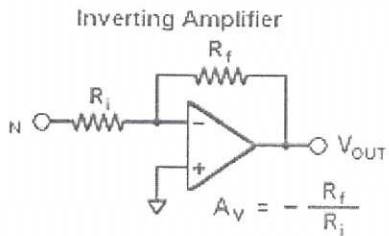
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6)



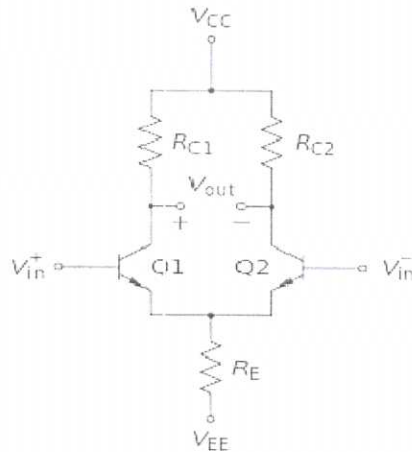
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	<p style="text-align: center;">Explanation</p> <p>7) An optocoupler is an optical link and it connects two circuits via this link.</p> <p style="text-align: center;"><u>Optocoupler</u></p>  <p style="text-align: center;">Fig a : LED to Photodiode      Fig b : LED to Phototransistor</p> <p>The optical link is contained within a chip. A Light Emitting Diode inside the chip shines on a photo-diode, photo-transistor or other photo device. When the photo device sees illumination, the resistance between its terminals reduces. This reduced resistance can activate another circuit.</p>	3	6	
<p>III a)</p>	<p style="text-align: center;">PART C</p>  <p style="text-align: center;">Figure 1: Block Diagram of a Typical Op-amp</p> <p><b>Input Stage:</b></p> <ol style="list-style-type: none"> <li>Increases the CMRR.</li> </ol>	4		30

<p>b)</p>	<p>2. High gain requirement is adjusted.  3. Most of the gain is adjusted.  4. Provides the input impedance very high.</p> <p><b>Intermediate Stage:</b></p> <p>1. Driven by output of 1<sup>st</sup>  2. Adjust the half gain of 1<sup>st</sup>  3. Error voltage is cancelled in this stage.</p> <p><b>Level Shifting:</b></p> <p>1. Suppress the dc level downward to zero volt with respect to ground  2. Consisting of current amplifiers as emitter followers.  3. Also minimizes the error by suppressing dc level to ground.</p> <p>Output Stage:</p> <p>1. This stage increases the output voltage swing and the current in supplying capability of the amplifiers.  2. Provides low output impedance</p> <p style="text-align: center;"><b>Inverting Amplifier</b></p>  <p style="text-align: center;"><math>A_v = -\frac{R_f}{R_i}</math></p> <p>Current through <math>R_i</math> is <math>I_i</math> and current through <math>R_f</math> is <math>I_f</math>. Due to virtual ground concept, <math>I_i = I_f</math>  <math>I_i = V_{in}/R_i</math> and <math>I_f = -V_{out}/R_f</math>  So <math>A_v = V_{out}/V_{in} = -R_f/R_i</math></p>	<p>4</p> <p>8</p> <p>4</p> <p>3</p>	<p>15</p> <p>7</p>
<p>IV a)</p>	<p>Differential output- With two inputs and two outputs, this forms a differential amplifier stage. The two bases are inputs which are differentially amplified by the transistor pair; they can be fed with</p>		

a differential (balanced) input signal

Single-ended output- If the differential output is not desired, then only one output can be used (taken from just one of the collectors , disregarding the other output; this configuration is referred to as single-ended output. The gain is half that of the stage with differential output



**Single-ended input-** The differential pair can be used as an amplifier with a single-ended input if one of the inputs is grounded or fixed to a reference voltage (usually, the other collector is used as a single-ended output)

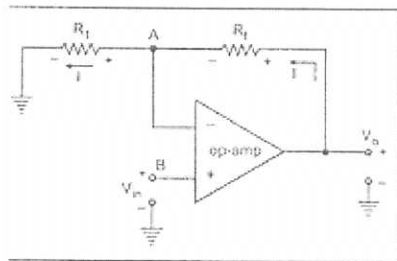


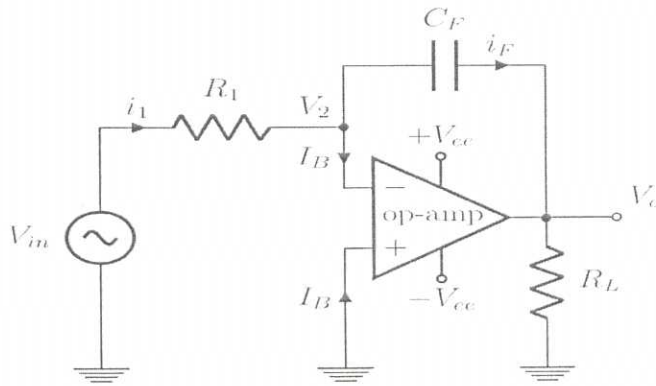
Fig. 2.20 Noninverting amplifier

The op amp has two input terminals (pins). One is inverting denoted with minus sign (-), and other is non-inverting denoted with a positive sign (+). When we apply any signal to the non – inverting input of, it does not change its polarity when it gets amplified at the output terminal. So, in that case, the gain of the amplifier is always positive.

$$A = \left( 1 + \frac{R_f}{R_1} \right)$$

<p>V</p> <p>a)</p>	<p><b>Astable multivibrator</b> is capable of producing square wave for a given frequency, Amplitude and Duty cycle. The output of <b>OP AMP</b> is forced to swing between positive saturation, <math>+V_{sat}</math> and negative saturation, <math>-V_{sat}</math> repeatedly. Which will results in Square wave output. This circuit is also called as Free Running Oscillator. Because, it doesn't requires any trigger pulse to get active. The output of an operational amplifier will be in positive saturation <math>V_{sat}</math>, if the differential input voltage is negative and vice versa. The differential voltage, <math>V_d = V_c - \beta V_{sat}</math>. Where <math>\beta</math> is the feedback factor and <math>\beta V_{sat}</math> is the potential at non-inverting terminal of the op amp.</p> <p>Consider the instant at which <math>V_c = +V_{sat}</math>. Now the capacitor charges exponentially towards <math>+V_{sat}</math> through R. Automatically, <math>V_d</math> increases and crosses zero. This happens when <math>V_c = +\beta V_{sat}</math>. At the moment <math>V_d</math> becomes positive due to further charging of the capacitor. Output changes to <math>-V_{sat}</math>. Now capacitor starts discharging to zero and recharges towards <math>-V_{sat}</math>. Now <math>V_d</math> decreases and crosses zero. This happens when <math>V_c = -\beta V_{sat}</math>. At the moment <math>V_d</math> becomes negative again, output changes to <math>+V_{sat}</math>. This completes one cycle of output. Astable multivibrator is useful for generating audio frequency</p> <div data-bbox="383 1288 917 1680" data-label="Diagram"> </div> <p>signals.</p>	<p>4</p>	<p>4</p> <p>8</p>
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b) The circuit operates by passing a current that charges or discharges the capacitor  $C_F$  during the time under consideration, which strives to retain the virtual ground condition at the input by off-setting the effect of the input current. Referring to the above diagram, if the op-amp is assumed to be ideal, nodes  $v_1$  and  $v_2$  are held equal, and so  $v_2$  is a virtual ground.



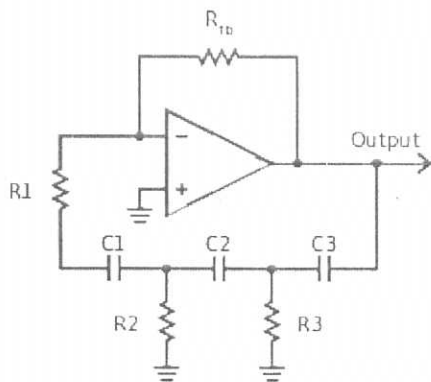
The input voltage passes a current through the resistor producing a compensating current flow through the series capacitor to maintain the virtual ground. This charges or discharges the capacitor over time. Because the resistor and capacitor are connected to a virtual ground, the input current does not vary with capacitor charge and a linear integration of output is achieved

$$V_0 = -\frac{1}{R_1 C_F} \int_0^t V_{in} dt$$

VI  
a)

A phase-shift oscillator is a linear electronic oscillator circuit that produces a sine wave output. It consists of an inverting amplifier element such as a transistor or op amp with its output fed back to its input through a phase-shift network consisting of resistors and capacitors in a ladder network. The feedback network 'shifts' the phase of the amplifier output by 180 degrees at the

oscillation frequency to give positive feedback. Phase-shift oscillators are often used at audio frequency as audio oscillators



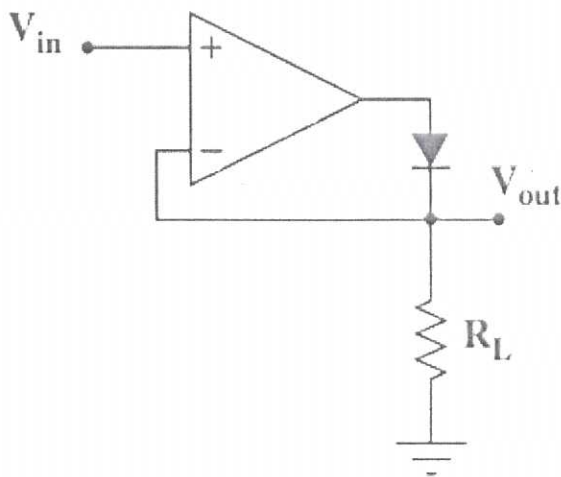
$$F = 1/2\pi RC\sqrt{6}$$

3

8

1

- b) For normal silicon diode to be on the minimum positive bias should be greater than the cut in voltage. Hence the diodes when used in rectification will have a dead time in which they will not conduct currents even when the voltages are positive ( $0 < V_d < V_{cut \text{ in voltage}}$ ). An ideal diode should have zero cut in voltage. A simple half wave rectifier is shown in the figure



4

When  $V_{out} < V'_{out}$ , diode will be on and the circuit reduces to voltage follower in which  $V_{out} = V_{in}$ . Because of high gain of op amps the input cut in voltage will be reduced to  $V_{\gamma}/A_{v0}$ .

3

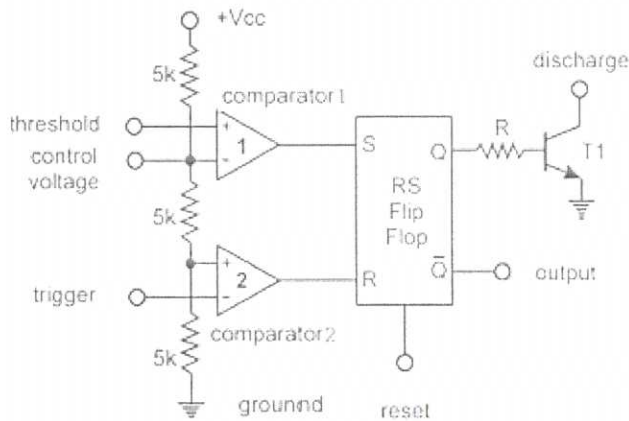
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where  $A_{vo}$  is the open loop gain of opamp. Thus for even for very small input positive voltages the output will be high, the combination of op amp and diode acts as diode with zero cut in voltage hence it is named as precision diode.

VII

a)



As shown in the above figure there are only two important components in timer, they are comparator and flip-flop. comparator is simply a device that compares the voltages at the input terminals (inverting (-VE) and non-inverting (+VE) terminals). So depending on the difference in the positive terminal and negative terminal at input port, the output of the comparator is determined. The flip-flop is a memory cell, it can store one bit of data. One another thing is comparator one output is connected to reset pin of flip-flop, so if the comparator one output goes high from low then the flip-flop will reset. And on the other hand the second comparator output is connected to set pin of flip-flop, so if the second comparator output goes high from low the flip-flop sets and stores ONE.

diagram -5 marks, explanation – 3 marks

5

8

3

b)

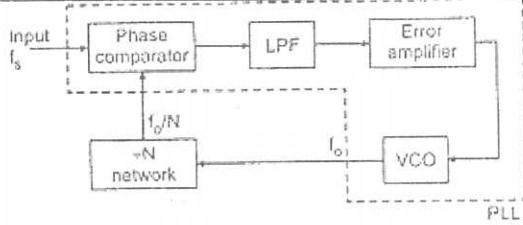


Fig. 2.128 Block diagram of frequency multiplier

Fig. Shows the block diagram for a frequency multiplier using PLL 565. Here a divide by N network is inserted b/w the VCO o/p and the phase comparator i/p. Since the o/p of the divider is locked to the i/p frequency  $f_i$ , the VCO is actually running at a multiple of the i/p frequency. So in the locked state, the VCO o/p frequency  $f_o$  is given by

$$f_o = Nf_i \quad \dots (1)$$

By selecting proper divider by N network, we can obtain desired multiplication.

4

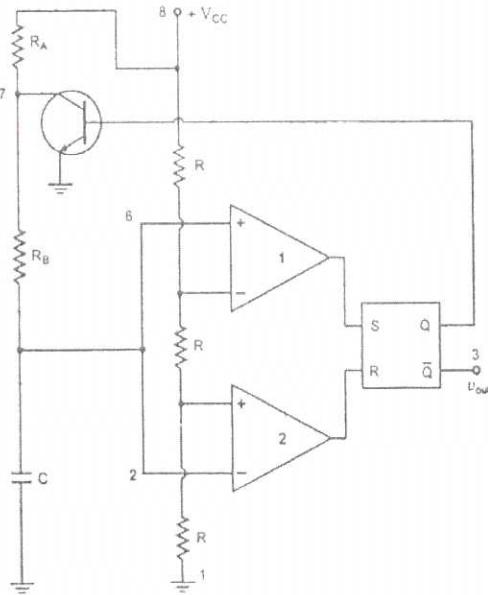
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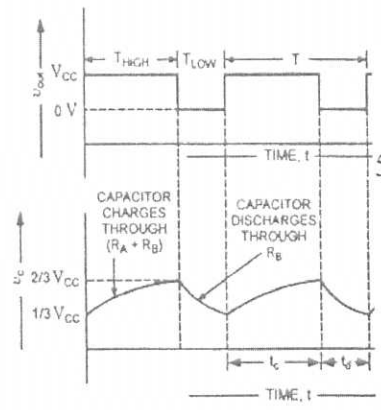
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VIII

a)



Internal Circuitry With External Connections



Capacitor and Output Voltage Wave

When the power is turned ON consider the flip flop is cleared

initially, then the o/p of the inverter will be high. The charging of the capacitor will be done using two resistors RA& RB. When the voltage of the capacitor goes above 2/3 Vcc, then the output of the higher comparator will be High, it changes the control flip flop. So the control flip-flop's Q o/p will be a LOW & Q' will be High. So the final o/p of the Inverter is LOW. At the same time the Q1 transistor switches ON and the C capacitor starts discharging through resistor R2.

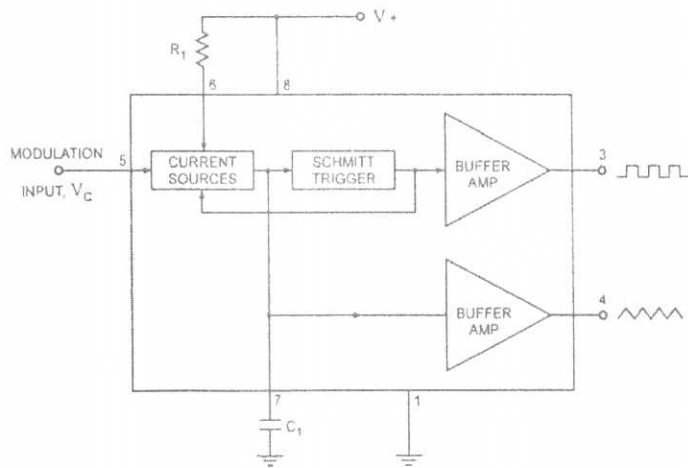
When the voltage of the capacitor is  $< 1/3V_{cc}$ , then the o/p of the lower comparator will be high and control flip flop gets is set to 1. When the discharge transistor Q1 gets off, then the capacitor gets charged and continues this process.

**Time High** (Seconds)  $t_c = 0.693 * (R_A + R_B) * C$

**Time Low** (Seconds)  $t_d = 0.693 * R_B * C$

VCO

b)



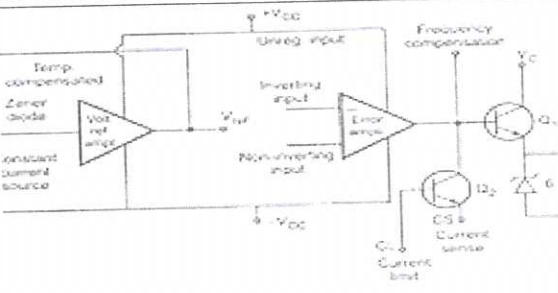
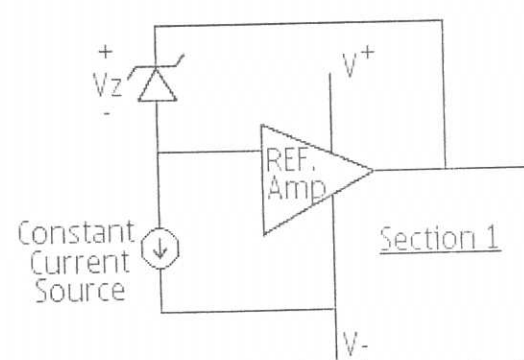
(a) Block Diagram

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Resistor R1 and capacitor C1 form the timing components. A LM567 is a voltage controlled oscillator IC unit which is built with internal circuitry to generate

3

8

4

	<p>both triangular and square wave signals whose frequency is set or adjusted by external capacitor and resistor followed with an application of DC voltage.</p> <p>The figure below shows the block diagram of LM566 IC in which current sources charge and discharge the external capacitor at its rate set by the resistor R1 and also controls the DC input voltage. For switching the capacitor between charging and discharging, a Schmitt trigger circuit is used as shown in figure.</p> <p>The square wave voltage developed from Schmitt trigger and the triangular voltage across capacitor are provided as outputs through buffer amplifiers.</p> <p>The output frequency of the VCO can be obtained using the following equation:</p> $F_{out} = 2.4(V^+ - V_5) / (R1C1V^+)$ <p>Where <math>F_{out}</math> is the output frequency, R1 and C1 are the timing components and <math>V^+</math> is the supply voltage.</p>	3	7	15
IX a)	 <p>IC 723 has two sections. As shown in the block diagram,</p>  <p>A constant current Source:- A zener diode and a reference amplifier producing a constant voltage of about 7 volts at <math>V_{ref}</math> end. The zener diode is being compelled to operate at fixed point (so that zener</p>	4	8	2

output voltage is a fixed voltage) by a constant current Source.

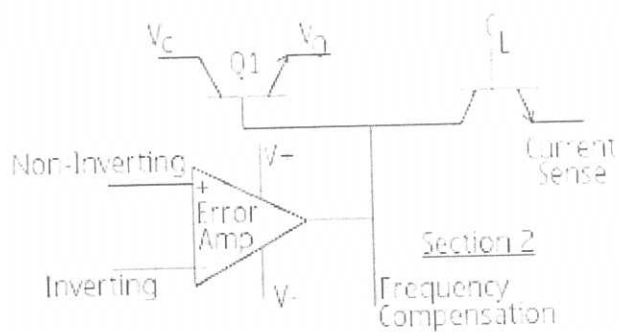


Figure 2.10: Section 2 of IC 723

The second section of IC 723 comprises of an error amplifier, a series pass transistor Q1 and a current limiting transistor. The error amplifier compares a sample of output voltage applied at Inverting input terminal to the reference voltage  $V_{ref}$  applied at the Non-Inverting terminal.

The conduction of the transistor Q1 is controlled by the error signal.

b)

#### Advantages

1. The switch mode power supply has a smaller in size.
2. The SMPS has light weight.
3. It has a better power efficiency typically 60 to 70 percent.
4. It has a strong anti interference.
5. SMPS has wide output range.
6. Low heat generation in SMPS.

#### Disadvantages

1. The switch mode power supply (SMPS) is more complex.
2. The SMPS has higher output ripple and its regulation is worse.
3. It can be used only as a step down regulator.
4. It has only one output voltage.
5. It has high frequency electrical noise.
6. SMPS also cause harmonic distortion.

2

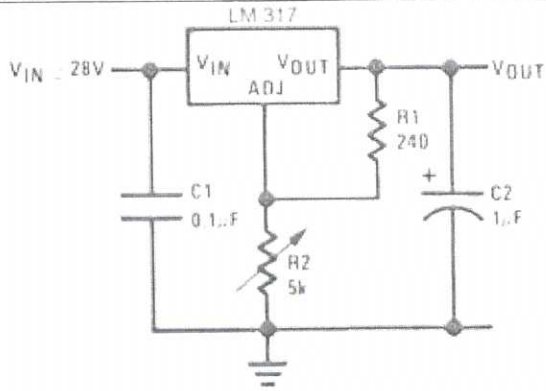
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X  
a)



- It is capable of providing excess current of 1.5A, hence it is conceptually considered as operational amplifier with an output voltage ranging from 1.2V to 37V.
- The LM317 voltage regulator circuit internally consists of thermal overload protection and short circuit current limiting constant with temperature.

The LM317 regulator can provide excess output current and hence with this capacity, it is conceptually considered as an operational amplifier. The adjustment pin is the inverting input of the amplifier and to produce a stable reference voltage of 1.25V, an internal bandgap reference voltage is used to set the non-inverting input.

The output pin voltage can be continuously adjusted to a fixed amount using a resistive-voltage divider between the output and ground, which will configure the operational amplifier as a non-inverting amplifier.

A bandgap reference voltage is used to produce constant output voltage irrespective of the changes in supply power. It is also called as temperature independent reference voltage frequently used in integrated circuits.

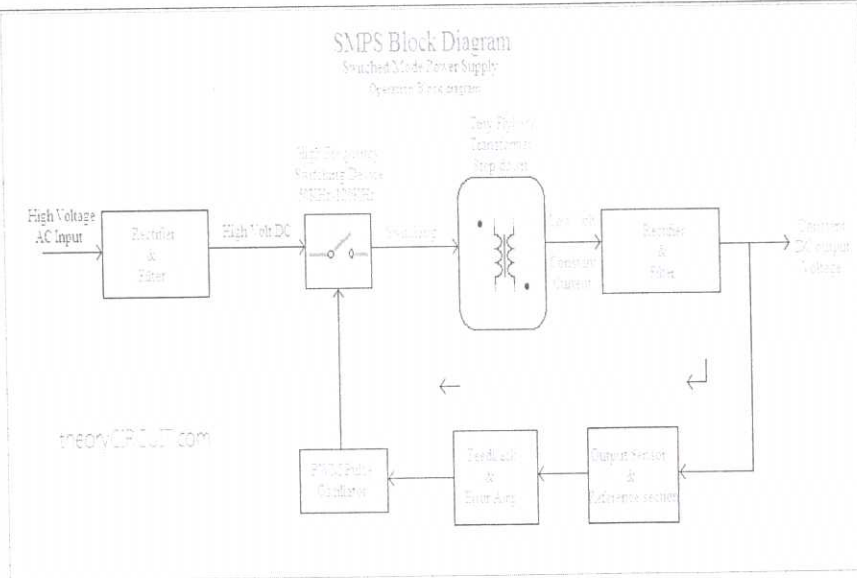
The output voltage (ideally) of the LM317 voltage regulator circuit  
 $V_{out} = V_{ref} * (1 + (R2/R1))$

4

7

3

b)



4

8

15

Switched mode power supplies or **SMPS** act as DC to DC converters. here we directly convert 230v ac to 12v unregulated dc by using rectifier ic the we use a capacitor filter then we use flyback converter (high frequency transformer is there) which switch (mosfet) is controlled by the pwm ic where reference is compared with the actual output and switching is done for regulated output and then filter it

4