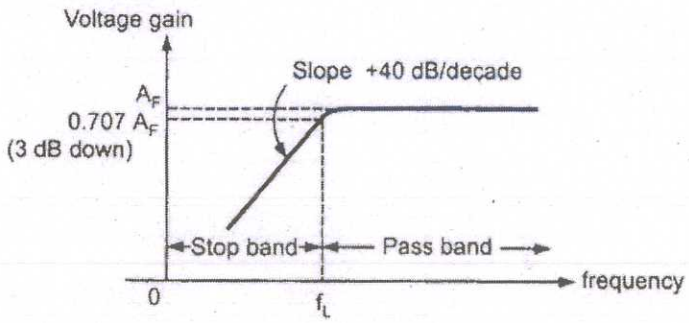
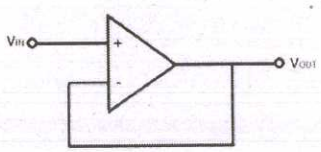
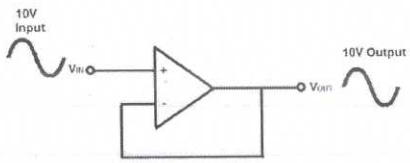
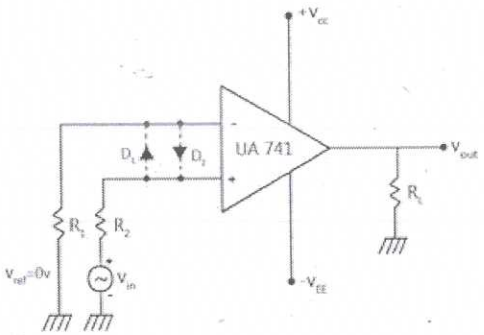
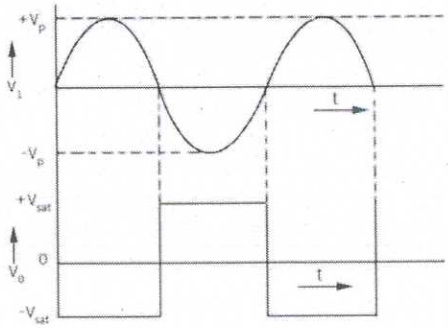
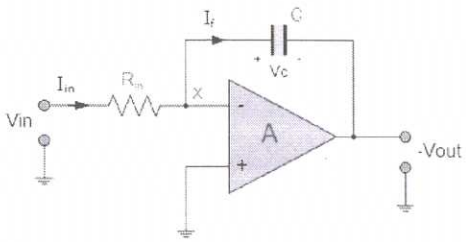
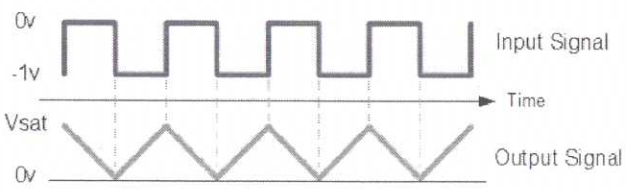
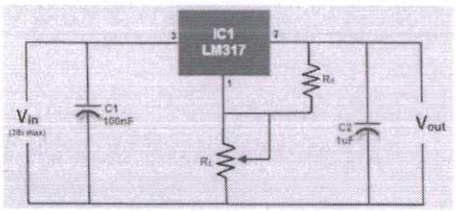
SCHEME OF EVALUATION
Scoring Indicators)

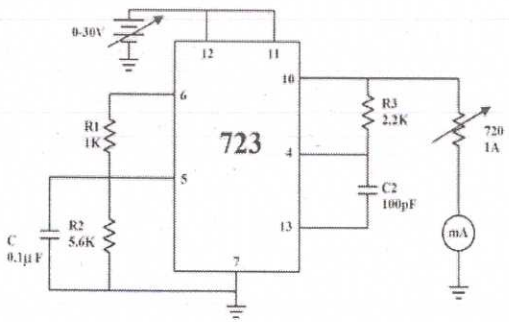
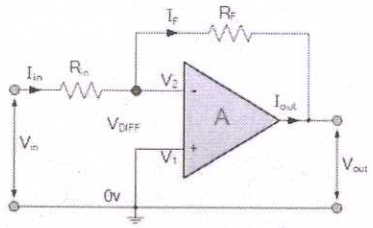
Revision:2015 Course Code:4042
Course Title: Linear Integrated Circuits

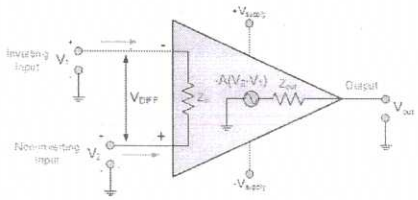
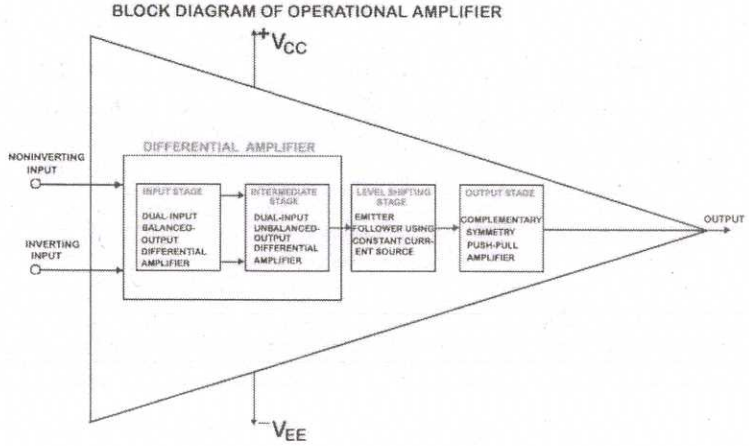
Q.NO	Scoring Indicators	Split up score	Sub Total	Total
	PART A	Any two		
I .1.	DIP, flat, metal can	2	2	
2.	CMMR stands for Common Mode Rejection Ratio and it is defined as the ratio of differential voltage gain to common mode voltage gain CMMR = Ad/Ac Where Ad is Differential voltage gain and Ac is common mode voltage gain	2	2	10
3		2	2	
. 4.	$T = t_1 + t_2 = 0.693(R_1 + 2R_2).C$	2	2	
5.	**Advantages** 1. The switch mode power supply has a smaller in size. 2. The SMPS has light weight. 3. It has a better power efficiency typically 60 to 70 percent. 4. It has a strong anti interference. 5. SMPS has wide output range. 6. Low heat generation in SMPS.	Any two 2	2	
	PART B			
II 1.	 A **voltage follower** is a op-amp circuit which has a voltage gain of	fig3+ exp3	6	30

2	1.The op amp does not provide any amplification to the signal. It is called a voltage follower because the output voltage directly follows the input voltage, meaning the output voltage is the same as the input voltage. A voltage follower acts as a buffer, providing no amplification or attenuation to the signal.  It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The input voltage to be compared, must be made zero (Vref = 0V). An input sine wave is given as Vin..  when the input sine wave passes through zero and goes in positive direction, the output voltage Vout is driven into negative saturation. When the input voltage passes through zero and goes in the negative direction, the output voltage is driven to positive saturation. The diodes D1 and D2 are also called clamp diodes. They are used to protect the op-amp from damage due to increase in input voltage. 	circuit 2 +exp2 +wave forms2	6	

3	 **Op-amp Integrator** is an operational amplifier circuit that performs the mathematical operation of **Integration**, Thee op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage.*  the voltage across the capacitor is output Vout therefore: - Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as: $V_c = \frac{Q}{C}, \quad V_n = V_{in} - V_{out} = 0 - V_{out}$ $\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$ But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, the input current I(in) flowing through the input resistor, Rin is given $I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$ The current flowing through the feedback capacitor C is given as: $I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$ $I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$ $\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$	fig2+eqn2+exp2	6	

4	$V_{out} = -\frac{1}{R_n C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$ Capture Range: The range of frequencies over which the PLL can acquire lock with an i/p signal. Lock in range: The range of frequencies over which the PLL can maintain lock with the incoming signal. Pull in time: The total time taken by the PLL to establish lock .	2+2+2	6	
5	Direct replacement for SE556/NE556 Timing from microseconds to hours Operates in both astable and monostable modes Replaces two 555 timers Adjustable duty cycle Output can source or sink 200mA Output and supply TTL compatible Temperature stability better than 0.005% per °C Normally on and normally off output Low turn off time, less than 2μs	Any 6X1	6	
6	 The LM317 regulator can provide excess output current. The adjustment pin is the inverting input of the amplifier and to produce a stable reference voltage of 1.25V, an internal bandgap reference voltage is used to set the non-inverting input.The output pin voltage can be continuously adjusted to a fixed amount using a resistive-voltage divider between the output and ground, which will configure the operational amplifier as a non-inverting amplifier.A bandgap reference voltage is used to produce constant output voltage irrespective of the changes in supply power.The output voltage of the LM317 voltage regulator circuit Vout = Vref * (1+ (RL/RH)) An error term is added because some quiescent current flows from the adjustment pin of the device. Vout = Vref * (1+(RL/RH)) + IQR	Fig 2+exp 4	6	

7	723 is the most versatile of the monolithic voltage regulators. It can be used to provide high and low positive regulated voltages .Current can be boosted to provide 5A or more. It has short circuit protection. The input voltage of IC723 vary from 9.5V to 40V and provide output voltage from 2V to 37V. IC 723 regulator has two separate sections. One section provides a fixed voltage of 7.15v at the terminal Vref, other section consists of an error amplifier. These two sections are not internally connected. For constructing low voltage regulator using 723, Vref point is connected through a resistance to the non-inverting terminal and the output is feedback to the inverting terminal of the error amplifier. If the output voltage becomes low, the voltage at the inverting terminal of error amplifier also goes down. Thus make the output of the error amplifier become more positive, there by driving transistor more into conduction. This reduces the voltage across transistor and drives more current into the load, causing voltage across the load to increase. Thus the initial decrease in the load voltage is compensated. Similarly any increase in the load voltage gets regulated  		6	
III a	**PART C**  The i/p signal Vin is applied to the invertind i/p terminal through Rin. The non inverting terminal is grounded.The o/p Vout id fed back to the i/p through Rin –Rf network.OP-AMP is ideal. So Vd = 0 . The current Iin= Vin/Rin.	fig3+ exp3 fig3+ exp5	8	

III b	Vout= -IinRf =-Vin/Rin *Rf. The gain A=Vout/Vin=-RF/Rin.  1. Infinite open loop gain. 2. Infinite I/P impedance. 3. Zero o/p impedance. 4. Infinite Bandwidth 5. Zero offset voltage.	fig2+ exp5	7	
IV a	The op-amp begins with a differential amplifier stage, which operates in the differential mode. Thus the inputs noted with '+' & '- ' . The positive sign is for the non-inverting input and negative is for the inverting input. The inverting and non-inverting inputs are provided to the input stage which is a dual input, balanced output differential amplifier. The voltage gain required for the amplifier is provided in this stage along with the input resistance for the op-amp. The output of the initial stage is given to the intermediate stage, which is driven by the output of the input stage.In this stage direct coupling is used, which makes the dc voltage at the output of the intermediate stage above ground potential. Therefore, the dc level at its output must be shifted down to 0Volts with respect to the ground. For this, the level shifting stage is used where usually an emitter follower with the constant current source is applied. The level shifted signal is then given to the output stage where a push-pull amplifier increases the output voltage swing of the signal and also increases the current supplying capability of the op-amp.  	fig4+ exp4	8	

IV b

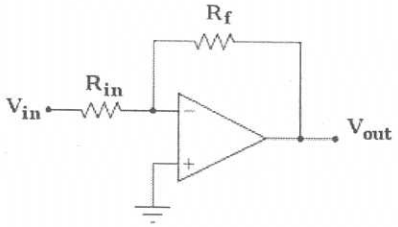


fig2+ exp5 | 7

Assume V1 is the V_1 voltage at non inverting terminal, V_2 at inverting terminal. By definition $V_0 = AV_{d, ie}$ $A(V_1 - V_2)$.

$V_1 - V_2 = V_0/A$.

For ideal op amp A= infinity. Hence $V_1 - V_2 = 0$ or $V_1 = V_2$. In the circuit the non inverting terminal is grounded. Since the differential i/p voltage is zero, the inverting terminal voltage V_2 is at ground potential. Therefore the inverting terminal is said to be at virtual ground.

V.a

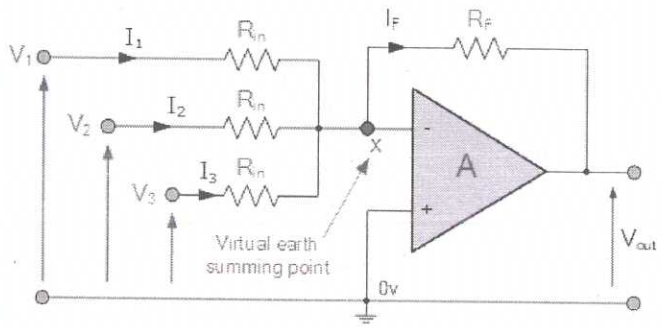


fig3+ exp5 | 8

Summing Amplifier is a type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage. In this simple summing amplifier circuit, the output voltage, (Vout) now becomes proportional to the sum of the input voltages, V1, V2, V3, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

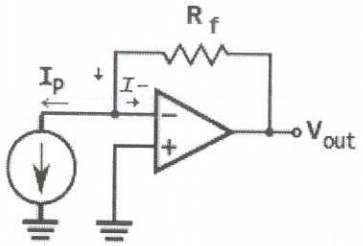
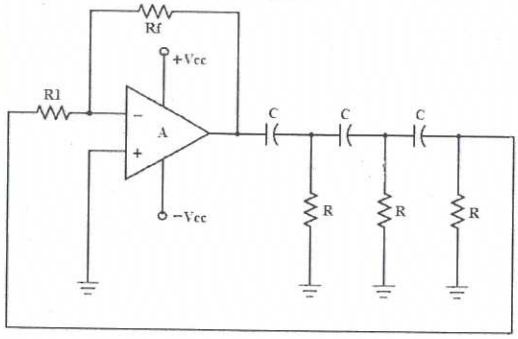
$$\text{then, } -Vout = \left[\frac{R_F}{Rin} V1 + \frac{R_F}{Rin} V2 + \frac{R_F}{Rin} V3\right]$$

If all the input impedances, (Rin) are equal in value, we can simplify the above equation to give an output voltage of:

Summing Amplifier Equation

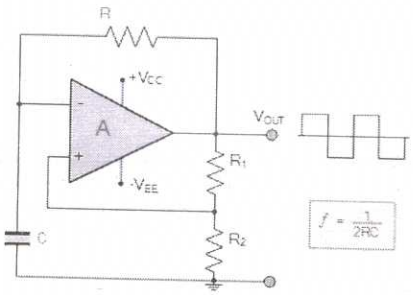
$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots etc\right)$$

This operational amplifier circuit that will amplify each individual

V.b	input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltages V_1, V_2 and V_3. A direct voltage addition can also be obtained when all the resistances are of equal value and Rf is equal to Rin. A current to voltage converter will produce a voltage proportional to the given current.  To analyse the current to voltage converter by inspection, if we apply KCL to the node at V- (the inverting input) and let the input current to the inverting input be I-, then Vout−V−Rf=Ip+I−(1)(1)Vout−V−Rf=Ip+I− since the output is connected to V- through R_f, the opamp is in a negative feedback configuration. Thus V−=V+=0 and assuming that I- is 0 and simplifying, Vout=IpRf	3 fig+4 exp	7	
VI.a	 This type of oscillator consists of an op-amp as amplifier stage and three RC cascaded networks as feedback circuit.This op-amp is operated in inverting mode and hence the output signal of the op-amp is shifted by 180 degrees to the input signal appeared at inverting terminal. And an additional 180 degrees phase shift is provided by the RC feedback network and hence the condition for obtaining the oscillations. The above circuit acts as an oscillator as	4 fig+ 4 exp	8	

the loop gain is greater than unity , if the op-amp provides the gain greater than 29.
The frequency of oscillations,
$1/(2\pi R C \sqrt{6})$
The condition of oscillations is given by $A \geq 29$.

VI.b



An astable oscillator circuit generates a rectangular output waveform using an RC timing network connected to the inverting input of the operational amplifier and a voltage divider network connected to the other non-inverting input.The astable multivibrator has two states, neither of which are stable as it is constantly switching between these two states with the time spent in each state controlled by the charging or discharging of the capacitor through a resistor.

In the op-amp multivibrator circuit the op-amp works as an analogue comparator. An op-amp comparator compares the voltages on its two inputs and gives a positive or negative output depending on whether the input is greater or less than some reference value.

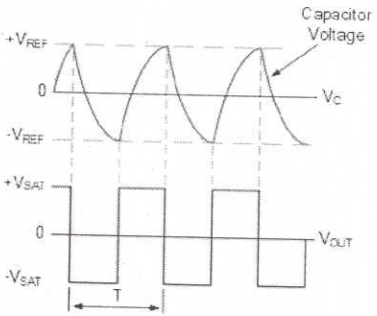
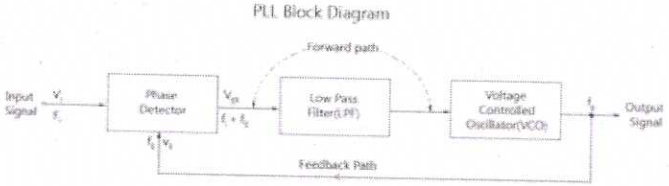


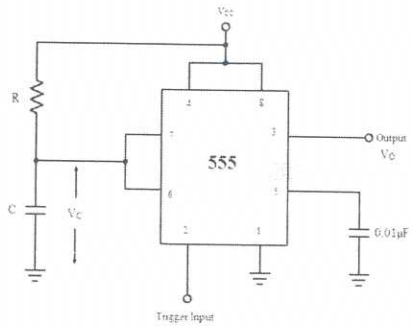
Fig3+ exp4

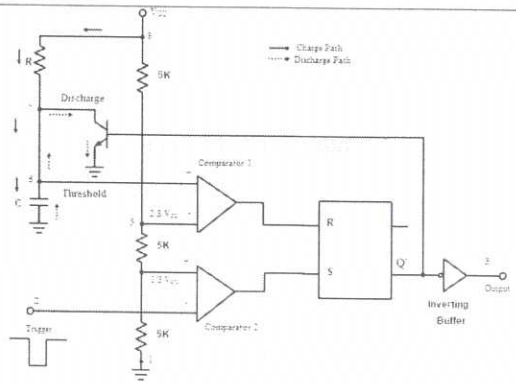
7

VII. a



The input signal Vi with an input frequency fi is passed through a phase detector. A phase detector basically a comparator which

	compares the input frequency fi with the feedback frequency fo .The phase detector provides an output error voltage Ver (=fi+fo),which is a DC voltage. This DC voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady DC level, Vf (=Fi-Fo). Vf also represents the dynamic characteristics of the PLL.The DC level is then passed on to a VCO. The output frequency of the VCO (fo) is directly proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals the input frequency. Thus the PLL works in these stages – free-running, capture and phase lock.As the name suggests, the free running stage refer to the stage when there is no input voltage applied. As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called the capture stage. The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency. This stage is called the phase locked state.	Fig3 +exp 4	7	
VII.b.	 A monostable multivibrator has only one stable state. The monostable mode is also called "one-shot" pulse generator. The sequence of events starts when a negative going trigger pulse is applied to the trigger comparator. When this trigger comparator senses the short negative going trigger pulse to be just below the reference voltage (1/3 VCC), the device triggers and the output goes HIGH.The discharge transistor is turned OFF and the capacitor C that is externally connected to its collector will start charging to the max value through the resistor R. The HIGH output pulse ends when the charge on the capacitor reaches 2/3 VCC. The internal connection of the IC 555 in monostable mode along with the RC timing circuit is shown below. Initially the flip-flop is RESET. This will allow the discharge transistor to go to saturation. The capacitor C, which is connected to the open collector (drain in case of CMOS) of the transistor, is provided with a discharge path. Hence the capacitor discharges completely and the voltage across it is 0. The output at pin 3 is low (0).	fig4+ exp4	8	



When a negative going trigger pulse input is applied to the trigger comparator (comparator 2), it is compared with a reference voltage of 1/3 VCC. The output remains low until the trigger input is greater than the reference voltage. The moment trigger voltage goes below 1/3 VCC, the output of comparator goes high and this will SET the flip-flop. Hence the output at pin 3 will become high.

At the same time, the discharge transistor is turned OFF and the capacitor C will begin to charge and the voltage across it rises exponentially. This is nothing but the threshold voltage at pin 6. This is given to the comparator 1 along with a reference voltage of 2/3 VCC. The output at pin 3 will remain HIGH until the voltage across the capacitor reaches 2/3 VCC.

The instance at which the threshold voltage (which is nothing but the voltage across the capacitor) becomes more than the reference voltage, the output of the comparator 1 goes high. This will RESET the flip-flop and hence the output at pin 3 will fall to low (logic 0) i.e. the output returns to its stable state. As the output is low, the discharge transistor is driven to saturation and the capacitor will completely discharge.

The output at pin 3 is low at start, when the trigger becomes less than 1/3 VCC the output at pin 3 goes high and when the threshold voltage is greater than 2/3 VCC the output becomes low until the occurrence of next trigger pulse. A rectangular pulse is produced at the output. The time for which the output stays high or the width of the rectangular pulse is controlled by the timing circuit i.e. the charging time of the capacitor which depends on the time constant RC.

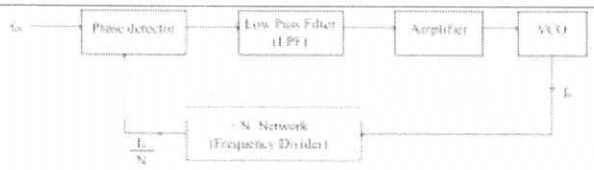
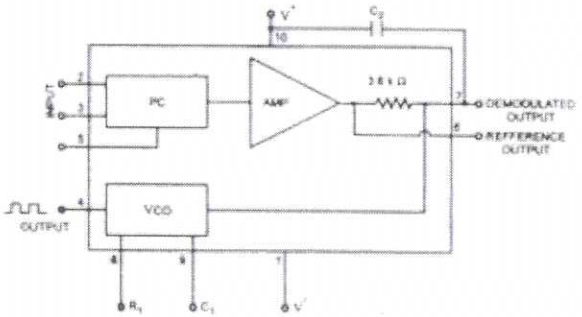
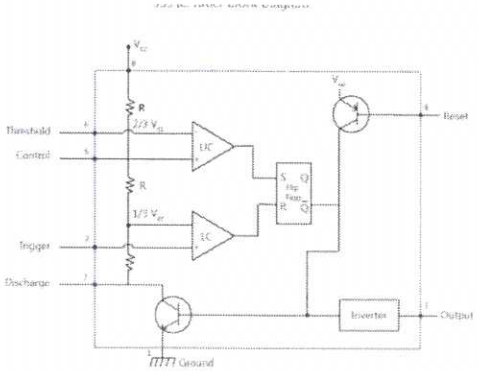
VIII. a

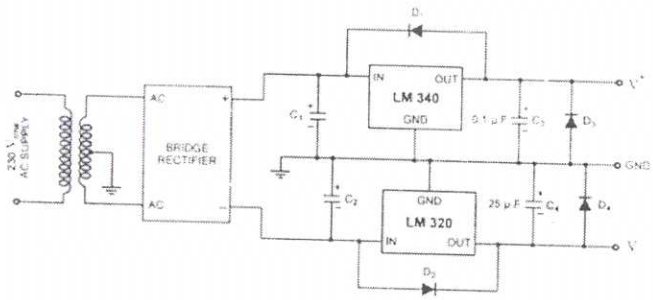
1) Frequency Divider

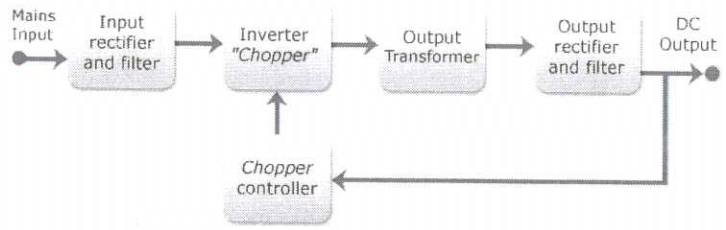
In this application, the loop is broken and a frequency divider network is inserted between VCO and phase detector as shown in figure below.

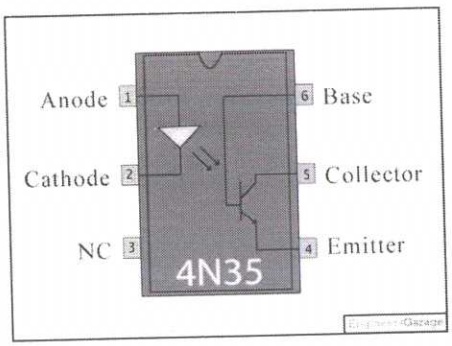
3.5+ 3.5

7

VIII.b.	 Since the output of frequency divider is locked to input frequency fin, the VCO is actually running at a multiple of the input frequency. The desired amount of multiplication can be obtained by selecting a proper ÷N network. ∴ Input to phase detector, fin=fo/N ∴ fo=Nfin 2) FM demodulation  *Block Diagram of PLL Unit 565 For Use As FM Detector* Frequency demodulation or detection can be obtained directly by using the PLL circuit. When the centre frequency of the PLL is selected or designed at the FM carrier frequency, the filtered or output voltage in the circuit shown in figure, is obviously the desired demodulated voltage, that varies in magnitude in proportion to the signal frequency.  The voltage divider consists of three identical 5k resistors which create two reference voltages at 1/3 and 2/3 of the supplied voltage, which can range from 5 to 15V. A comparator is a circuit element	Fig 4+exp 4	8	

IX.a.	that compares two analog input voltages at its positive (non-inverting) and negative (inverting) input terminal. If the input voltage at the positive terminal is higher than the input voltage at the negative terminal the comparator will output 1. Vice versa, if the voltage at the negative input terminal is higher than the voltage at the positive terminal, the comparator will output 0. The first comparator negative input terminal is connected to the 2/3 reference voltage at the voltage divider and the external "control" pin, while the positive input terminal to the external "Threshold" pin. On the other hand, the second comparator negative input terminal is connected to the "Trigger" pin, while the positive input terminal to the 1/3 reference voltage at the voltage divider. The flip-flop will output 1 when R is 0 and S is 1, and vice versa, it will output 0 when R is 1 and S is 0. The Q-bar output of the flip-flip goes to the output stage or the output drivers which can either source or sink a current of 200mA to the load. The output of the flip-flip is also connected to a transistor that connects the "Discharge" pin to ground.  *Simple Dual Power Supply* Opposite-phase ac is provided by the transformer's secondary and a grounded center tap. The single full-wave bridge converts these into positive and negative dc voltages. The output of the rectifier circuit is filtered with the help of capacitors C1 and C2.While the LM 340 provides regulation of the positive voltage, the LM 320 regulates the negative voltage.The diodes in the LM circuit are used to provide protection. They ensure that the transient voltages on the regulator outputs do not drive the outputs to a potential above their inputs and cause damage to to the regulators. The diodes also play an important role	4+4	8	

	in turning on the two regulators simultaneously. If there is a chance of such happening, the output of the slower regulator may be driven toward the potential of the faster one. Thus, the diodes prevent these reverse polarities on start up.			
IX.b.				
	Input rectifier stage If the SMPS has an AC input, then the first stage is to convert the input to DC. This is called **Inverter stage** The inverter stage converts DC to AC by running it through a power oscillator. **Voltage converter and output rectifier** If the output is required to be isolated from the input, as is usually the case in mains power supplies, the inverted AC is used to drive the primary winding of a high-frequency transformer. This converts the voltage up or down to the required output level on its secondary winding. The output transformer in the block diagram serves this purpose. If a **DC** output is required, the **AC** output from the transformer is rectified. The rectified output is then smoothed by a filter consisting of inductors and capacitors. **Regulation** A feedback circuit monitors the output voltage and compares it with a reference voltage, as shown in the block diagram above. Depending on design and safety requirements, the controller may contain an isolation mechanism (such as an opto-coupler) to isolate it from the DC output. Switching supplies in computers,. The feedback circuit needs power to run before it can generate power, so an additional non-switching power-supply for stand-by is added	Fig4+ exp 3	7	
X.a.	o It has small in size and lower in cost. o It operates in positive or negative supply operation. o It has choice of supply voltage. o Wide variety of applications such as series, shunt, switching	Any 7	7	

	and floating regulators. o Relative simplicity with power supply can be designed. o Low standby current gain. o Very low temperature drift and high ripple rejection. o Built in fold back current limiting. o Input voltage is maximum 40 V. o Output voltage adjustable from 2 V to 37 V. o Output current upto 150 mA without external pass transistor. o Load and line regulations of 0.03%.			
X.b.	 Current from the source signal passes through the input LED which emits an infra-red light whose intensity is proportional to the electrical signal. This emitted light falls upon the base of the photo-transistor, causing it to switch-ON and conduct in a similar way to a normal bipolar transistor. The base connection of the photo-transistor can be left open (unconnected) for maximum sensitivity to the LEDs infra-red light energy or connected to ground via a suitable external high value resistor to control the switching sensitivity making it more stable and resistant to false triggering by external electrical noise or voltage transients. When the current flowing through the LED is interrupted, the infra-red emitted light is cut-off, causing the photo-transistor to cease conducting. The photo-transistor can be used to switch current in the output circuit.	4+4	8	