LINEAR INTEGRATED CIRCUITS

PART A TED(15)4042

I (1) The small input voltage required at the input terminals of an OPAMP to make output zero is called input offset voltage.

(2) (i) provides gain and frequency adjustment flexibility.
(ii) It does not cause loading of the source or load.
(iii) Size and weight is reduced.
(iv) design procedure is simple.
(v) response is very much improved
(any two)

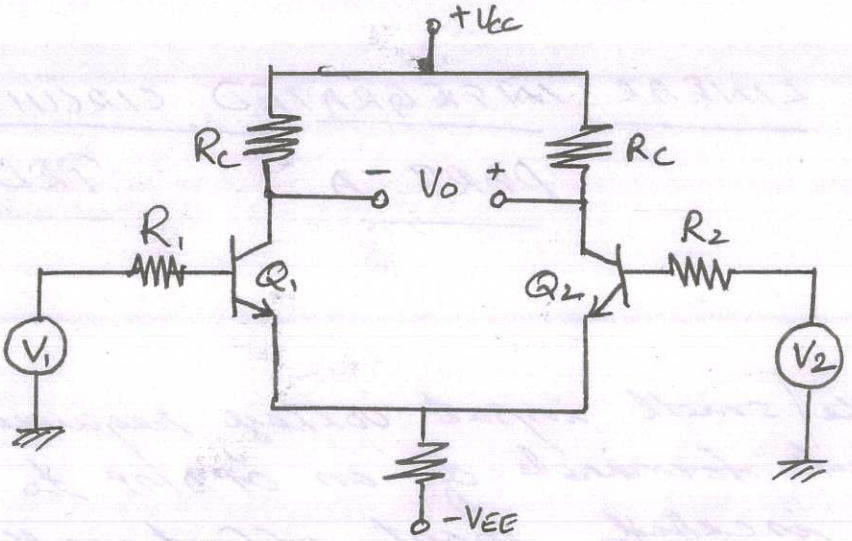
(3) The total time taken by the PLL to establish lock is called pull-in time.

(4) (i) frequency devider (ii) pulse generator
(iii) Linear saw tooth generator
(iv) Square wave generator
(v) Temparature Controller
(vi) pulse detector (any two)

(5) fixed positive 78XX
fixed Negative 79XX

Part B

11 (1)



(3)

- Two identical bipolar junction transistors Q_1 and Q_2 with emitters are coupled together. The collectors of transistors are connected through resistors R_C to the $+V_{CC}$.
- It can be arranged in the following configuration

Dual input balanced output
Dual input unbalanced output
Single input balanced output
Single input unbalanced out put

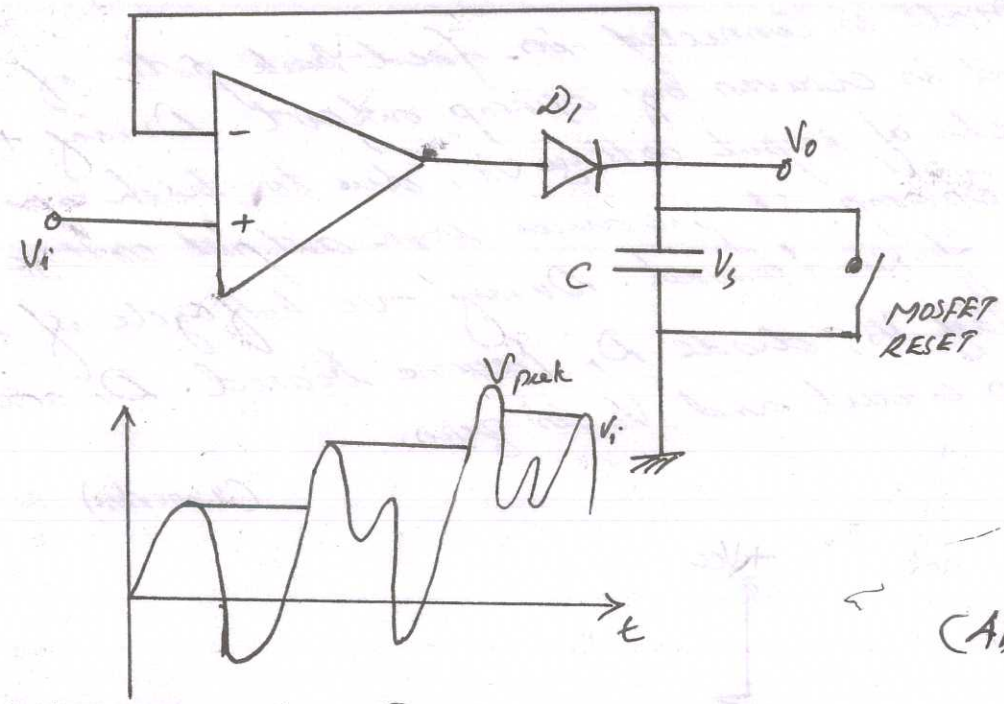
(3)

$$V_{out} = A(V_1 - V_2)$$

V_1 and V_2 are two inputs and V_{out} is the voltage between two collectors.

(2) (1) Infinite voltage gain
(2) Infinite input impedance
(3) Zero output impedance
(4) Zero offset voltage
(5) Infinite Bandwidth
(6) Infinite CMRR
(7) Infinite slew rate
(8) Zero offset current.
(9) Zero input noise (any six)

(3)



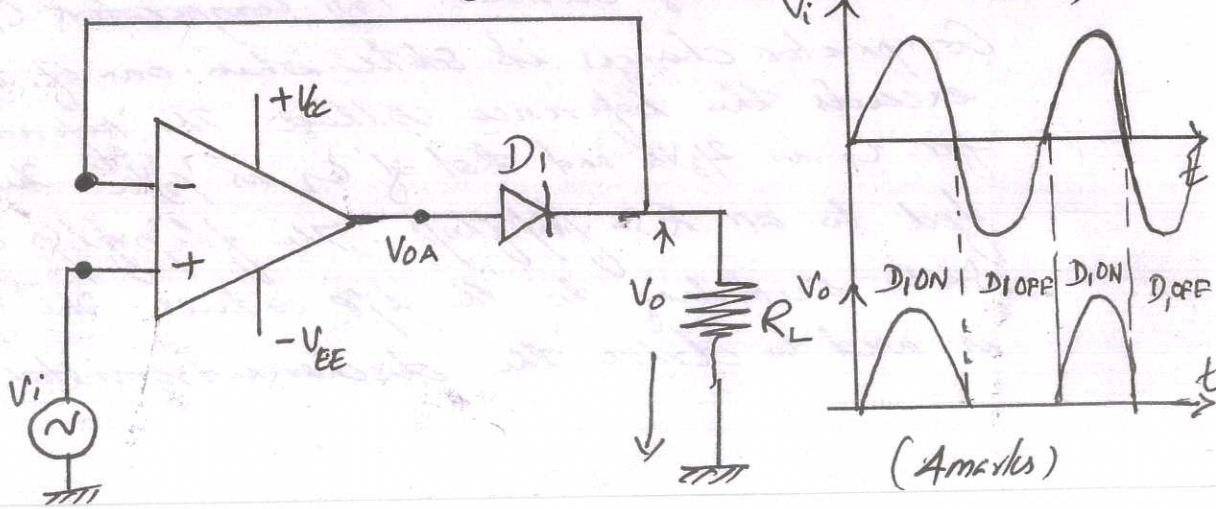
(4 marks)

The circuit follows the voltage peaks of a signal and stores the highest value of capacitor voltage. If a higher peaks signal comes along, this new value gets stored in capacitor. The highest value is stored until the capacitor is discharged.

Assume the capacitor is initially charged up to Vc. When Vin exceeds Vc the diode gets forward biased and circuit behaves as a voltage follower circuit. The o/p voltage Vo follows Vi as long as Vi exceeds Vc. When Vi drops below Vc, the diode becomes reverse biased and the capacitor holds the charge till input voltage again attains a value greater than Vc.

(2 marks)

(4)

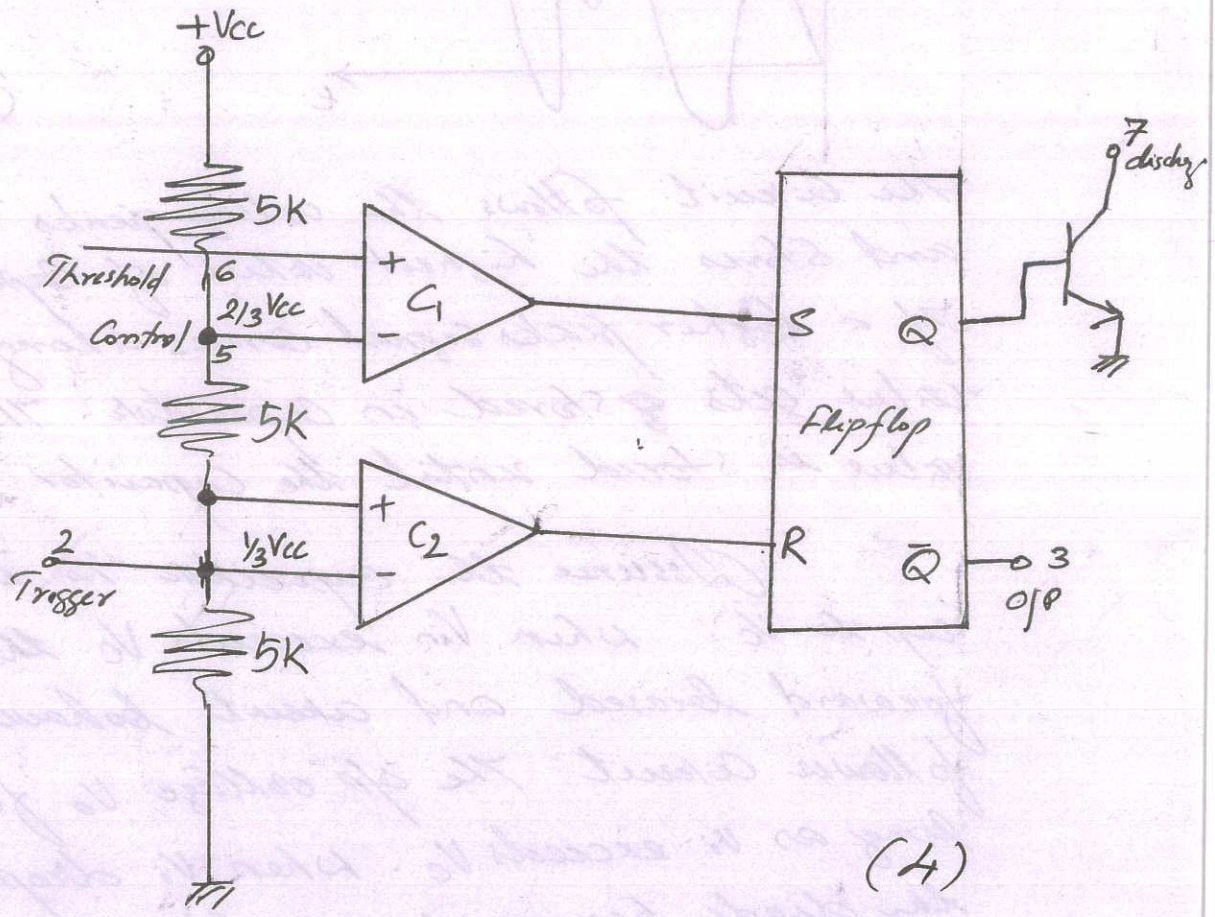


(4 marks)

Diode is connected in feed back path of opamp and is driven by opamp output. During +ve half cycle of input voltage V_i, due to high open loop gain of opamp, it produces high output voltage and hence D_1 forward biased. During -ve half cycle of input voltage V_i, diode D_1 reverse biased. D_1 acts as an open circuit and V_o is zero.

(2 marks)

(5)

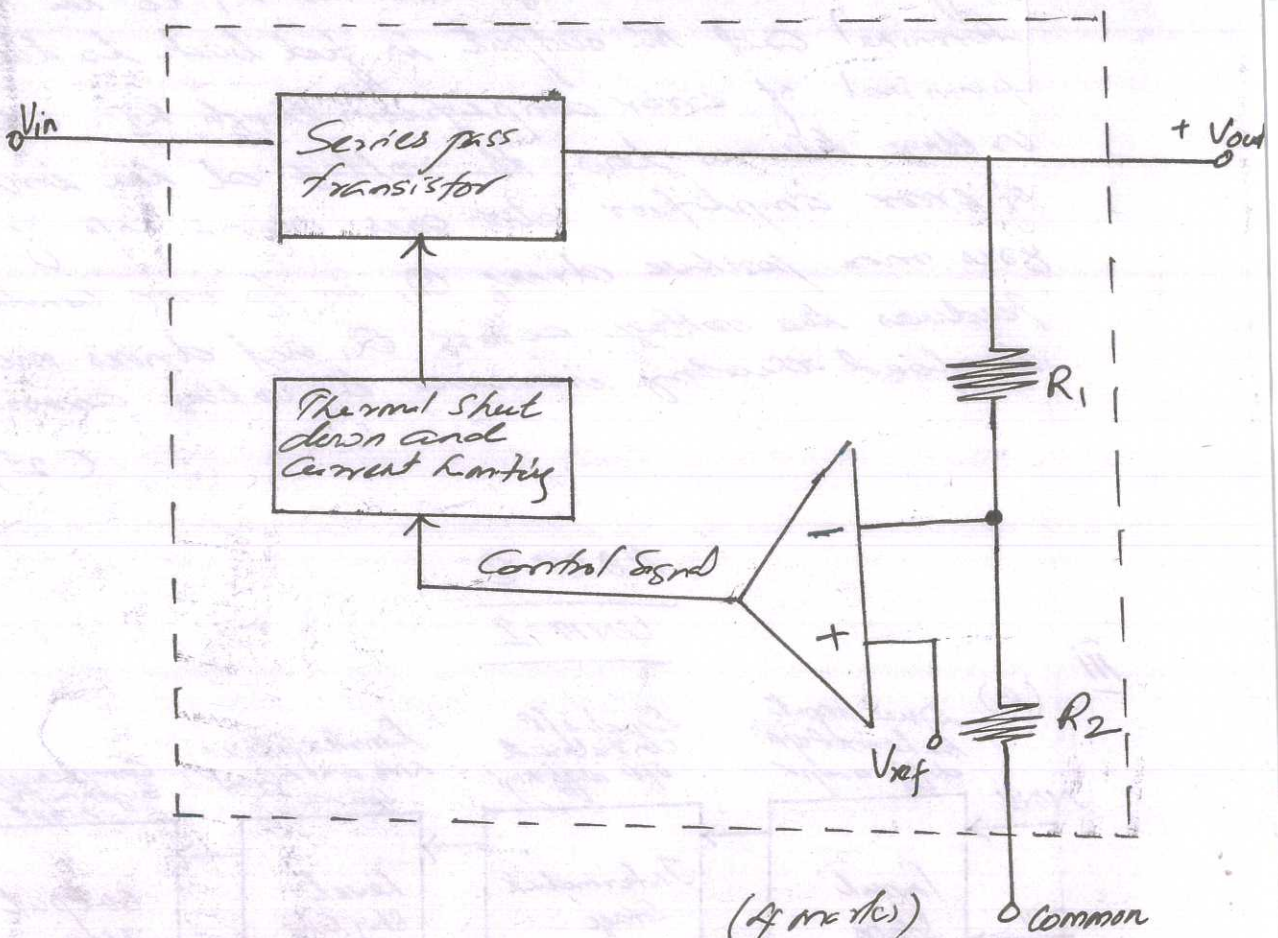


(4)

The functional Block diagram of IC 555 is shown in the figure. Three equal resistor 5K each serves as internal voltage devider. Two comparators C_1 and C_2. Comparator changes its state when one of its inputs exceeds the reference voltage. The reference voltage for C_1 is $\frac{2}{3}V_{cc}$ and that of C_2 is $\frac{1}{3}V_{cc}$. The o/p is fed to an RS flipflop. The flipflop changes its state according to the i/p values. The o/p of flipflop is used to drive the discharge transistor.

(2)

(6)

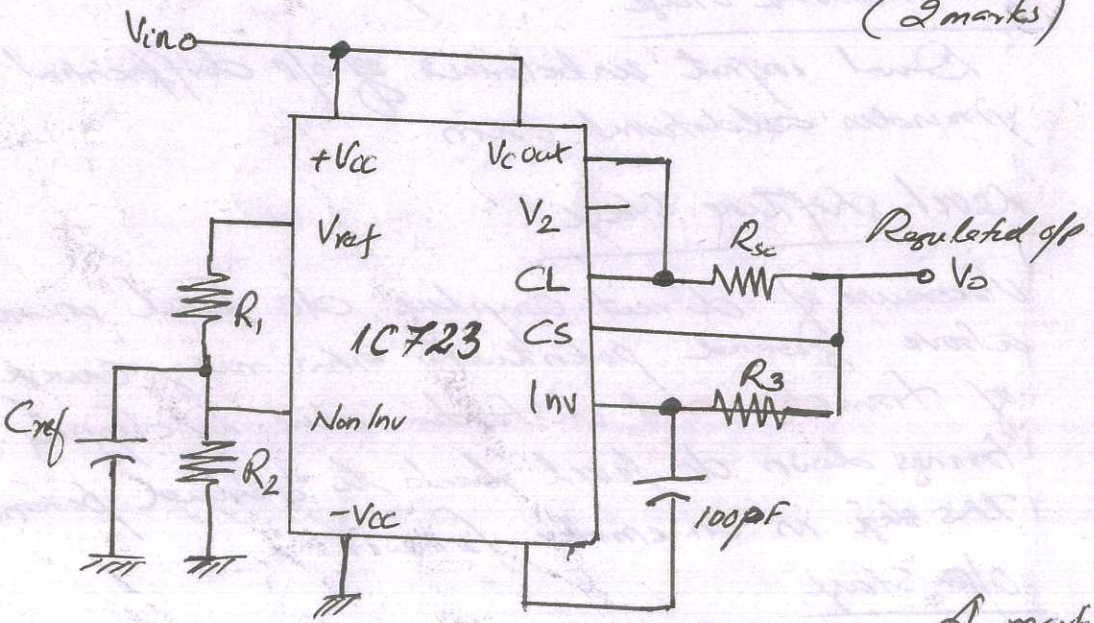


(4 marks)

The figure shows the functional block diagram of 3 terminal IC voltage regulator. A part of o/p voltage is taken through a potential decider formed by R_1 and R_2. This voltage is compared with internally generated reference voltage. Generated control signal is applied to the series pass ~~trans~~ transistor through a protective circuit. It regulates varies as required for maintaining the o/p voltage constant.

(2 marks)

(7)



4 marks

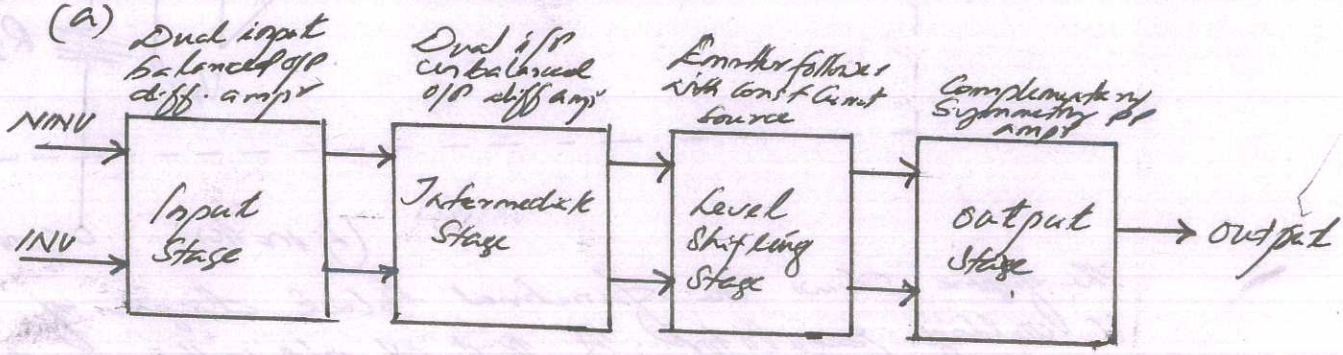
V_{ref} is connected through resistor R_1 to the non-inverting terminal and the output is fed back to the inverting terminal of error amplifier through R_3. When the o/p voltage becomes low, the voltage at the inverting terminal of error amplifier also goes down. o/p of error amplr goes more positive driving Q_1 in to more conduction. This reduces the voltage across Q_1 and drives more current to load thereby increases the voltage across the load.

(2)

PART C

UNIT I

III (a)



I/P Stage

(5marks)

Dual i/p balanced output diff. amplr. amplifies difference between two input signals. This stage provides most of the voltage gain for the amplr and provides high i/p resistance.

Intermediate Stage

Dual input unbalanced o/p differential amplr. provides additional gain.

Level shifting Stage

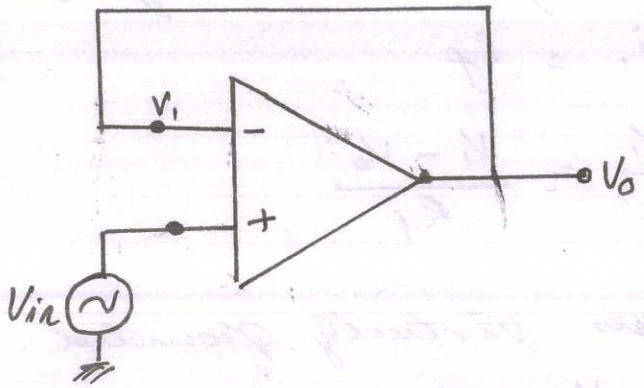
Because of direct coupling, dc level increases well above ground potential. This may cause saturation of transistors and distortion due to clipping. This stage brings down dc level back to ground potential. Usually this stage is an emitter follower.

O/p Stage

PP complementary Symmetry amplr. increases o/p voltage swing and current supplying capability of amplr (5marks)

(7)

(6)



(3)

The configuration of OPAMP as voltage follower is shown in figure. O/P is fed back to the i/p by directly connecting the inverting i/p terminal to o/p. i/p is directly applied to NINV terminal.

$$V_{out} = V_{in}.$$

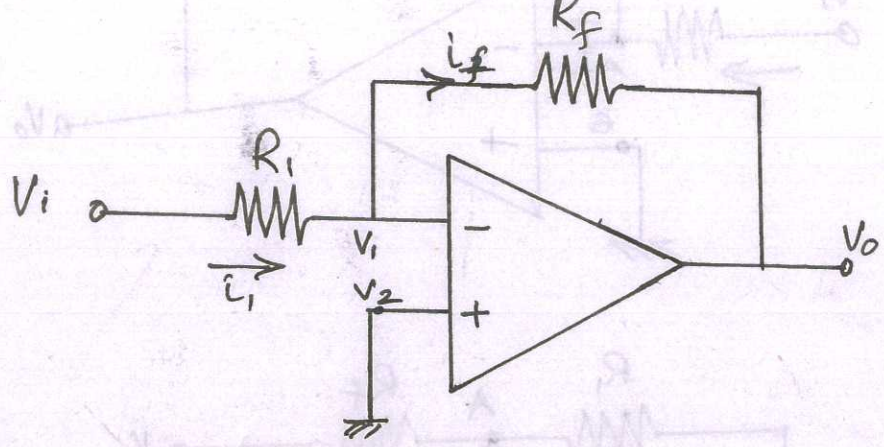
The o/p follows input and hence the name voltage follower. The ckt provides low o/p impedance and high i/p impedance and can be used as a buffer amplifier.

(2)

OR.

IV

(A)



(3)

figure shows opamp as inverting amplifier. O/P is fed back to the input through a resistor R_f. Input is applied to the inverting terminal through input resistor R_1 and the non-inverting terminal is grounded.

(2)

$$i_1 = \frac{V_i - V_1}{R_1}$$

$$i_f = \frac{V_1 - V_o}{R_f}$$

(6)

Since input impedance is very high.

$$i_1 = i_f$$

ie $$\frac{V_i - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

Since V_1 is virtually grounded.

$$V_1 = V_2 = 0$$

ie $$\frac{V_i}{R_1} = \frac{-V_o}{R_f}.$$

ie $$V_o = -\left(\frac{R_f}{R_1}\right) V_i \quad ; \quad V_o \propto -V_i$$

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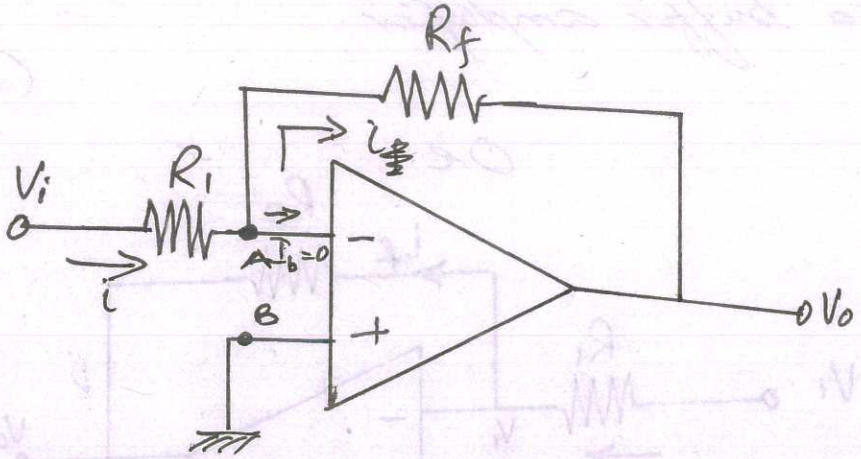
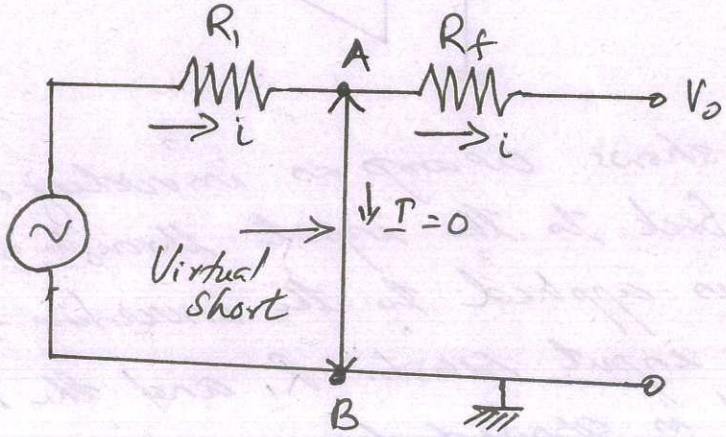
where $\frac{R_f}{R_1}$ is the gain of the amplifier

(3)

(b)



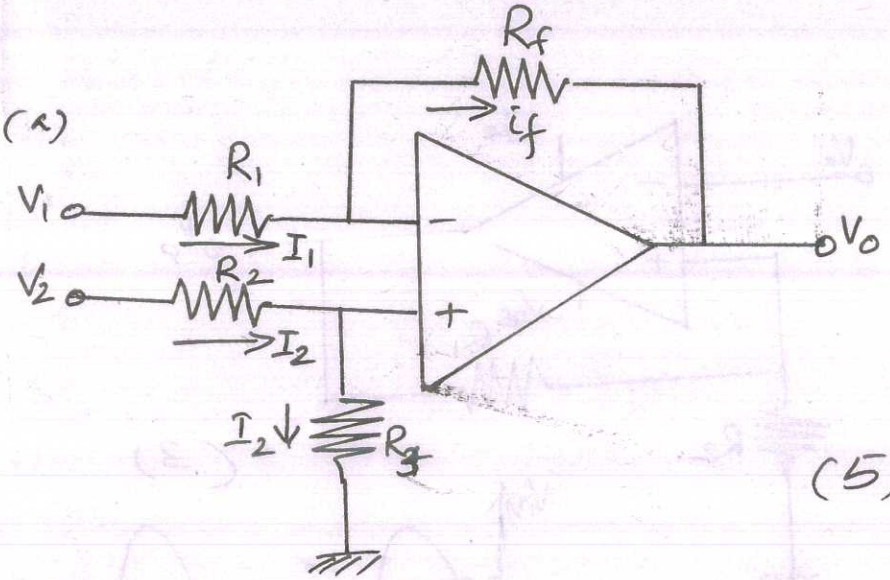


(5)

Explanation (2)

UNIT II (4)

V (a)



(5)

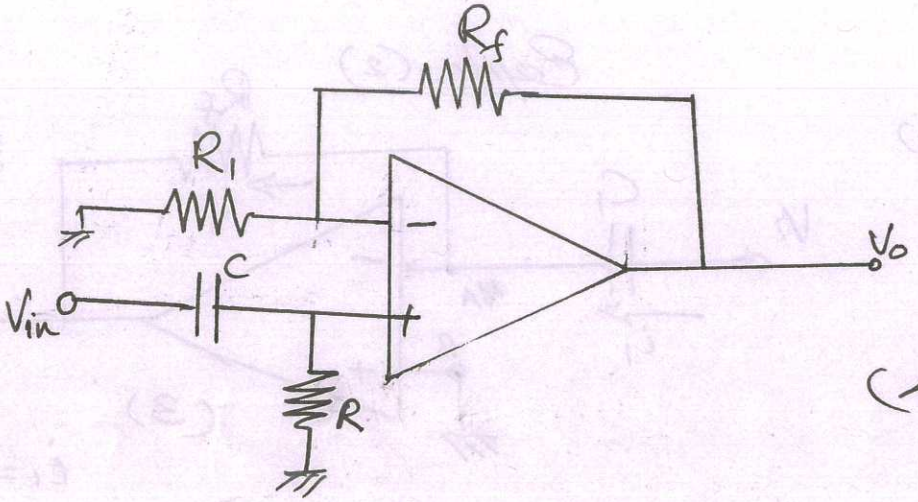
A OPAMP can be used as subtractor is shown in fig. The inputs are applied to two inputs.
$R_1 = R_2 = R_3 = R_f$ ∴ gain is unity

$$V_o = -\left(\frac{R_f}{R_1}\right)(V_2 - V_1)$$

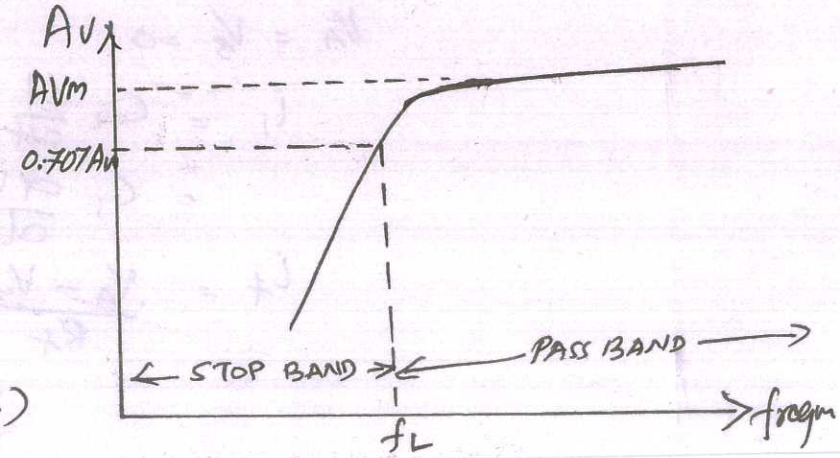
$$= V_2 - V_1$$

(3)

(b)



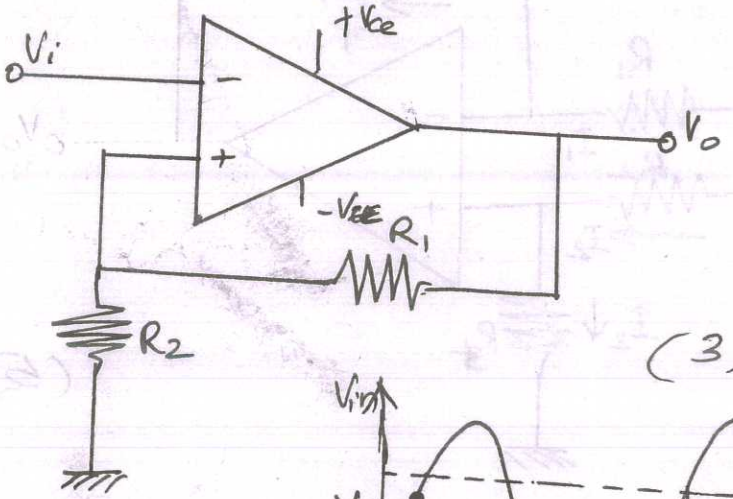
(4)



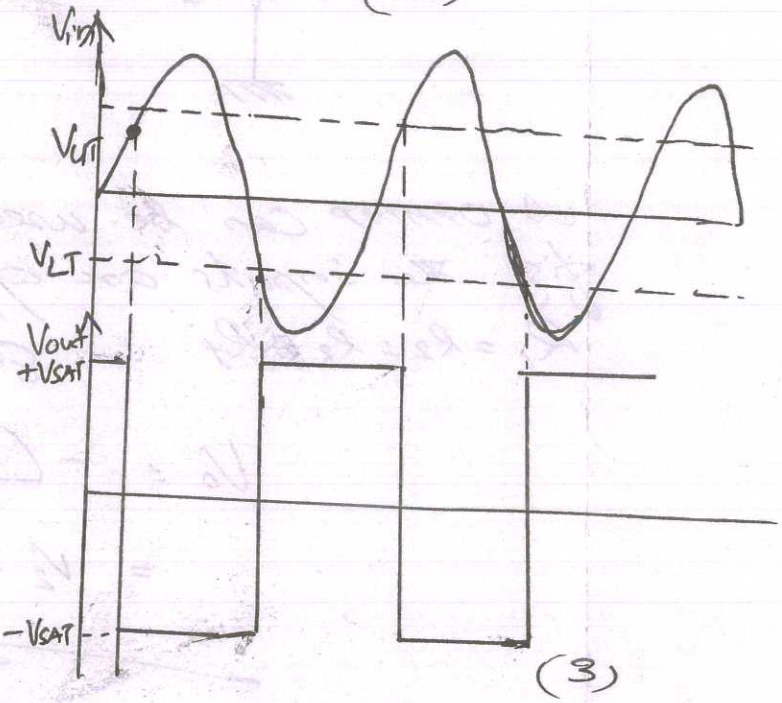
(3)

OR (10)

VI (A)



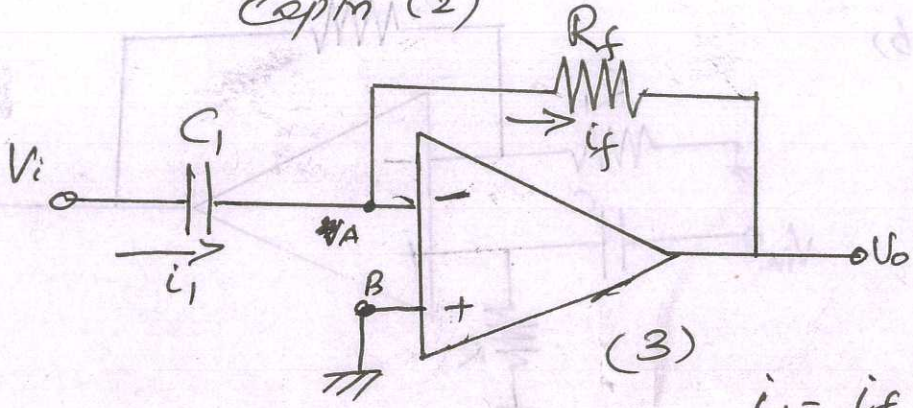
(3)



(3)

Eqn (2)

(b)



(3)

$i_1 = i_f$

$V_A = V_B = 0$

$i_1 = C_1 \frac{d}{dt}(V_i - V_A)$

$= C_1 \frac{dV_i}{dt}$

$i_f = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f}$

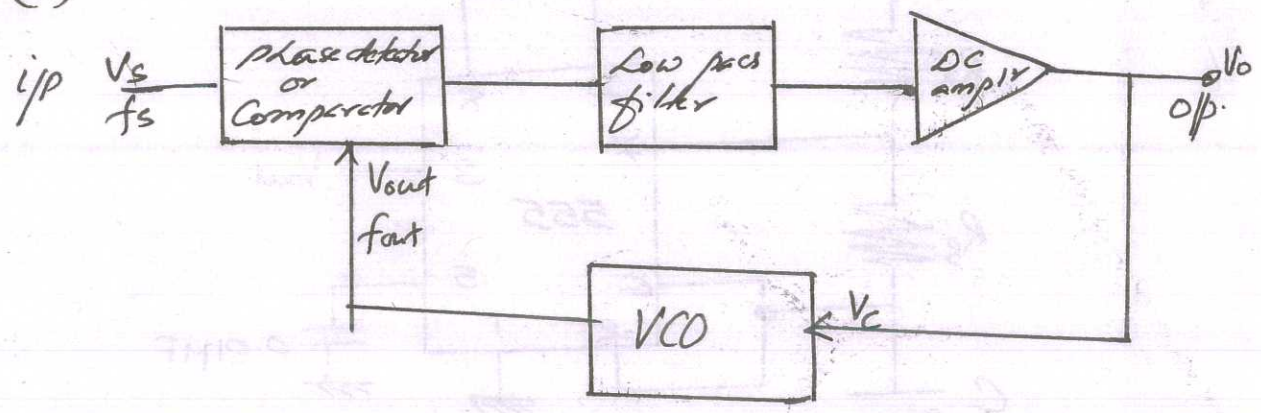
$-\frac{V_o}{R_f} = C_1 \frac{d}{dt} V_i$

$V_o = -R_f C_1 \frac{d}{dt} V_i$

(4)

UNIT III

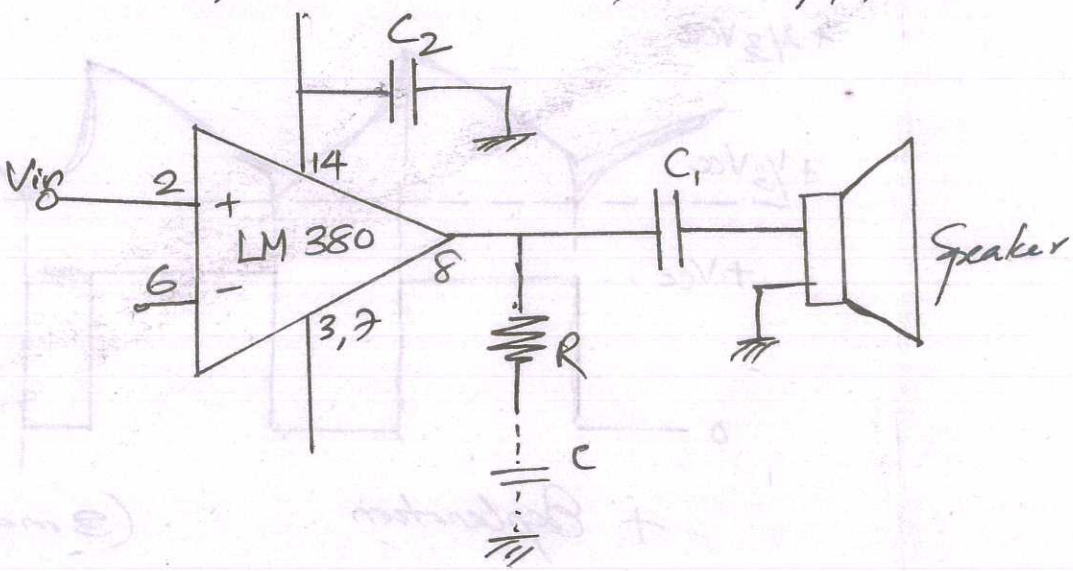
VII (a)



(4)

Explanation (4) 4+4 = 8

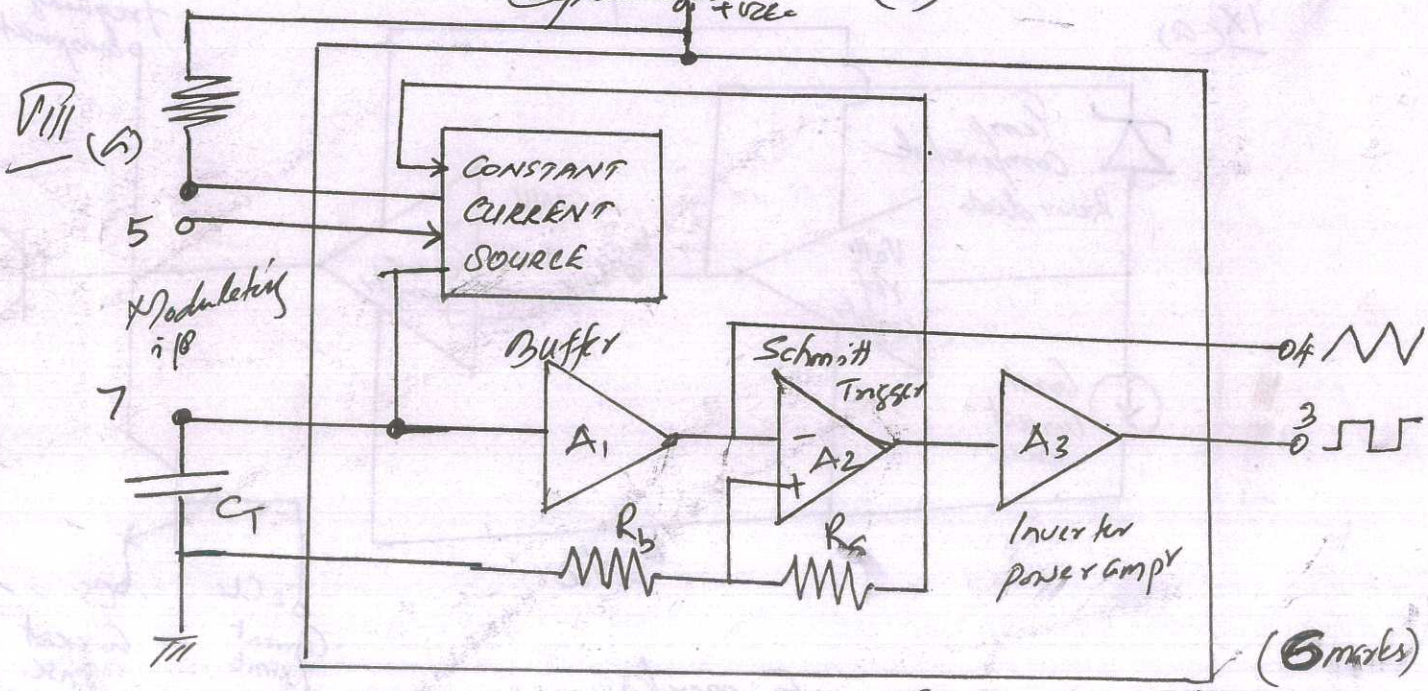
(b)



(4)

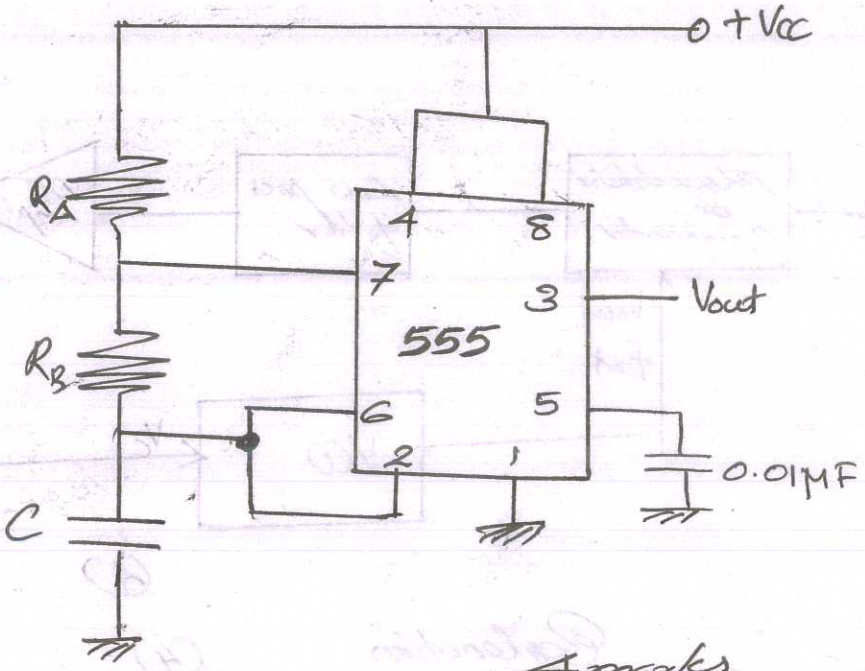
Explanation (3)

VIII (a)

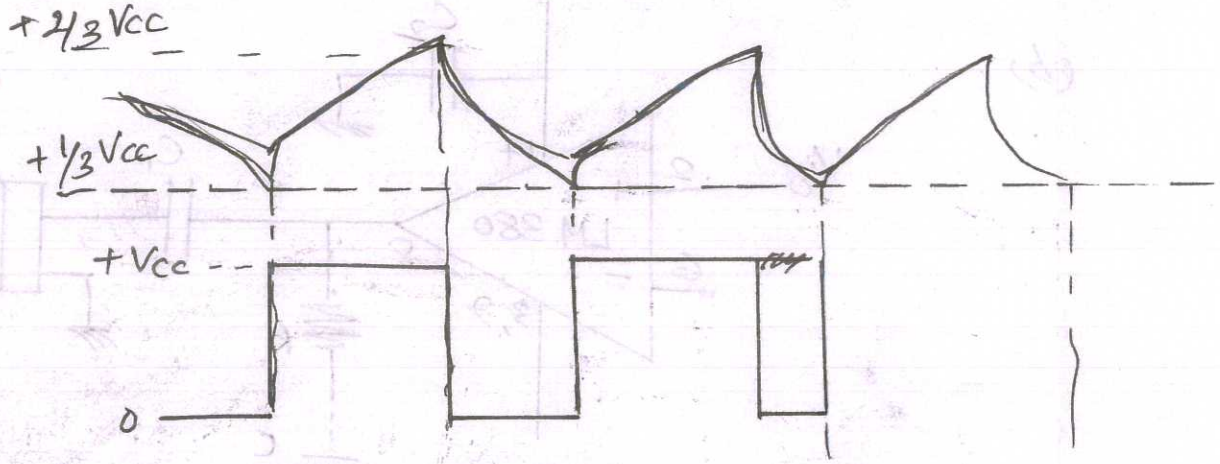


Explanation (~~4 marks~~ 4 marks)

(b)



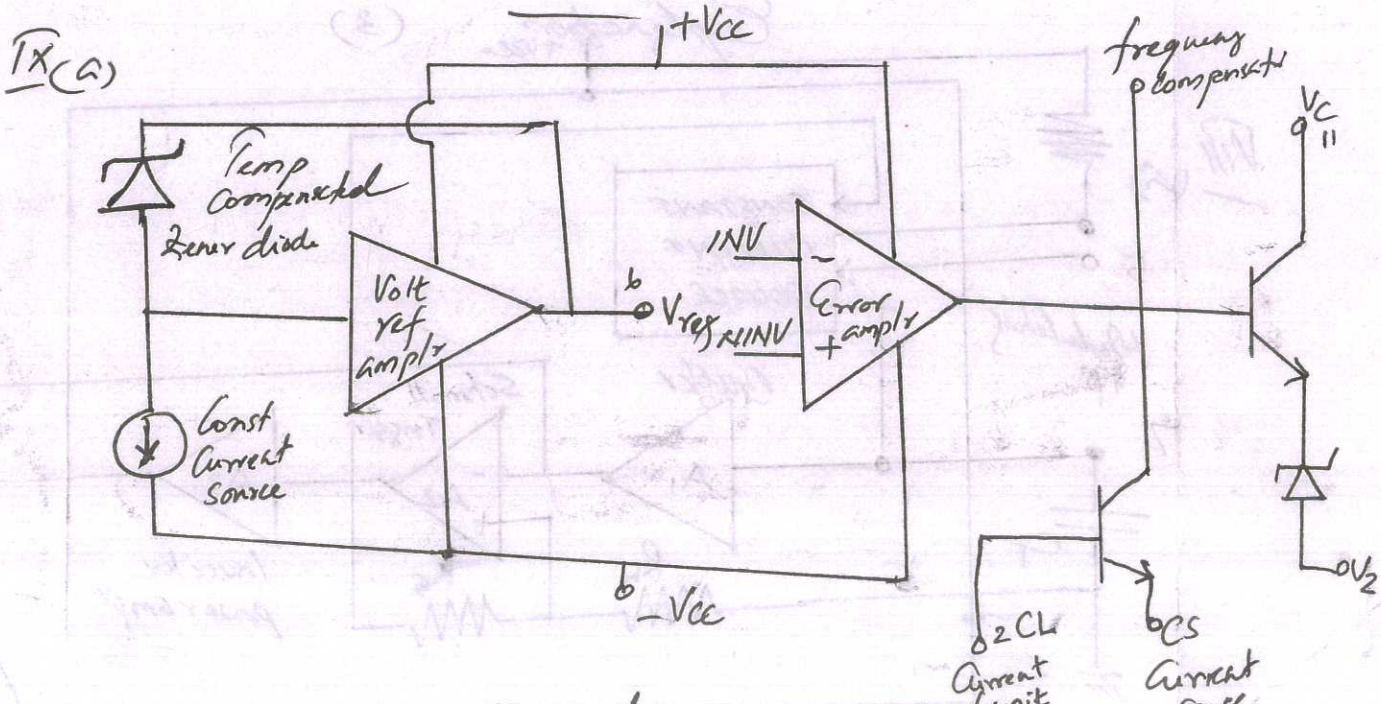
4 marks



+ Explanation (3 marks)

UNIT IV

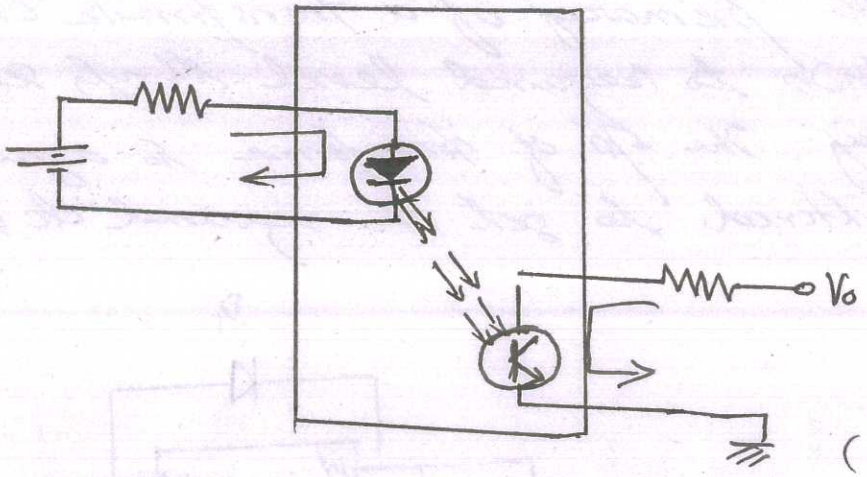
IX (a)



5 marks.

+ Explanation 3 marks.

(b)



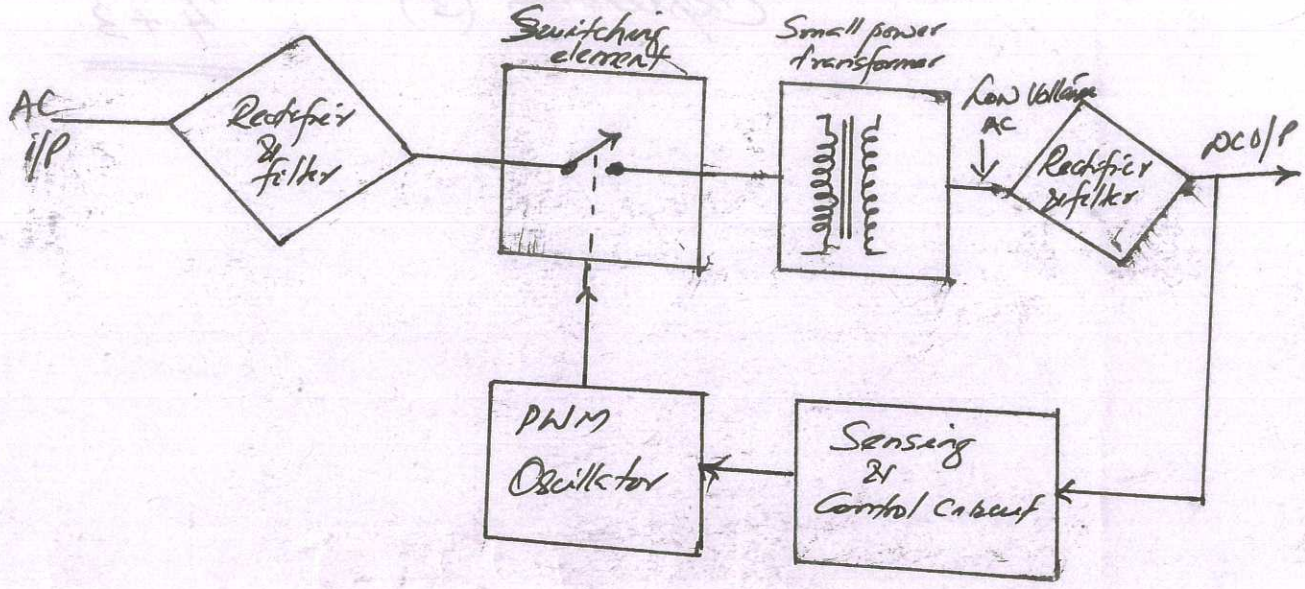
(3)

It consist of a photo emissive device such as LED and a photo detector like photo transistor, photodiode etc. Current through LED produces light and is incident on phot transistor. due to this a current in set up. Thus IC opto coupler couples two circuits and provides excellent isolation.

(2)

OR

X (a)



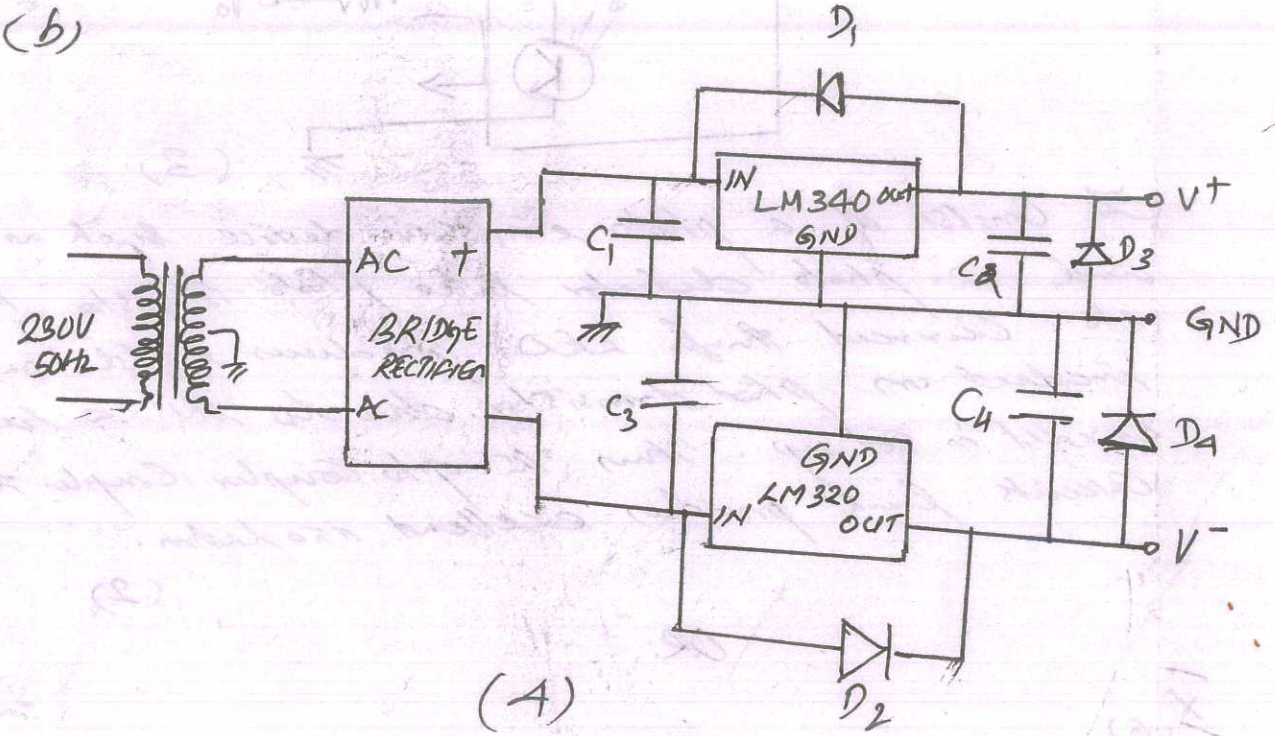
(5 marks)

Explanation (3 marks) 5+3

Used in computers, telephone exchanges, television receivers. The unregulated DC input voltage is rectified and filtered. This unregulated voltage is then chopped at a high frequency. The resultant high frequency pulse is applied

to the primary of a transformer and then step down to required level through secondary winding. The o/p of transformer is again rectified and filtered to get the required dc voltage.

(b)



(4)

Explanation (3) 4+3