SCHEME OF VALUATION
(Scoring Indicators)

Revision: 2015 Course Code: 4042
Course Title LINEAR INTEGRATED CIRCUITS

Qst No	Scoring Indicator	Split Up score	Total
I 1.	Flat package, Dual-in-line package, Metal can or Transistor package		
2.	High input impedance, High common mode rejection, Differential input, single ended output, High gain etc.		
3.	The total time taken by PLL to establish lock.		
*	$T = 2RC \log \frac{1+\beta}{1-\beta}$ where β is the feedback factor		
4.	$T = 0.69 (R_A + 2R_B) C$		
5.	Change in output voltage per a change in load current		
II 1.	Infinite input impedance Zero output impedance Infinite voltage gain Infinite bandwidth Zero offset and drift Infinite common mode rejection Infinite slew rate	6	

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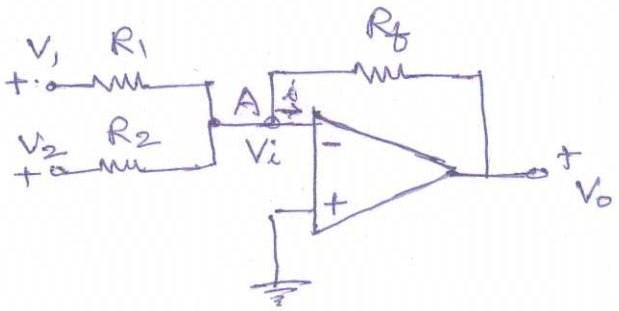
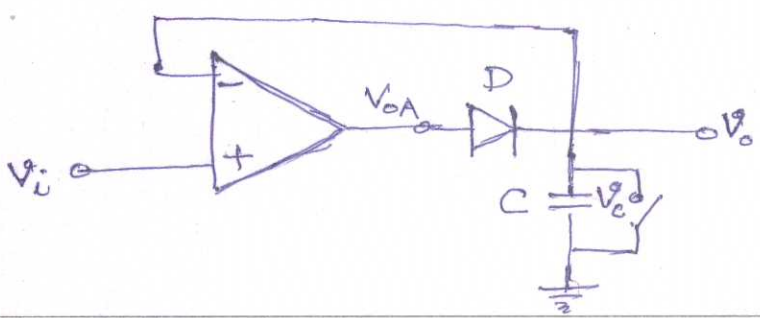
2.	The inverting input terminal of an operational amplifier is referred to as virtual ground. The input terminal ~~of~~ voltage of an inverting amplifier with non-inverting input connected to ground, is always zero, because of an apparent short circuit between the two, even though no current flows between them.	6	
3.	Applying KCL at node A $\frac{V_1 - V_i}{R_1} + \frac{V_2 - V_i}{R_2} = \frac{V_i - V_o}{R_f}$  $V_i = 0$ and $i = 0$ $\Rightarrow V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2\right]$ If $R_1 = R_2 = R$, $V_o = -(V_1 + V_2)$	6	
4.	 		

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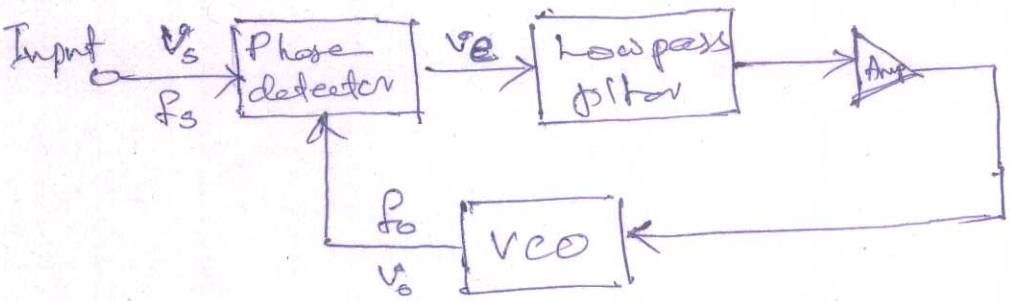
	When V_i exceeds V_c, D is forward biased and the circuit acts as voltage follower. When V_i drops below V_c D becomes reverse biased the C holds the charge till input voltage again attains a value greater than V_c. The capacitor voltage can be made zero by connecting an active switch across the capacitor	6	
5.			
	The phase detector compares the phase and frequency of the incoming signal to that of the output of VCO. If the two signals differ in frequency and/or phase an error voltage V_e is generated. The phase detector produces the sum and difference components f_s+f_o and f_s-f_o	6	

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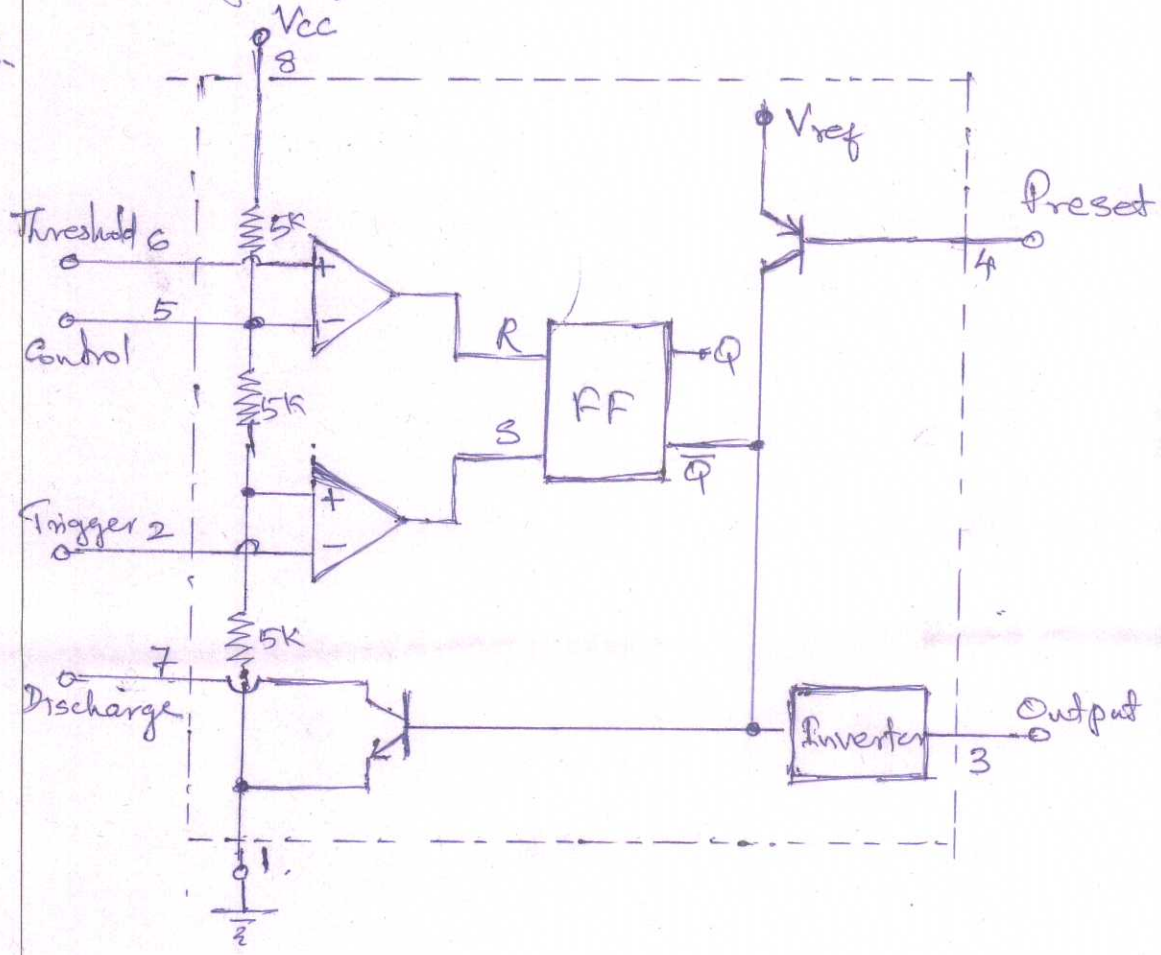
	at its output. The high frequency component f_s+f_o is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage V_c to counterbalance the change in frequency of VCO to reduce the frequency difference between f_s and f_o.		
6.		6	

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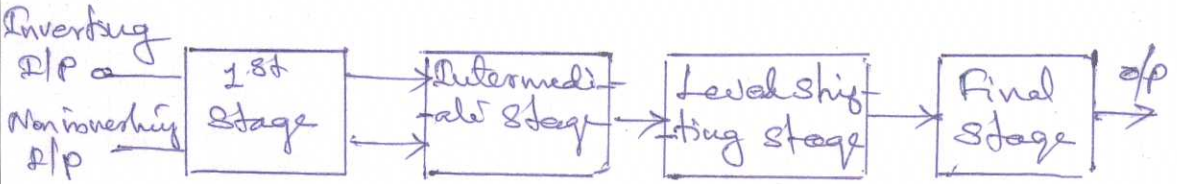
7 i)	Since they rely on switching (i.e ON-OFF) for its operation efficiencies ranging from 65 to 85 percent are typical compared to 30 to 45 percent for linear supplies.		
ii)	Because of higher switching rate the power transformer, inductor and filter capacitors are much smaller and lighter.	6	
iii	It can operate under low ac input voltage. Also since more energy can be stored in input filter capacitors long hold up period is available		
iii a)		3	
	1st stage is basically a dual input balanced output Differential amplifier which provides most of the voltage gains II stage is also dual input but unbalanced output Differential ampr. Third stage is basically emitter follower	6	

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	which keeps the dc level down to zero.		
	The final stage is basically class-B ~~push-pull~~ complementary symmetry amplifier and increases the current supplying capability of the amplifier		
b. i	Input Offset voltage : Voltage that must be applied between the input terminals to nullify the output		
ii	Input Offset Current : The algebraic difference b/w the currents into the − input and + input.		
iii	Input Bias current : The average of the current entering into the two input terminals.		
iv	Input resistance : The differential input resistance with one of the input terminals grounded.	6	
v	Input Capacitance : measured similar to the above		
vi	CMRR : Sensitivity to a difference signal as compared to a common mode signal		
vii	Slew rate : Max. rate of change of o/p voltage caused by a step input voltage		

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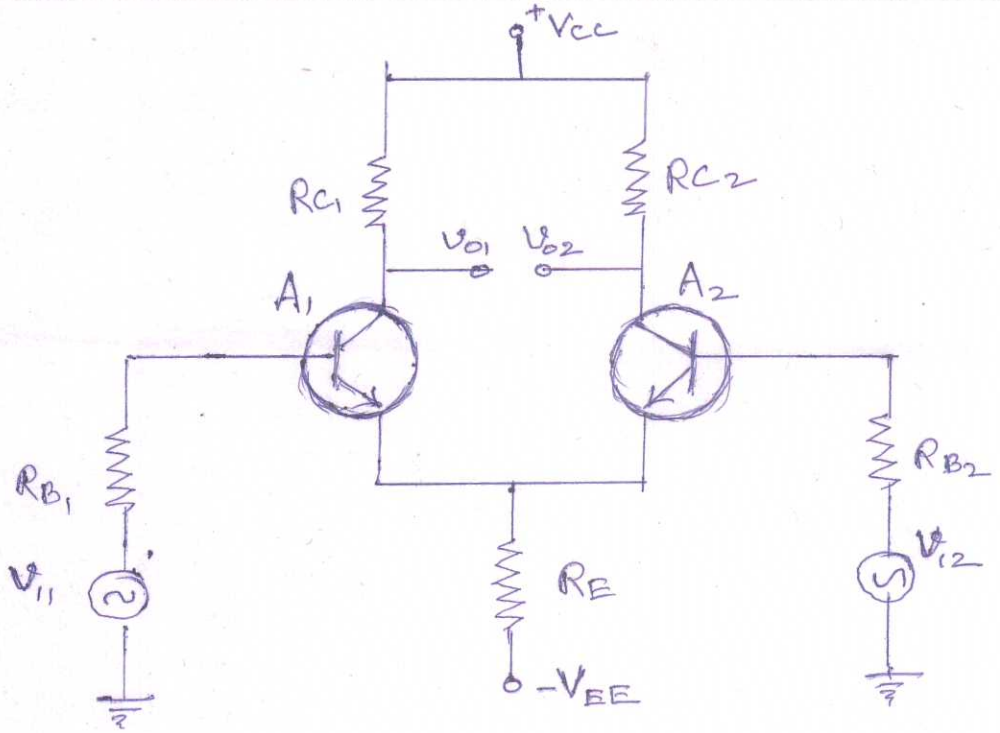
IV a



$V_{o1} = A_1 V_{11}$; $V_{o2} = A_2 V_{12}$

9

The differential o/p voltage of DA, V_o is given by $V_o = V_{o1} \sim V_{o2} = A_1 V_{11} - A_2 V_{12}$ (say)

If $A_1 = A_2 = A$ $V_o = A(V_{11} - V_{12})$

(The ckt can also be drawn with proper biasing using resistive n/w with emitters connected to ground through R_E)

A description of the ckt is necessary

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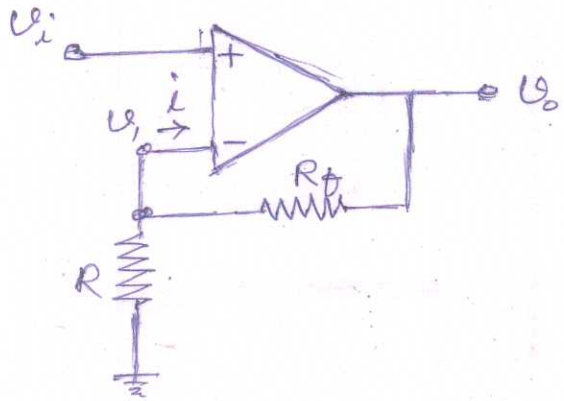
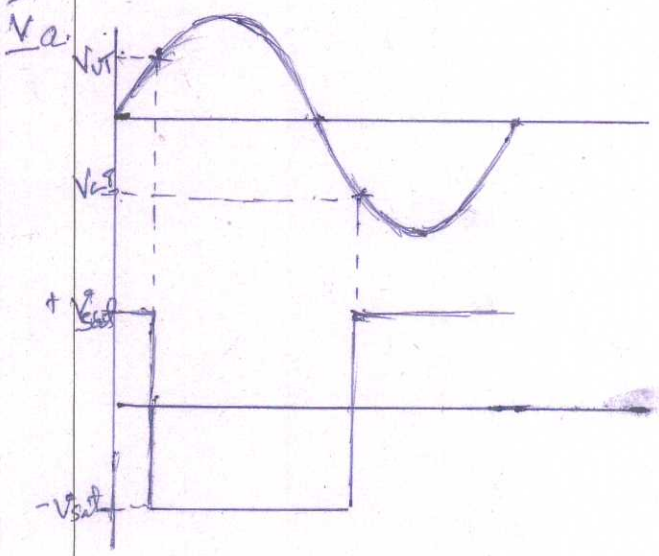
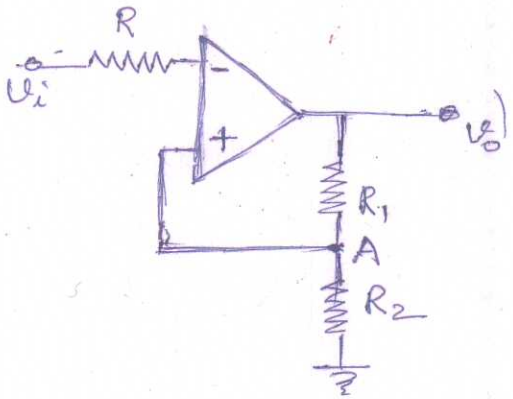
b.	$v_1 = v_i$ and $i = 0$ $\frac{v_1}{R} + \frac{v_1 - v_o}{R_f} = 0$ $\Rightarrow \frac{v_o}{v_1} = 1 + \frac{R_f}{R}$ 	6	
a.	 	6	9
	Voltage at $A = v_o \times \frac{R_2}{R_1 + R_2} = \beta v_o$.	3	
	when $v_i > \beta v_o$ $v_o = -v_{sat}$ when $v_i < \beta v_o$ $v_o = +v_{sat}$		

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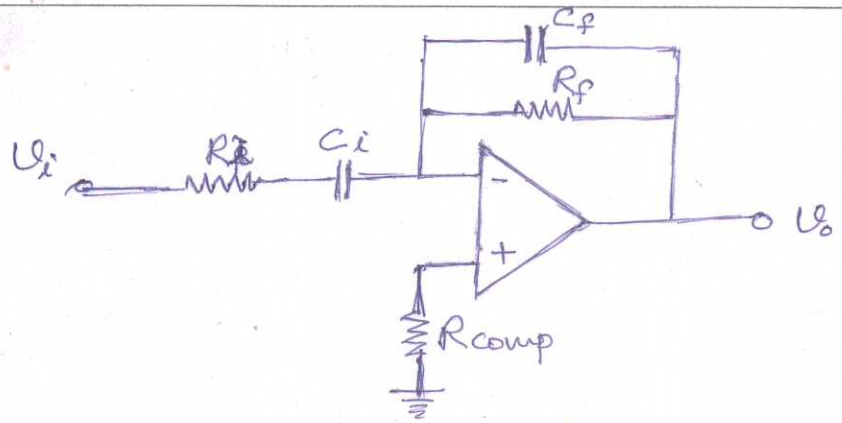
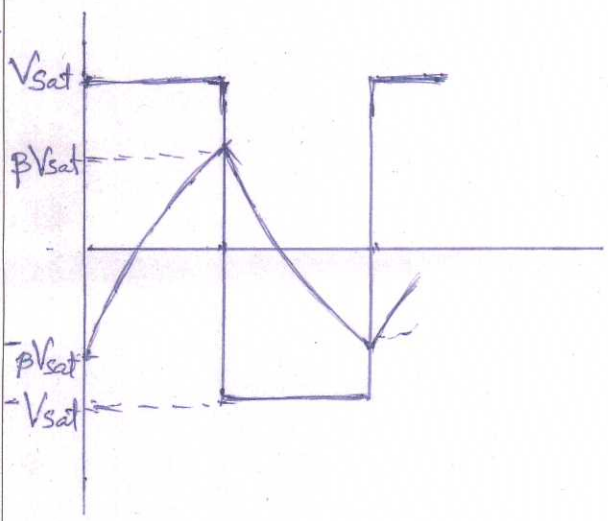
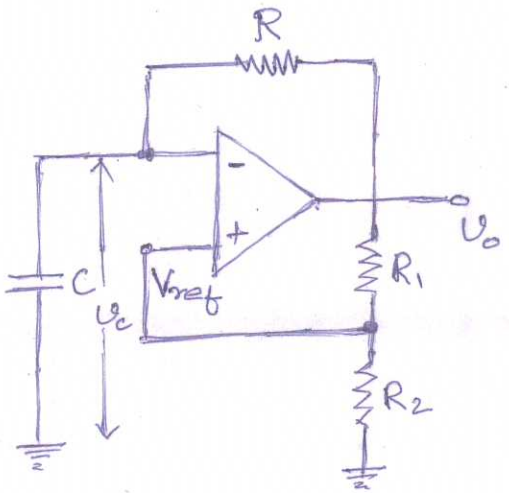
b.	 The introduction of R_i and C_f makes the ckt more stable and insensitive to high frequency noise. With increase in frequency the input impedence decreases in a simple differentiator because of reduction in X_{Ci}. Here C_f compensates for this.	6	
VII a.	  $V_{ref} = \beta V_o$ where $\beta = \frac{R_2}{R_1+R_2}$ and $V_o = {}^{+}V_{sat}$ or $^{-}V_{sat}$	6	

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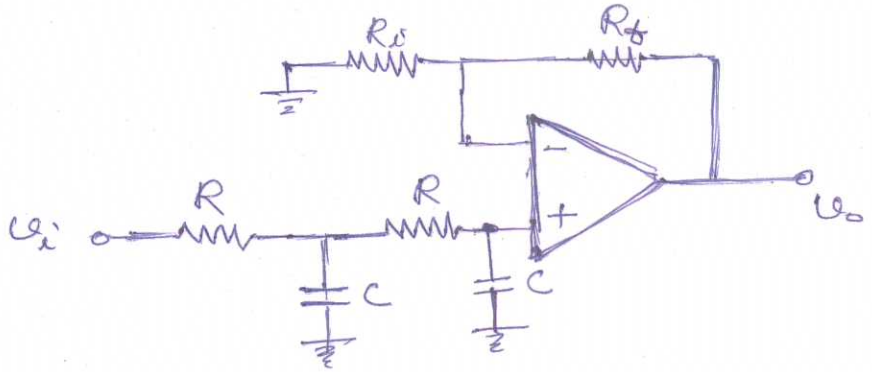
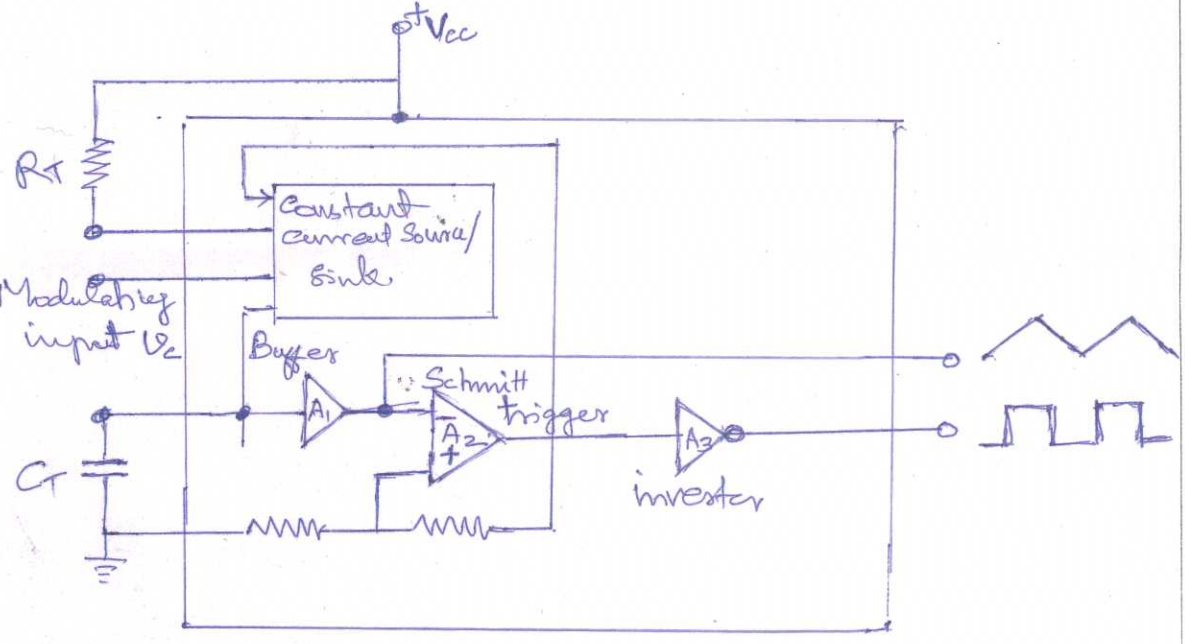
	Let initially $v_o = +V_{sat}$ C charges toward $+V_{sat}$ through R. When v_c exceeds $+\beta V_{sat}$ v_o becomes $-V_{sat}$ now $V_{ref} = -\beta V_{sat}$. When v_c exceeds $-\beta V_{sat}$ the o/p switches back to $+V_{sat}$.	6	
b.		3	
	Cut off frequency $= \frac{1}{2\pi RC}$		
VII a		7	

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	The timing capacitor C_T is linearly charged or discharged by the constant current source/sink. The amount of current can be controlled by changing the voltage modulating voltage or by changing the timing resistor R_T. Since the source and sink currents are equal capacitor charges at discharges for the same amount of time, giving a triangular voltage waveform across C_T which is available at the o/p as shown. The o/p frequency is given by $f_o = \frac{2(V_{cc} - V_E)}{R_T C_T V_{cc}}$	5	
b) i	As frequency multiplier/divider	3	
ii	As frequency translator		
iii	In AM detection, FM detection etc.		
VIII	In the standby state FF holds the transistor Q_1 ON thus clamping the capacitor C to ground and keeping the o/p at ground potential. As the trigger passes through $V_{cc}/3$ the FF is set making Q_1 off thus allowing C to charge through R towards V_{cc}. After a time interval T when the	4	

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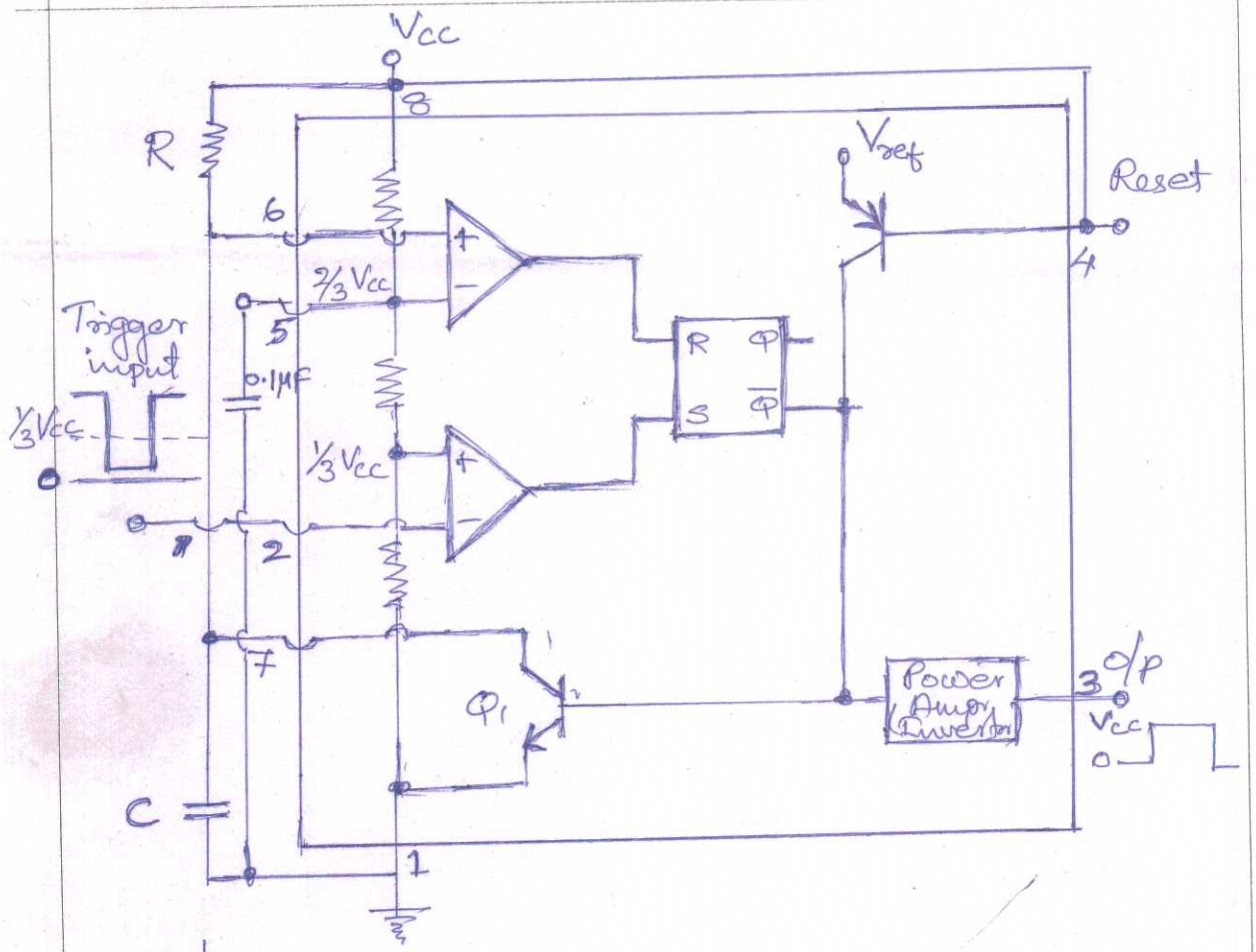
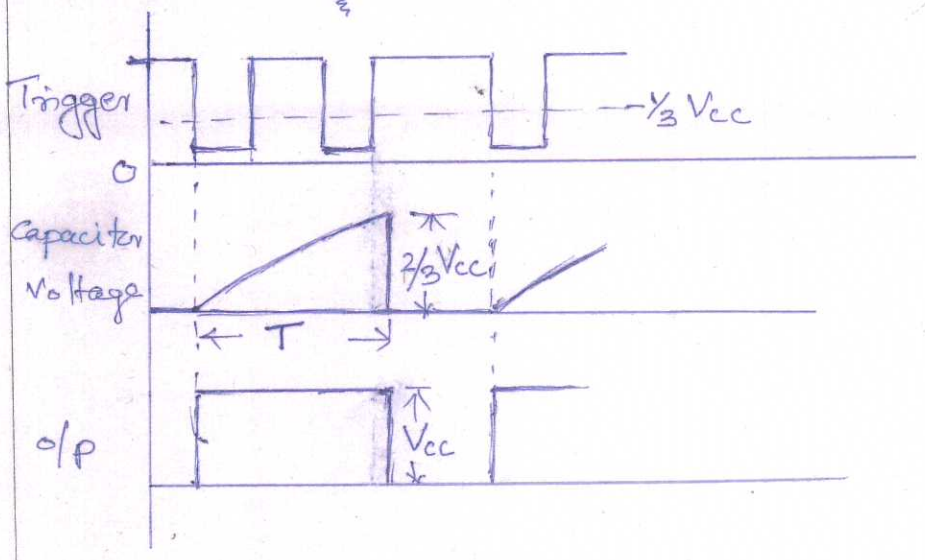
t	Scoring Indicator	Split Up score	Total
		7	
		4	

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	capacitor voltage exceeds $\frac{2}{3}V_{cc}$ the upper Comparator resets the FF making Q_1 again ON, thereby discharging C rapidly.		
IX a) i)	The regulated o/p voltage is fixed as specified by the manufacturer and is available as 78XX/79XX Series, with last two digits showing the o/p voltage		
ii)	The unregulated input voltage must be atleast 2V more than the regulated output voltage	3	
iii)	The IC is usually provided with a heat sink to provide the maximum rated current $I_{o(max)}$		
iv)	The IC has a temperature sensor which turns off the IC when it becomes too hot. The o/p current will drop and remain there until the IC is cooled.		
b)	Figure shows the set up for a +15/-15 V dual supply using IC 320 and IC 340. D_1 and D_2 protect the regulator against short circuit at input terminals D_3 and D_4 provides protection against non-synchronous turn-on of two regulators.	4	

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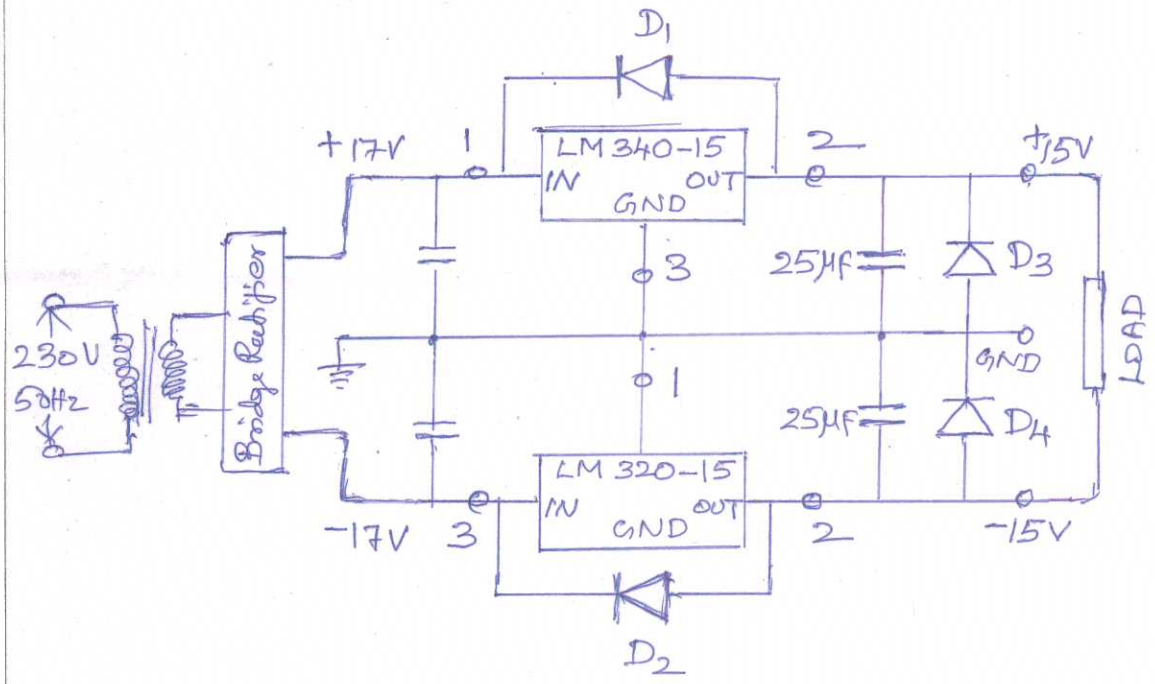
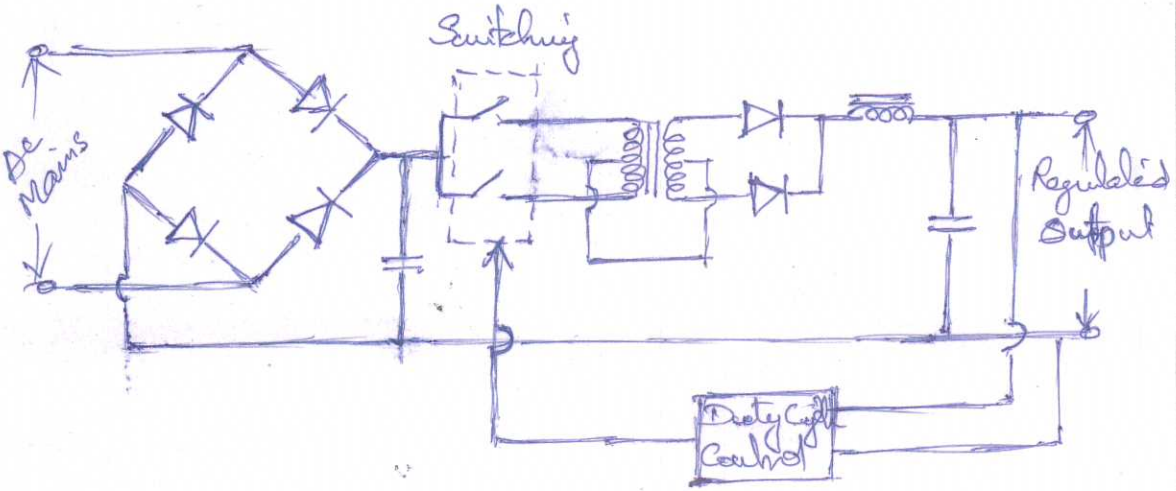
A		8	12
X Q1		5	9

The input AC is first converted into unregu-
-lated dc which in turn is chopped by the
switching elements operating at a rapid rate

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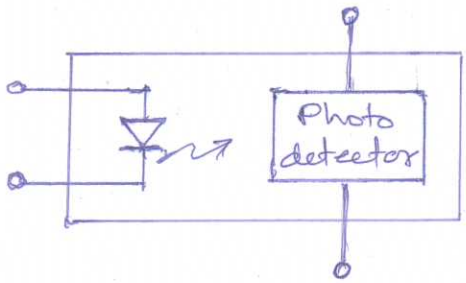
	The resultant pulse train is transformer coupled to an output n/w which provides final rectification and smoothing of the dc o/p. Regulation is accomplished by control circuits which vary the duty cycle of the switching elements of the o/p voltage tends to vary	4	
b)	Opto couplers are used to provide electrical isolation b/w two parts of a circuit. It generally consists of an LED and photo transistor coupled together with a dielectric or light pipe encapsulated in a case as shown so that the light from the LED is focused directly on the opening of the photo transistor and no outside light is detected. The input signal is connected to the LED and the o/p signal to the transistor 	6	