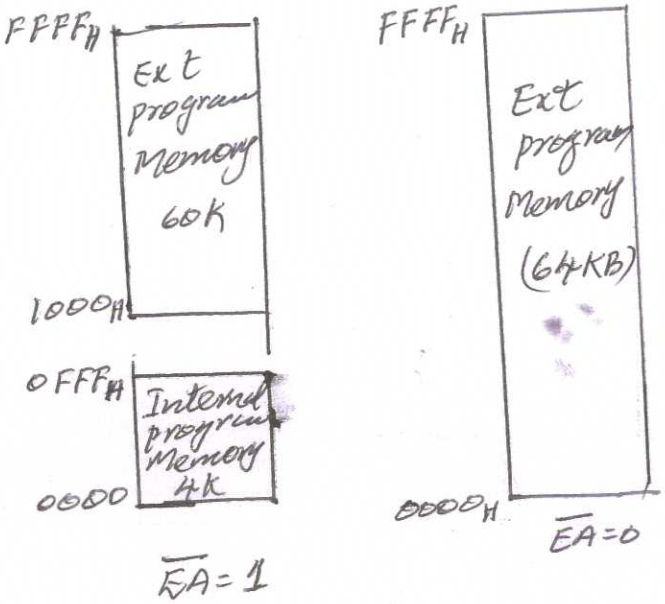
SCHEME OF VALUATION
(Scoring Indicators)

Revision : 2015 course code : 4043

Course Title : Microcontroller and Interfacing

Qst No.	Scoring Indicator	Split up score	Sub Total	Total
	PART A			
I (1)	Used as temporary storage register Mul and Div instructions one operand is in B reg:	1	2	
(2)	INTO		2	
(3)	Timer 1		2	
(4)	Used to control contrast of LCD		2	
(5)	To set variouse Timer operation modes		2	10
	PART B.			
II 1			3	
	Code (program) memory max: 64KB when EA=0 it select Ext code memory When EA=1 it select int code memory of 4KB remaining shared by Ext Memory of 60K	3		-6-

II

2

```
TOP:  SETB  P1.3
      ACALL DELAY
      CLR   P1.3
      ACALL DELAY
      SETB  P2.3
      ACALL DELAY
      CLR   P2.3
      ACALL DELAY
      SJMP  TOP

DELAY: MOV R2, #FFH
TOP1:  MOV R3, #FFH
here:  DJNZ R3, here
       DJNZ R2, TOP1
       RET
```

-6-

6-

3.

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{EA}$	-	ET2	ES	ET1	EX1	ET0	EX0

3

$\overline{EA}$ = 0 Disable all interrupts
= 1 Interrupts enabled as per individual enable bits

ET2 = Enable or disable Timer 2 o/f interrupt

ES = Enable or disable serial interrupt

ET1 = Enable or disable Timer 1 overflow interrupt

EX1 = Enable or disable Ext. interrupt 1.

ET0 = Enable or disable Timer 0 o/f interrupt

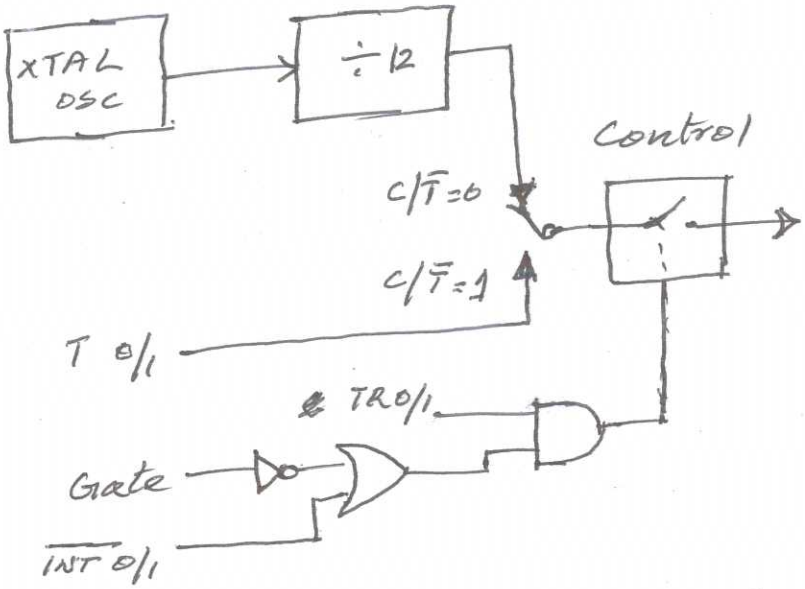
EX0 = Enable or disable Ext interrupt 0.

-3-

-6-

II

(b)



3

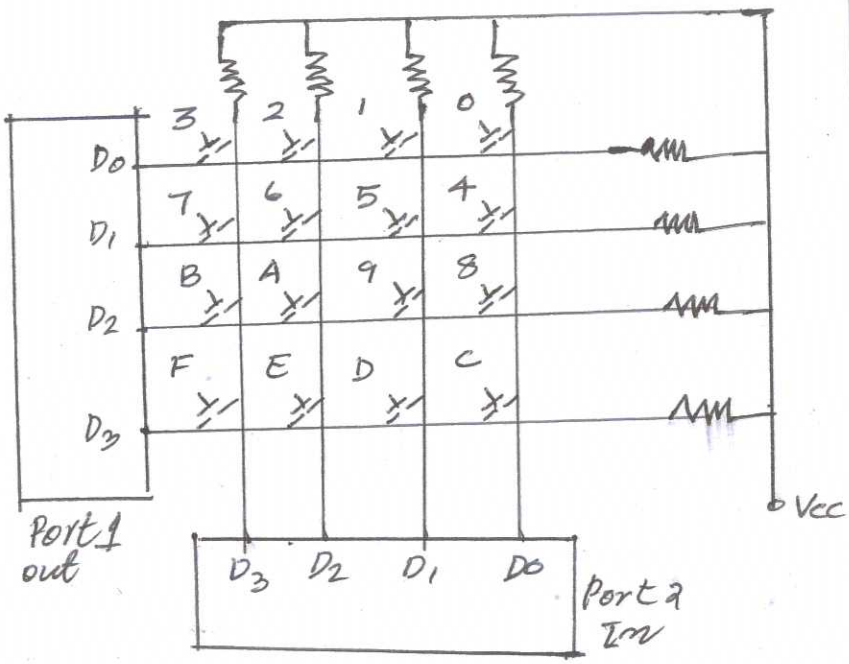
In 8051 Timer 0 and Timer 1 are controlled separate control circuits

Timer 0 by T0, TR0, Gate, INT0

Timer 1 by T1, TR1, Gate, INT1

3 -6-

(5)

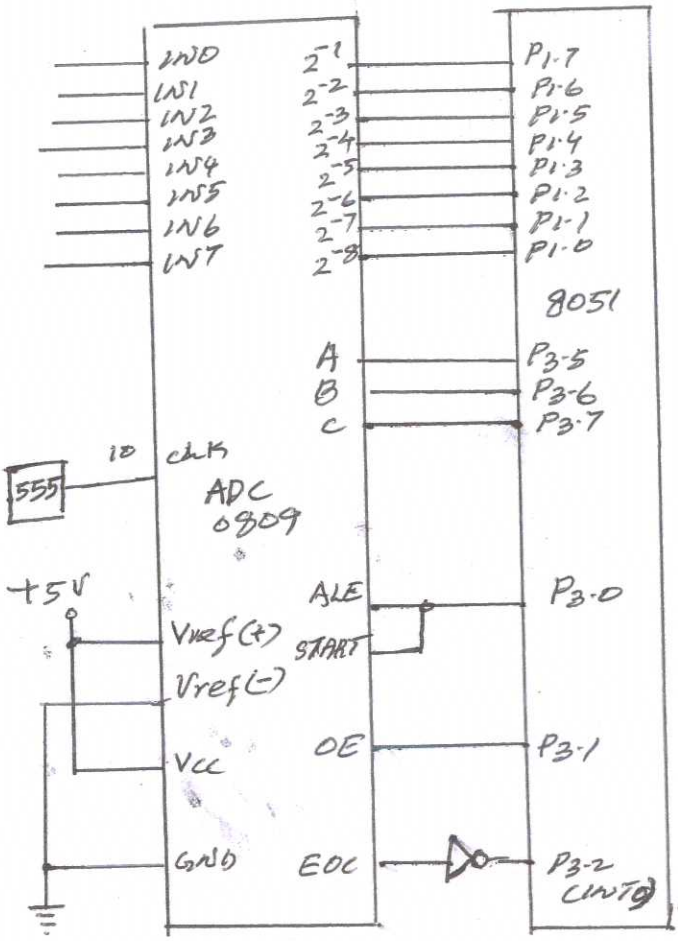


3

*Rows are connected at the output of one port
*columns are connected to the input of the port.
*If no keys are pressed reading the port 1 for all columns.
* If rows are grounded a key is pressed, one of the columns have 0
* Microcontroller by using scanmode identifying the key pressed by using software

3 -6-

6-



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I

(f) 1. RESET must be active high.
2. It requires 2 machine cycles.
In this period internal registers initialised
program counter is cleared.
3. Reset does not change content of
internal RAM
4. PC is cleared
5. SP is initialised by 07H.
6. register bank #0 is selected
all ports output 1=FH.

6x1 | 6 | 6

PART C

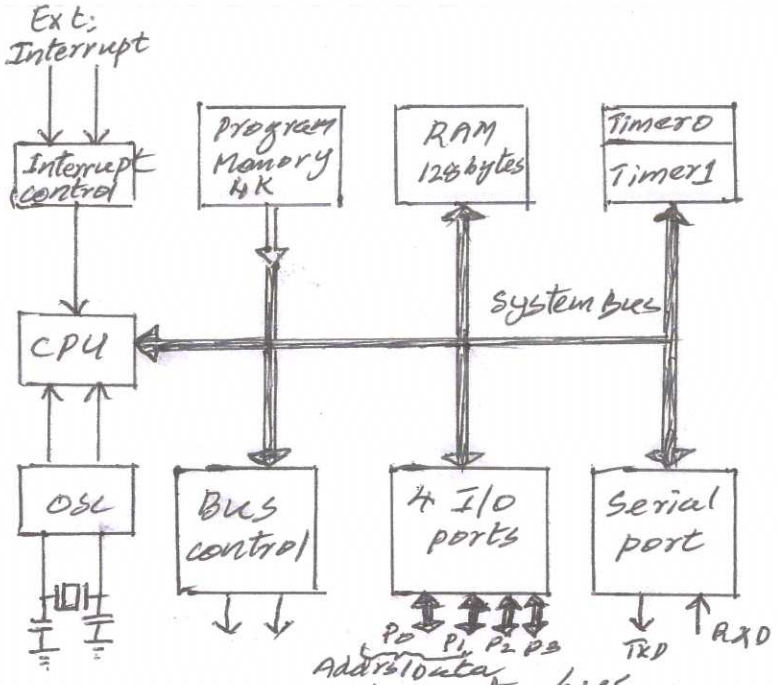
III

(a)

Feature	8031	8032	8051
Onchip ROM	0	0	4K.
RAM	128	256	128
Timers	2	3	2
I/o pins	32	32	32
Serial port	1	1	1
Interrupt source	6	6	6
No. of pins	40	40	40

7x1 | 7 | 7

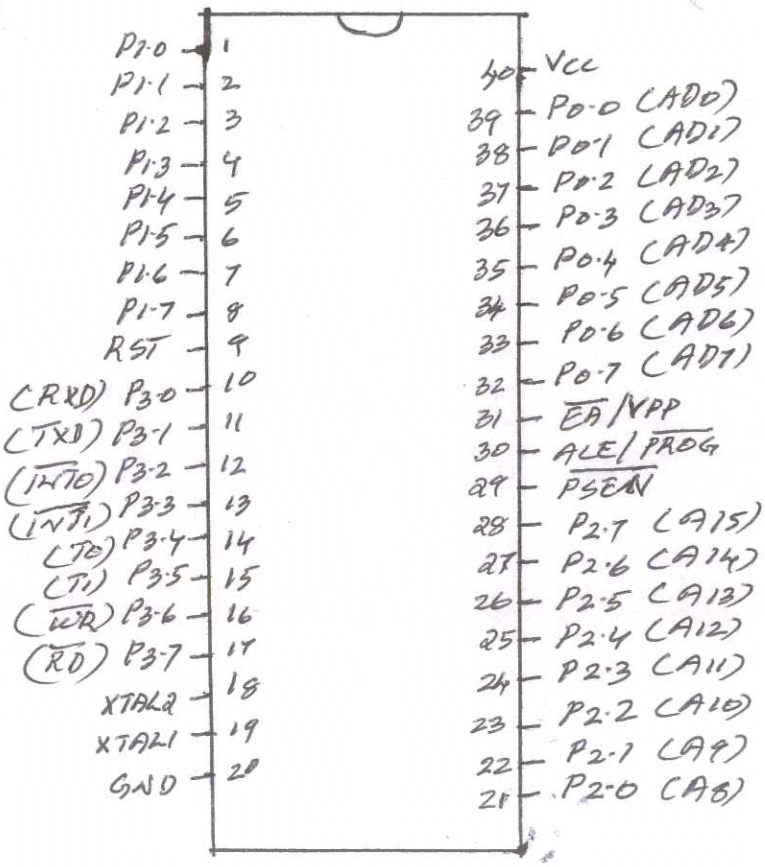
(b)



4 -

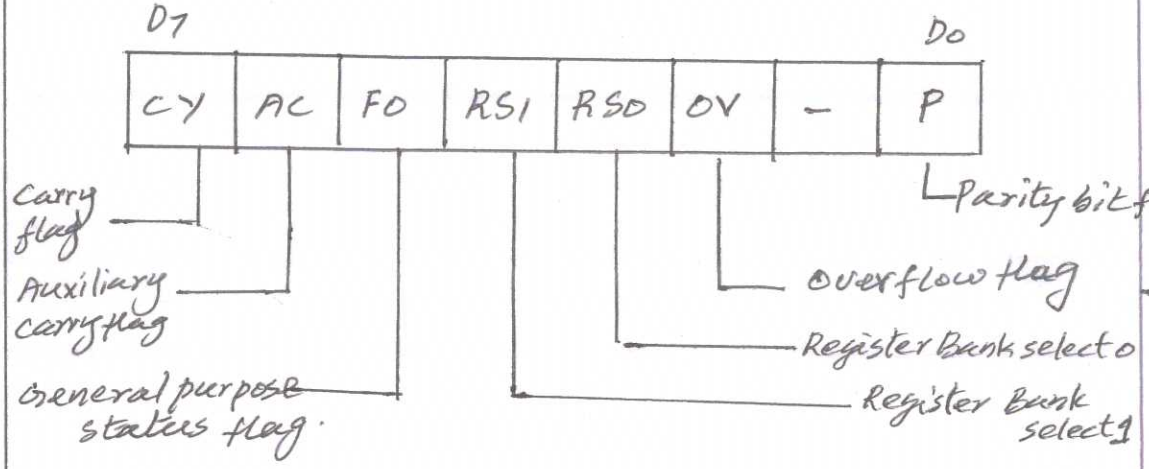
8051 has 8 bit data bus
16 bit address lines
4K program memory
128 byte data memory.
4, parallel port such as P_0, P_1, P_2, P_3
Timers, Serial Interface, bus controller 4 8 - 8 -
interrupt controller, CPU, osc ckts

IV (a)



- 8 -

(b)



CY – when carry out from D7 it set of Acc

AC – set when carry D3 to D4 of Acc

F0 – User defined general purpose flag.

RS1	RS0	Select Bank
0	0	Bank0
0	1	Bank1
1	0	Bank2
1	1	Bank3

OV – Overflow flag bit sets when arithmetic operation carry from D6 not from D7 or a carry from D7 not from D6 of Acc

P – Parity flag – set for odd parity of Acc.

V (a)

CJNE A, direct rel
CJNE A, #data rel
CJNE Rn, #data rel
CJNE @Ri, #data rel

CJNE <destbyte>, <sourcebyte>, rel

compare the magnitude of first two operands and branches if their values are not equal

* 3 byte Instruction

DJNZ <byte>, <rel addr>

Decrement and Jump if not zero.

*2&3 byte instruction

DJNZ Rn, rel — 2 byte Instructions -3-

DJNZ direct, rel — 3 byte Instructions -8-

V (b)

Interrupt	ROM location	Pin
Reset	0000H	9
INT0	0003H	P3.2 (12)
TF0	000BH	
INT1	0013H	P 3.3 (13)
TF1	001BH	
RI and TI	0023	

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VI (a)

```
      MOV DPTR, #4500H
      MOV A, #0X55
      SUBB A, #0X77
      JNC NEXT
      CPL A
      INC A
NEXT : MOVX @DPTR, A
XXX  SJMP XXX
```

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(b) IP- Interrupt Priority Register

D7							D0
—	—	PT2	PS	PT1	PX1	PT0	PX0

PT2 - Timer 2 interrupt priority level (8052)

PS — Serial port interrupt priority level

PT1 = Timer 1 interrupt Priority level

PX1 = Ext interrupt 1 priority level -7-

PT0 - Timer 0 interrupt priority level

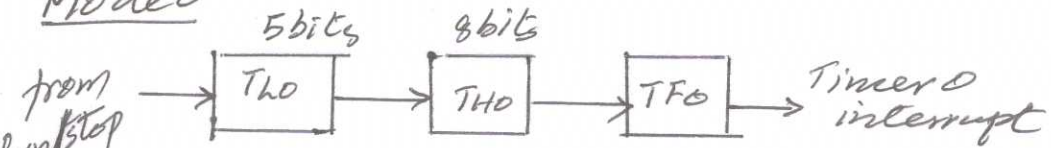
PX0 - Ext: interrupt priority level

(If the bit is 0 - lowest priority

" " 1 - Highest priority

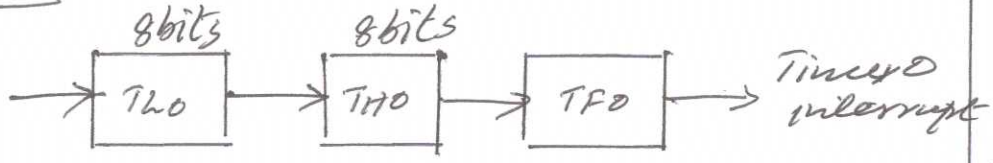
VII (a) Any two modes of Timer 0 explain

Mode 0



13 bit Timer/counter 4

Mode 1.



16 bit Timer/counter 4

Mode 2 (auto reload)
Mode 3 (Two 8bit Timer) } can also explain. -8-

(b) $T = \frac{1}{1KHz} = 1ms$.

ie $0.5ms + 0.5ms$.

$\frac{0.5ms}{1.085\mu s} = \frac{500\mu s}{1.085\mu s} = 461$ cycles.

Delay to Timer = $65536 - 461$

$= 65075$

In Hex =

16 | 65075	
4067	3
254	3
F	E

$= FE33$

```
        MOV TMOD, #10H
AGAIN : MOV TL1, #33H
        MOV TH1, #FEH
        SETB TR1
BACK :  JNB TF1, BACK
        CLR TR1
        CPL P2.4
        CLR TF1
        SJMP AGAIN
```

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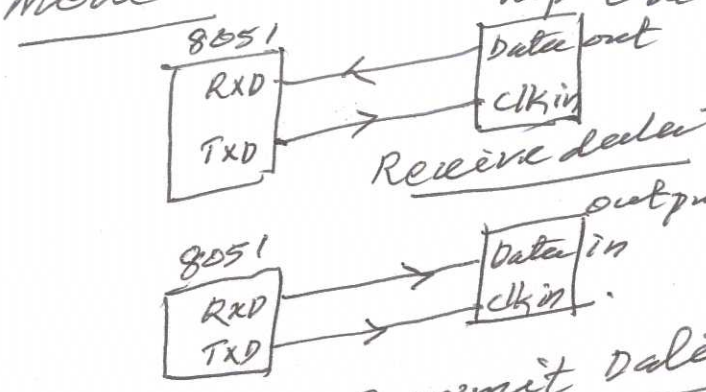
VII (a) Any two modes explain

1. mode 0 - Shift register mode
2. mode 1 - 8 bit UART
3. mode 2 - 9 bit UART with fixed Baud rate
4. mode 3 - 9 bit UART with variable baud rate

mode 0



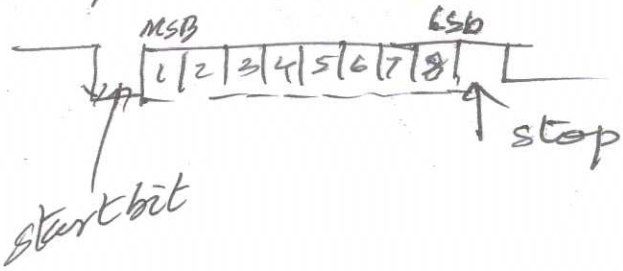
Use half duplex mode. TXD pin used as clock signal. RXD pin used for data reception in one case & RXD pin used for data transmission in another case.

4

Mode 1- standard UART.

Here One start bit, 8 data bit and one stop bit.

Totally 10 bit format. Uses Full duplex receiver / transmitter

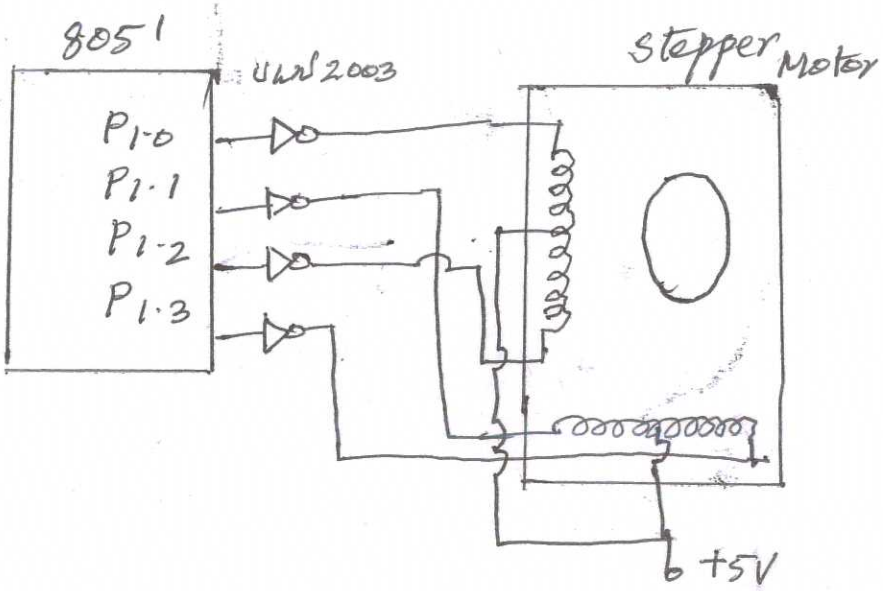


4 8-

(b)

```
        MOV TMOD, #20H
        MOV TH1, #-3
        MOV SCON, #50H
        SETB TR1
AGAIN:  MOV A, #"X"
        MOV SBUF, A
HERE:   JNB TI, HERE
        CLR TI
        SJMP AGAIN
```

IX (a)

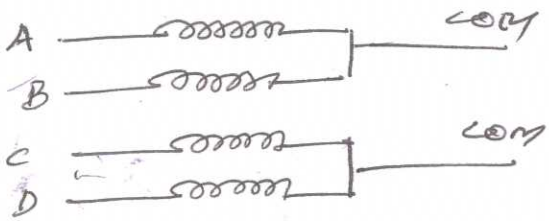


Normal 4 step sequence.

step	A	B	C	D
1	1	0	0	1
2	1	1	0	0
3	0	1	1	0
4	0	0	1	1

↑ anticlockwise

↓ Clock wise



stator winding

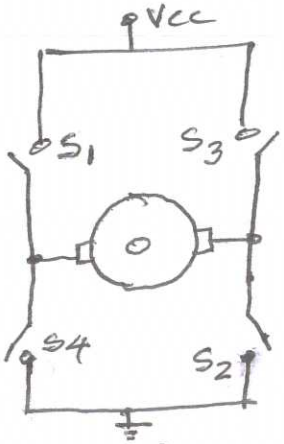
- 8 -

Stepper motor made of stator and rotor. stator consist of 4 electromagnets coils which is stationery. Rotor is permanent magnet which rotates. when coil energized by applying current electromagnetic field creates, rotor rotates. coil energised in a particular sequence to rotate.

```
        MOV A, #66H
TOP:    MOV P1, A
        RRA
        ACALL DELAY
        SJMP TOP
```

fig/Exp 4+4 - 8.

(b)



Polarity interchanging using H bridge

If S_1 and S_2 are closed, S_3 and S_4 are open the motor rotate clockwise otherwise S_3 and S_4 are closed, S_1 and S_2 are open the motor rotate anti clockwise.

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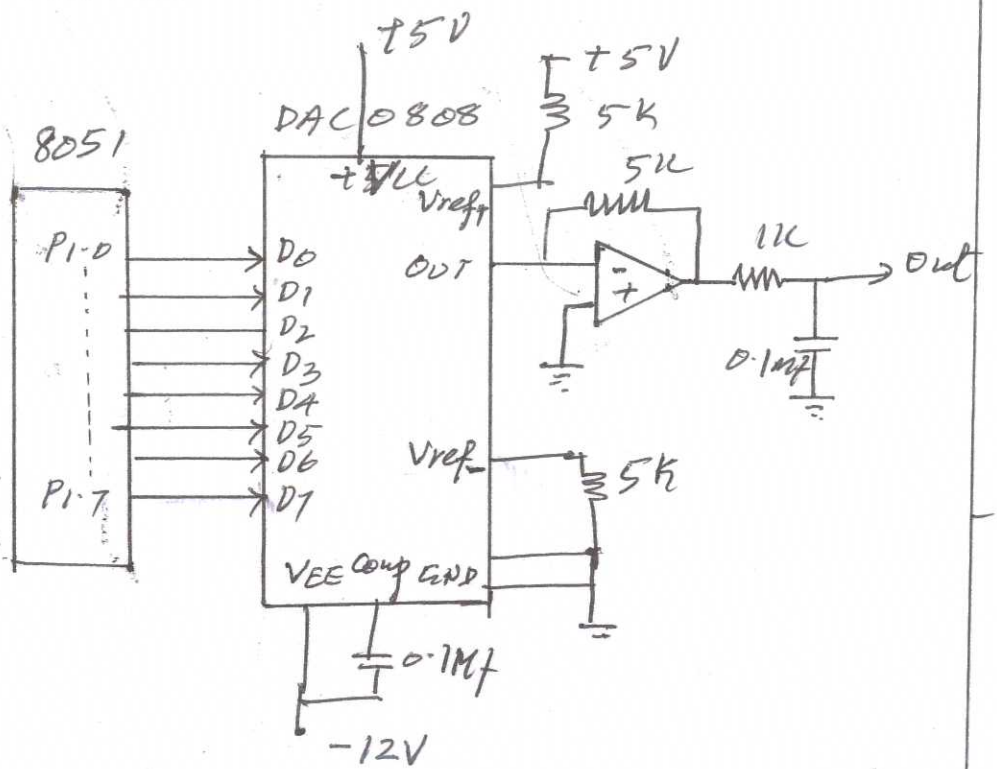
X (a)



-3-

DAC convert digital I/P to analog output. The output from micro-controller in digital form by using R/2R ladder method

DAC convert it as Iout in Outpin

$$I_{out} = I_{ref}\left(\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256}\right)$$

It is converted to voltage by the op amp Integrater circuit. -3-

Program

```
        org 0
            clr A.
up:     INC A.
        MOV P2, A
        CJNE A, #0FFH up.
        ACALL DELAY.
down:   DEC A.
        MOV P1, A.
        CJNE A, #00H down
        ACALL DELAY.
        sjmp up.
        End
```

2 -8-

(b) water level Indicater 7.