SCHEME OF VALUATION

(Scoring Indicators)

Revision :2015		Course Title: Digital Communication		
Course Code: 5201				
QST No	Scoring Indicator	Split up Score	Sub Total	Total
I	**PART A**			
1	Slope Overload Distortion Granular Noise	1*2	2	2
2	Amplitude Shift Keying Frequency shift keying Phase shift keying	2	2	2
3	Phase Shift Keying (PSK) is the digital modulation technique in which the phase of the carrier signal is changed accroding to message bits	2	2	2
4	Shannon–Hartley theorem tells the maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise $$C = B\log_2\left(1+\frac{S}{N}\right)$$	2	2	2
5	Half-duplex data transmission means that data can be transmitted in both directions on a signal carrier, but not at the same time	2	2	2
II	**Part B**	Fig:3	6	6
1	A continuous time signal can be represented in its samples and can be recovered back when sampling frequency fs is greater than or equal to the twice the highest frequency component of message signal. i. e. **fs≥2fm**. Sampling of input signal x(t) can be obtained by multiplying x(t) with an impulse train δ(t) of period T_s. The output of multiplier is a discrete signal called sampled signal which is represented with y(t) in the following diagrams:	Exp:3		

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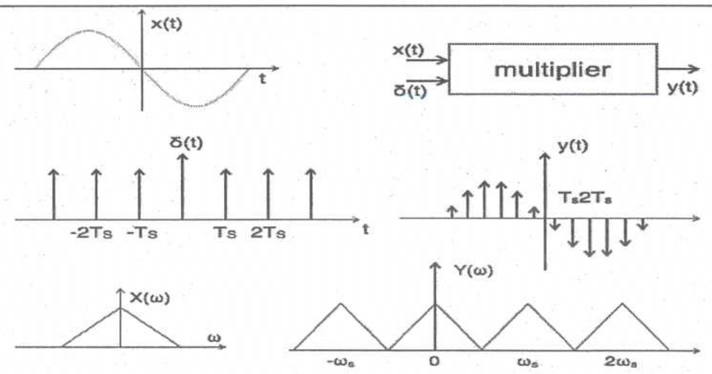
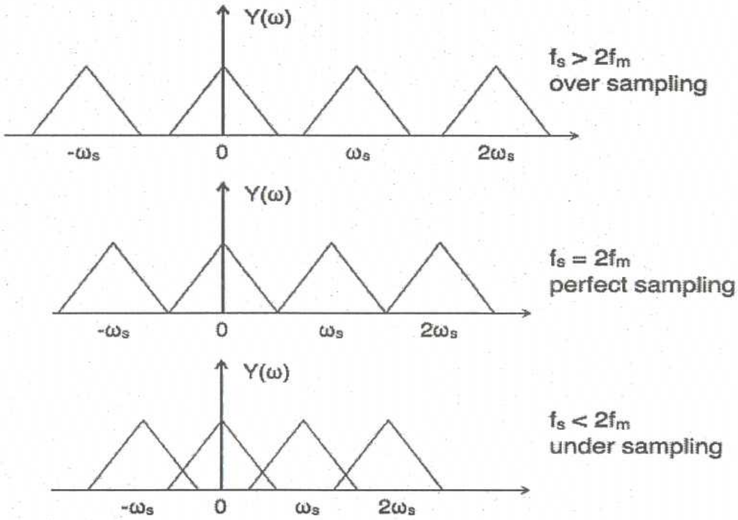


When fs < 2fm , aliasing occurs



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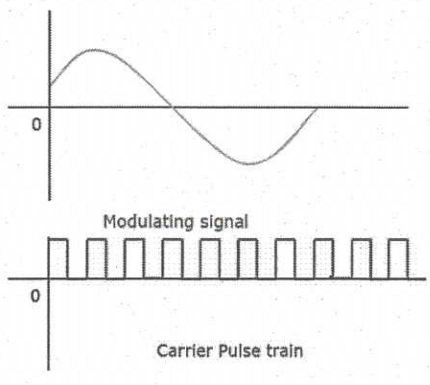
Pulse Amplitude Modulation (PAM) is an analog modulating scheme in which the amplitude of the pulse carrier varies proportional to the instantaneous amplitude of the message signal. Here width and position of the pulse remains constant.



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<td>Fig:3
Exp:3</td>
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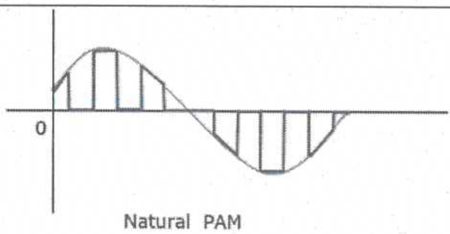
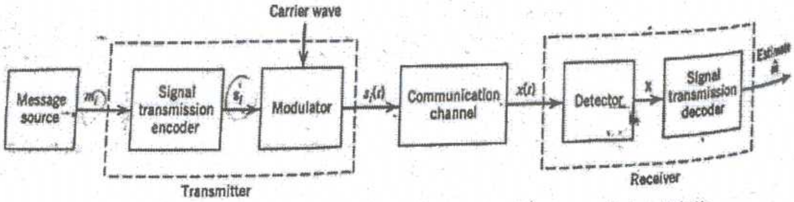
<tr><td></td><td>
Natural PAM</td><td></td><td></td><td></td></tr>
<tr><td>3</td><td>

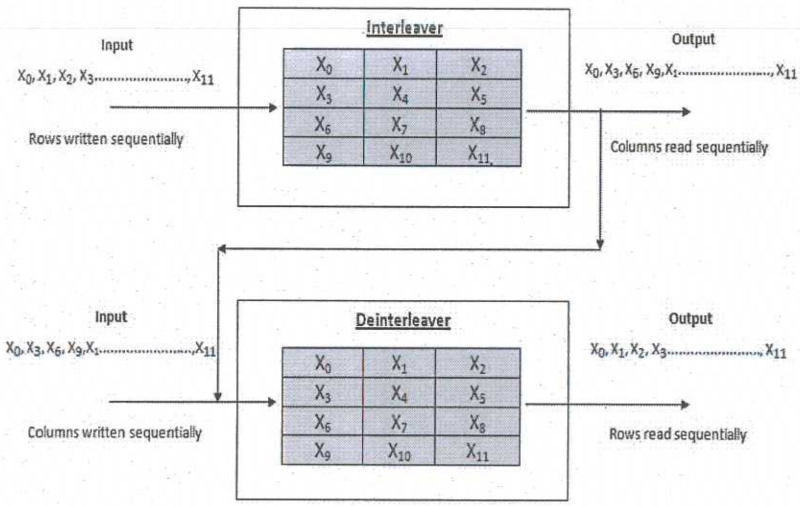
Functional model of passband data transmission system.

➢ Message source emits one symbol every T seconds
➢ Transmitter modulates the carrier wave
➢ Communication channel includes satellite channel/microwave radio link channel
➢ Receiver performs the reverse operation of transmitter and reduces the effect of channel noise</td><td>Fig:4

Exp: 2</td><td>6</td><td>6</td></tr>
<tr><td>4</td><td>Interleaving is used to convert convolutional codes from random error correctors to burst error correctors.

The basic idea behind interleaved codes is to jumble symbols at the receiver.

Block Interleaving : The input symbols are written sequentially in the rows .The output symbols are obtained by reading the columns sequentially. Thus, this is in form of M X N array. where N is length of the codeword.



Drawbacks of Block Interleaver :
Fig. A 4 X 3 Interleaver and Deinterleaver</td><td>Fig :2

Exp:2

Disadv:
2</td><td>6</td><td>6</td></tr>
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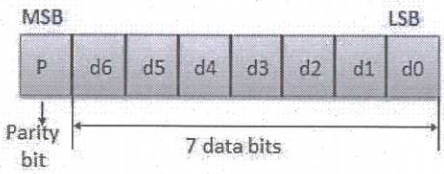
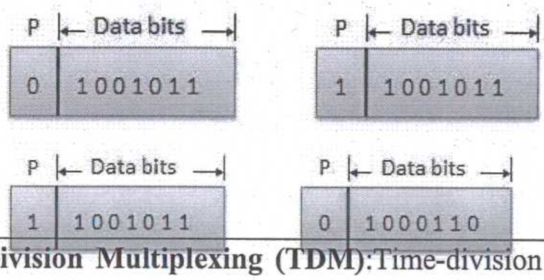
<table>
<tr><td></td><td>As, the columns are read sequentially, the receiver can interpret single row only after it receives complete message and not before that.
Also, receiver requires considerable amount of memory in order to store the received symbols and has to store complete message.
Two drawbacks,
1. latency
2. storage (fairly large amount of memory).</td><td></td><td></td><td></td></tr>
<tr><td>5</td><td>It is the simplest technique for detecting and correcting errors.The MSB of an 8-bits word is used as the parity bit and the remaining 7 bits are used as data or message bits.

The parity of 8-bits transmitted word can be either even parity or odd parity.



Even parity -- Even parity means the number of 1's in the given word including the parity bit should be even (2,4,6,....).

Odd parity -- Odd parity means the number of 1's in the given word including the parity bit should be odd (1,3,5,....).
The parity bit can be set to 0 and 1 depending on the type of the parity required.
For even parity, this bit is set to 1 or 0 such that the no. of "1 bits" in the entire word is even.
For odd parity, this bit is set to 1 or 0 such that the no. of "1 bits" in the entire word is odd

</td><td>Exp:6</td><td>6</td><td>6</td></tr>
<tr><td>6</td><td>Time-Division Multiplexing (TDM):Time-division multiplexing all signals operate with same frequency at different times.
An electronic commutator sequentially samples all data source and combines them to form a composite base band</td><td>Fig:4

Exp:2</td><td>6</td><td>6</td></tr>
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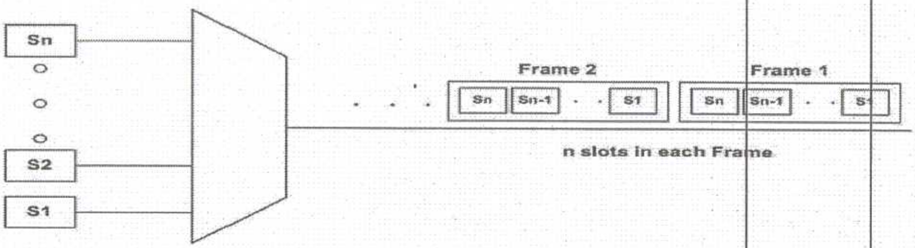
<td>signal.

The incoming data from each source are briefly buffered. Each buffer is typically one bit or one character in length.
The buffers are scanned sequentially to form a composite data stream.
The composite signal can be transmitted directly or through a modem.



The composite signal has some dead space between the successive sampled pulses, which is essential to prevent interchannel cross talks.
Along with the sampled pulses, one synchronizing pulse is sent in each cycle. These data pulses along with the control information form a frame.
Each of these frames contain a cycle of time slots and in each frame,
Synchronous TDM is called synchronous mainly because each time slot is preassigned to a fixed source. The time slots are transmitted irrespective of whether the sources have any data to send or not.

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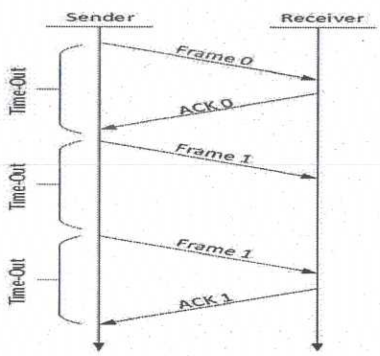
<td>7</td>
<td>Stop-and-wait ARQ


1.
The following transition may occur in Stop-and-Wait ARQ:

The sender maintains a timeout counter.
When a frame is sent, the sender starts the timeout counter.
If acknowledgement of frame comes in time, the sender transmits the next frame in queue.

</td>
<td>Fig:3
Exp:3</td>
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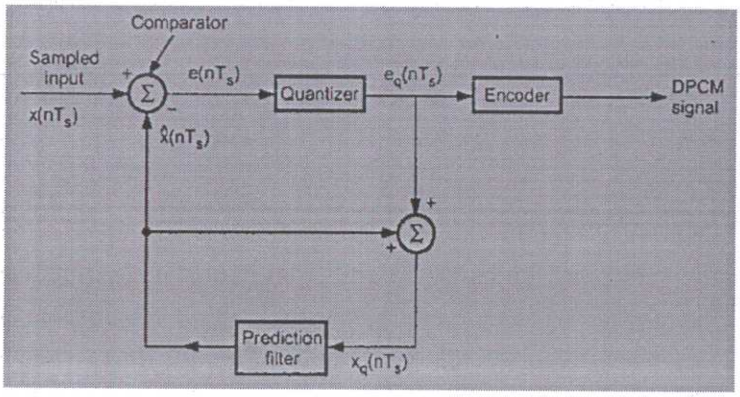
	4. If acknowledgement does not come in time, the sender assumes that either the frame or its acknowledgement is lost in transit. Sender retransmits the frame and starts the timeout counter. If a negative acknowledgement is received, the sender retransmits the frame.			
III a	(see table below)	Any 5 points : 7	7	7

PAM	PWM	PPM
Amplitude is varied	Width is varied	Position is varied
Bandwidth depends on the width of the pulse	Bandwidth depends on the rise time of the pulse	Bandwidth depends on the rise time of the pulse
Instantaneous transmitter power varies with the amplitude of the pulses	Instantaneous transmitter power varies with the amplitude and width of the pulses	Instantaneous transmitter power remains constant with the width of the pulses
System complexity is high	System complexity is low	System complexity is low
Noise interference is high	Noise interference is low	Noise interference is low
It is similar to amplitude modulation	It is similar to frequency modulation	It is similar to phase modulation

b | Fig: Txr : 3, Rxr: 3, Exp:2 | 8 | 8

Differential **p**ulse **c**ode **m**odulation (DPCM) is a procedure of converting an analog into a digital signal in which an analog signal is sampled and then the difference between the actual sample value and its predicted value (predicted value is based on previous sample or samples) is quantized and then encoded forming a digital value.

Transmitter



x(nTs) → sampled signal

x^(nTs)→ predicted signal.

The comparator finds out the difference between the actual sample value x(nTs) and the predicted value x^(nTs). This is called signal error and it is denoted as e(nTs)

$$e(nTs) = x(nTs) - x\hat{}(nTs) \; \ldots\ldots.(1)$$

Here the predicted value x^(nTs) is produced by using a prediction filter. The quantized error signal $e_q(nTs)$ is very small and can be encoded by using a small number of bits. Thus the number of bits per sample is reduced in DPCM.

The quantizer output would be written as,

$e_q(nTs) = e(nTs) + q(nTs)$ ……(2); q(nTs) is quantization error.

Prediction filter input $x_q(nTs)$ is obtained by sum of x^(nTs) and the quantizer output $e_q(nTs)$.

$x_q(nTs) = x\hat{}(nTs) + e_q(nTs)$………. (3)

by substituting the value of $e_q(nTs)$ from the equation (2) in equation (3) we get,

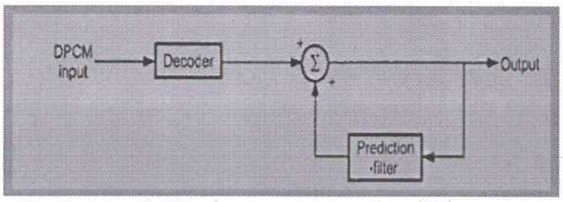
$x_q(nTs) = x\hat{}(nTs) + e(nTs) + q(nTs)$……. (4)

Equation (1) can written as, **$e(nTs) + x\hat{}(nTs) = x(nTs)$……. (5)**
from the above equations 4 and 5 we get,

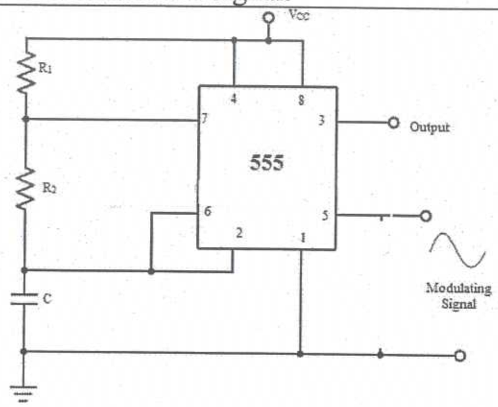
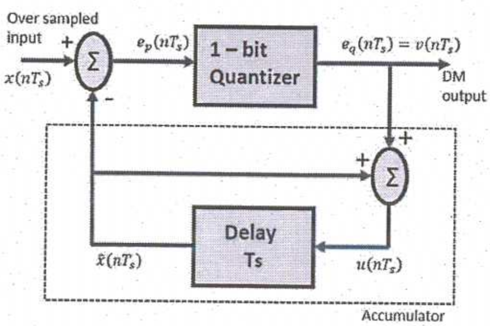
$x_q(nTs) = x(nTs) + x(nTs)$

Therefore, the quantized version of signal xq(nTs) is the sum of original sample value and quantized error q(nTs). The quantized error can be positive or negative. So the output of the prediction filter does not depend on its characteristics.

Receiver



DPCM Receiver consists of a decoder, a predictor, and a summer circuit.Decoder reconstructs the quantized error signal from incoming binary signal. The prediction filter output and quantized

	error signal are summed up to give the quantized version of original signal. The signal at the receiver differs from actual signal by quantization error q(nTs) which is permanently introduced in the reconstructed signal.			
IV a	 Modulating signal is applied to pin 5 which will get added to the threshold voltage inside. Initially the trigger voltage [2nd Pin] is below 1/3 VCC. Therefore the output voltage will be high. Capacitor starts charging and when the voltage across the capacitor reaches above threshold voltage the comparator gets reset and the output switches to 0v. Now the capacitor starts discharging. Once the capacitor voltage crosses 1/3VCC due to discharging the comparator inside IC555 again switches and the output voltage becomes high..Thus the charging and discharging time of capacitor varies and a PWM signal is obtained at the ouptut	Fig :4 Exp:3	7	7
b	Delta modulation is viewed as a 1-bit DPCM scheme. Present sample value is compared with the previous sample value and this result whether the amplitude is increased or decreased is transmitted Delta modulation provides a staircase approximation of input sampled signal. If step is reduced '0' is transmitted and is step is increased '1' is transmitted  The predictor circuit in DPCM is replaced by a simple delay circuit in DM.The 1-bit quantizer is equivalent to a two-level comparator.	Fig:4 Exp:4	8	8

x(nTs) = over sampled input
e(nTs) = summer output and quantizer input
e_q(nTs) = quantizer output = v(nTs)
x^(nTs) = output of delay circuit
u(nTs) = input of delay circuit

Error between sampled value and last approximated sample is given by

$$e(nT)=x(nTs) - \hat{x}(nTs)$$

v(nTs)=e_q(nTs)=Δ.sgn.[e(nTs)]

Depending on the sign of error e(nTs) , the sign of step size is decided

v(nTs) = +Δ if x(nTs) > x^(nTs) ; binary '1' is transmitted
v(nTs) = -Δ if x(nTs) < x^(nTs) ; binary '0' is transmitted

V a	QPSK is an expanded version from binary PSK where in a symbol consists of two bits and two orthonormal basis functions are used.	Fig:4 Exp:3	7	7

A group of two bits is often called a 'dibit'.

four dibits are possible. Each symbol carries same energy.

E: Energy per Symbol

T: Symbol Duration = 2. Tb, where Tb: duration of 1 bit.

$$s_i(t) = \sqrt{\frac{2E}{T}} \cos\left[2\pi f_c t + (2i-1).\frac{\pi}{4}\right]$$

S. No.	Input successive bits		Symbol	Phase shift in carrier
i = 1	1(1 V)	0 (-1 V)	S_1	π/4
i = 2	0(-1 V)	0(-1 V)	S_2	3π/4
i = 3	0(-1 V)	1(1 V)	S_3	5π/4
i = 4	1(1 V)	1(1 V)	S_4	7π/4

Incoming binary data sequence is first transformed into polar form by a non return to zero level encoder.

Symbol 1

Symbol 0

Demux seperates the binary wave into odd & even number input bits a1(t) & a2(t)

a1(t) & a2(t) are used to modulate the quadrature carriers

Result is two binary PSK signal which are added to produce

<table>
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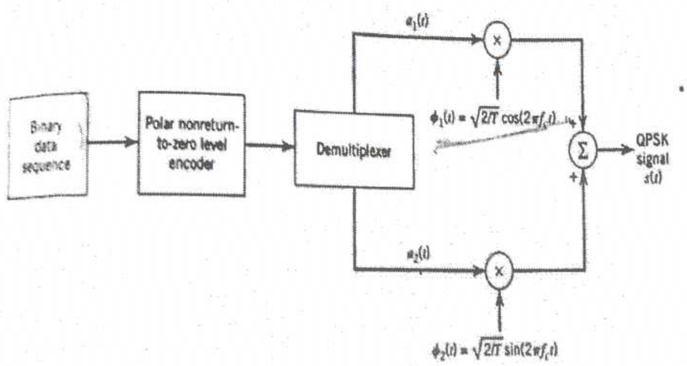
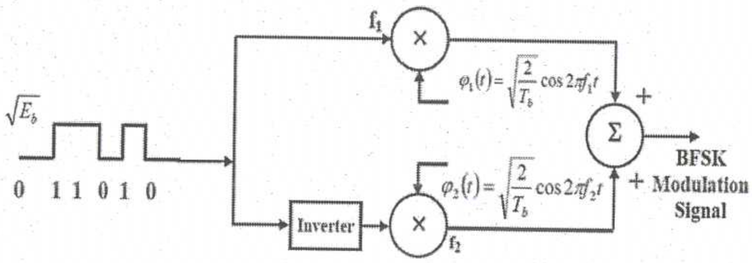
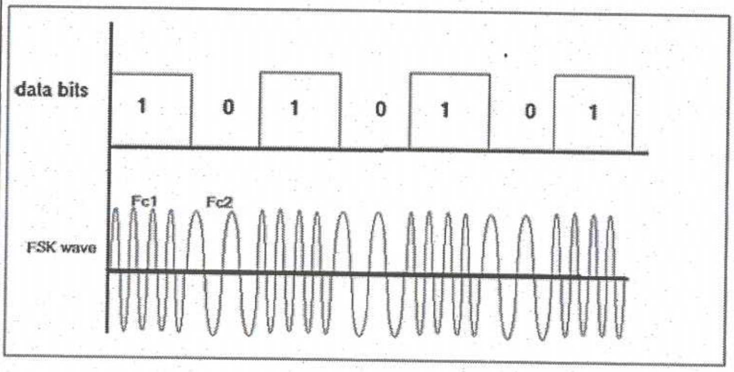

</td><td></td><td></td><td></td></tr>
<tr><td>b</td><td>Two carrier frequencies are used for binary frequency shift keying modulation.
FSK modulated signal
$$s_i(t)=\begin{cases}\sqrt{\dfrac{2E_b}{T_b}}\cos 2\pi f_i t, & 0\le t\le T_b,\ i=1,2\\ 0, & \text{elsewhere.}\end{cases}$$



</td><td>Fig: 5(Txr+ Rxr)

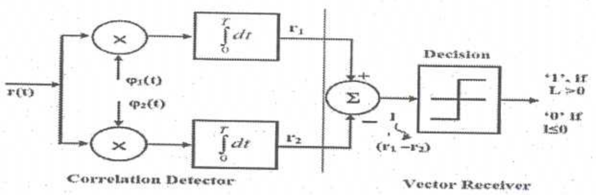
Exp:3</td><td>8</td><td>8</td></tr>
</table>

Input random binary sequence is represented by '1' and '0' where '0' represents no voltage at the input of the multipliers.

A '0' input to the inverter results in a '1' at its output.

Inverter, along with the two multipliers and the summing unit behave as a 'switch' which selects output of one of the two oscillators ·

FSK Demodulator



r(t) is the noisy received signal

Demodulator consists of two correlators with common input

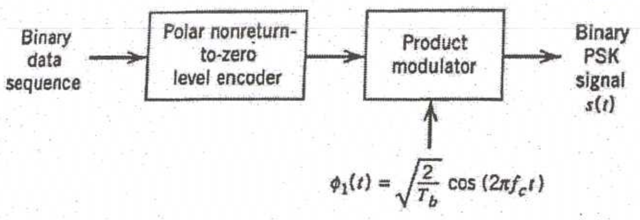
Locally generated coherent reference signal φ1(t) and φ2(t)

Correlated output is subtracted and the difference 'l' is compared with a threshold of '0' volts

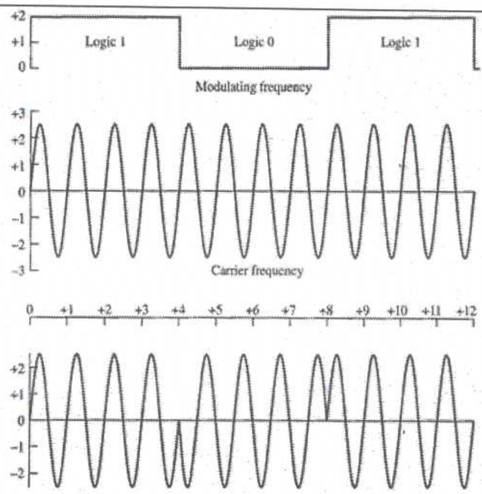
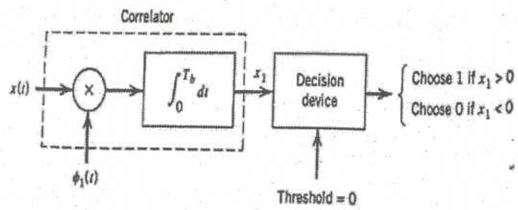
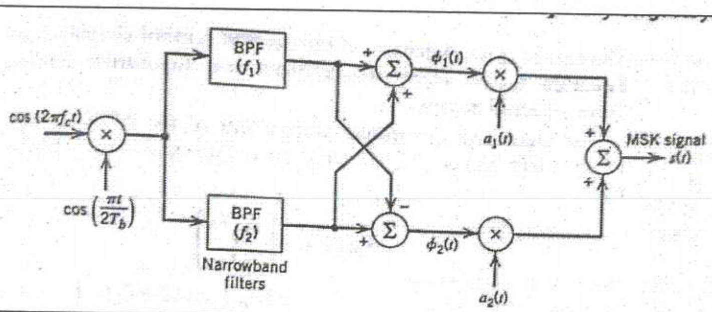
If l>0,'1' is transmitted & if l<0 '0' is transmitted

VI a | Fig :3*2 | 9 | 9

Exp: 3



- Input binary sequence '1' & '0' is represented by √Eb and -√Eb
- Resulting binary wave and carrier wave is applied to product modulator

	  ▸ Noisy PSK x(t) is applied to a correlator to which carrier is also given ▸ Correlator output x1 is compared with a threshold value of '0' ▸ If x1 > '0', receiver decides in favor of symbol 1 ▸ If x1 < '0', receiver decides in favor of symbol 0			
b		Fig: 6	6	6
VII a	Shanon Fano Algorithm ▸ Step1:List the source symbols in the order of decreasing probability ▸ Step2: Partition the set in to two sets such that sum of probabilities in each partition is nearly same and assign 0 to upper set and 1 to lower set ▸ Step3:Continue this process ,each time partitioning the sets with as nearly as equal probabilities as possible until	Exp:4 Exampl e:3	7	7

further partitioning not possible.

x_i	$P(x_i)$	Step 1	Step 2	Step 3	Step 4	Code
x_1	0.30	0	0			00
x_2	0.25	0	1			01
x_3	0.20	1	0			10
x_4	0.12	1	1	0		110
x_5	0.08	1	1	1	0	1110
x_6	0.05	1	1	1	1	1111

b

- Hamming codes are defined as (n,k) linear block codes
    - Number of check bits m≥3
    - Block length $n = 2^m - 1$
    - Number of message bits k = n-m
    - Minimum distance dmin = 3
    - Code rate r = k/n = (n-m)/n
    - r =1-(m/n)
    - Detect 2 errors (dmin $\geq$ t+1)
    - Correct one error (dmin $\geq$ 2t+1)

~~Fig 4~~

Exp :2

6

6

Generator Matrix

- *Matrix used to generate the code words from the given data bits*
- In an (n,k) linear block code C , a code vector c is given by

$$\mathbf{c} = \mathbf{d}G = [d_1\ d_2\ \dots\ d_k]\begin{bmatrix} 1 & 0 & \dots & 0 & p_{11} & p_{21} & \dots & p_{m1} \\ 0 & 1 & \dots & 0 & p_{12} & p_{22} & \dots & p_{m2} \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & \dots & 1 & p_{1k} & p_{2k} & \dots & p_{mk} \end{bmatrix}$$

$$G = [I_k\, P]$$

- c =dG
- Generator matrix have 'k' rows and 'n' columns;
    - i.e. G is a 'k x n' matrix
- Generator matrix is used in the encoder side.

Parity Check Matrix

- *Used in the receiver side to check whether the received word is correct or not*
- Denoted by H;
- H is an 'm x n' matrix $H = [\, P^T I_m]$
- c is the codeword $cH^T = dGH^T = 0$

$m = n - k$ and I_m is the mth-order identity matrix. Then

$$H^T = \begin{bmatrix} P^T \\ I_m \end{bmatrix}$$

Syndrome Decoding

- Let 'r' be the received word of length 'n' , when code word 'c' of length 'n' was sent over a noisy channel
- Then $r = c \oplus e$; where 'e' is the error pattern.
- To check whether the received vector is erraneous or not
  - Find the syndrome vector $S = rH^T$
  - If the syndrome vector is '0' ; no error occurred
  - If the syndrome vector is not '0' ;an error occurred
- To correct the detected error, find the bit position where error has occurred.
- i.e find the row position of syndrome vector in H^T matrix
- Row number will give the error bit position in the received word.
- Change the bit '0' to '1' or '1' to '0' accordingly for error correction

VIII a		Fig :6 Exp:3	9	9

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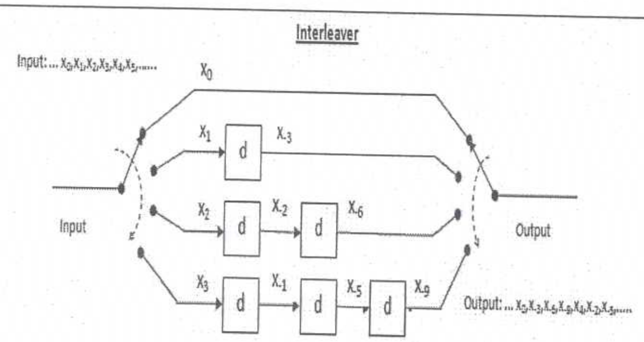
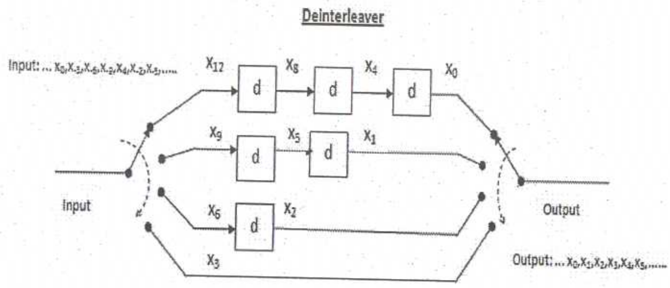


- Interleaver is used to rectify the Burst error
- Cross interleaver is a kind of multiplexer-demultiplexer system.
- In this system, delay lines are used to progressively increase length.
- Let **n** be the number of delay lines and **d** be the number of symbols introduced by each delay line.
- Thus, the separation between consecutive inputs = **nd** symbols



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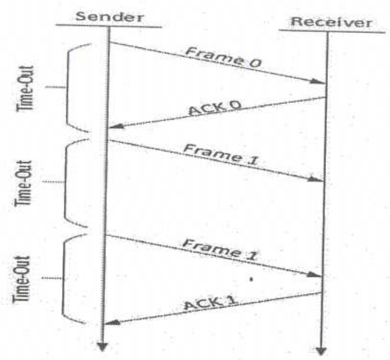
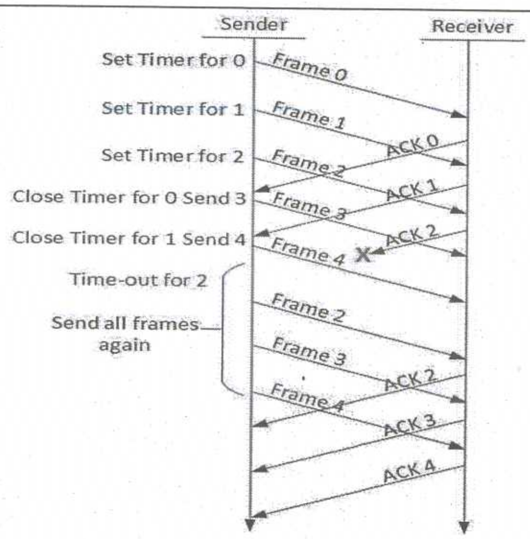
Cyclic Redundancy Code

- Error detecting code
- For a 'k'bit block of message bits, CRC Encoder generates (n-k) bit long frame check sequence(FCS)
- Let
  - T = n-bitframe to be transmitted
  - D=k-bit message block (information bits)
  - F=(n-k) bit FCS, the last (n-k) bits of T
  - P= predetermined divisor ,a pattern of (n-k+1)bits
- Pre determined divisor P should divide the codeword T.
- T/P has no remainder.
- Codeword T= $2^{(n-k)}$D +F
- Where F is the Frame check sequence
- $2^{(n-k)}$D amounts to shifting the 'k' message bits to left by (n-k)bits
</td><td>Exp :6</td><td>6</td><td>6</td></tr>
</table>

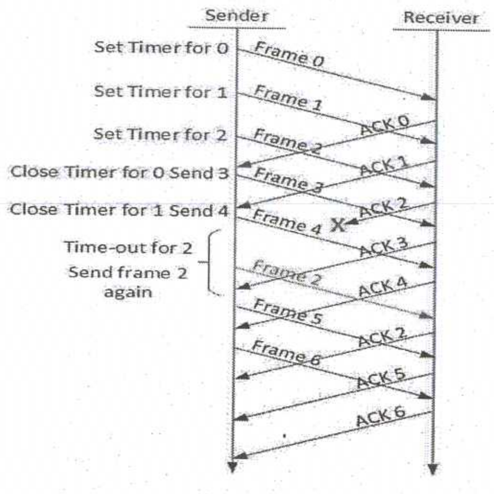
	▸ To generate an FCS , ▸ divide $2^{(n-k)}D$ by 'P' and use (n-k) bit remainder as FCS ▸ Let an error 'E' occur when 'T' is transmitted over noisy channel ▸ The received word V=T+E ▸ CRC will fail to detect the error if V is completely divisible by P ▸ i.e E is completely divisible by P			
IX a	• **Stop-and-wait ARQ**  The following transition may occur in Stop-and-Wait ARQ: • The sender maintains a timeout counter. • When a frame is sent, the sender starts the timeout counter. • If acknowledgement of frame comes in time, the sender transmits the next frame in queue. • If acknowledgement does not come in time, the sender assumes that either the frame or its acknowledgement is lost in transit. Sender retransmits the frame and starts the timeout counter. • If a negative acknowledgement is received, the sender retransmits the frame. **Go-Back-N ARQ (Sliding Window ARQ)** In Go-Back-N ARQ method, both sender and receiver maintain a window.	Fig:3*2. Exp:3	9	9

<table>
<tr><td></td><td>


The sending-window size enables the sender to send multiple frames without receiving the acknowledgement of the previous ones. The receiving-window enables the receiver to receive multiple frames and acknowledge them. The receiver keeps track of incoming frame's sequence number.

When the sender sends all the frames in window, it checks up to what sequence number it has received positive acknowledgement. If all frames are positively acknowledged, the sender sends next set of frames. If sender finds that it has received NACK or has not receive any ACK for a particular frame, it retransmits all the frames after which it does not receive any positive ACK.

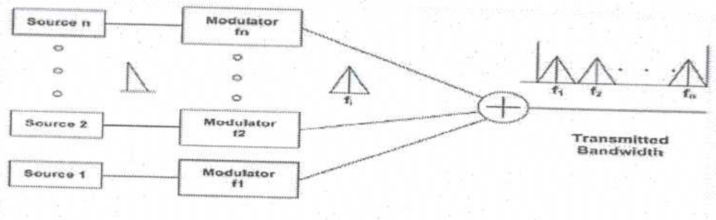
Selective Repeat ARQ



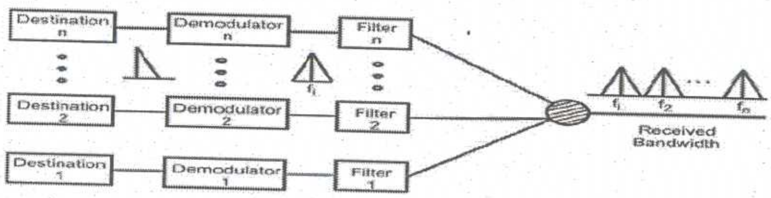
In Selective-Repeat ARQ, the receiver while keeping track of sequence numbers, buffers the frames in memory and sends NACK for only frame which is missing or damaged.

The sender in this case, sends only packet for which NACK is receive*d*.
</td><td></td><td></td><td></td></tr>
<tr><td>b</td><td>Frequency-Division Multiplexing (FDM): In frequency division</td><td>Fig :4</td><td>6</td><td>6</td></tr>
</table>

	multiplexing,Independent message signals are translated into different frequency bands using modulation techniques, which are combined by a multiplexer, to a composite signal. The resulting signal is then transmitted along the single channel. Basic approach is to divide the available bandwidth of a single physical medium into a number of smaller, independent frequency channels.The carriers used to modulate the individual message signals are called sub-carriers, shown as f1, f2, …, fn	Exp:2		

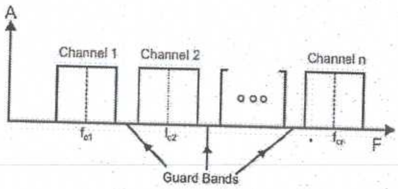


FDM Multiplexing Process



FDM Demultiplexing Process

At the receiving end the signal is applied to a bank of band-pass filters, which separates individual frequency channels. The band pass filter outputs are then demodulated and distributed to different output channels



If the channels are very close to one other, it leads to inter-channel cross talk.Channels must be separated by strips of unused bandwidth to prevent inter-channel cross talk. These unused channels between each successive channel are known as **guard bands** . FDM are commonly used in radio broadcasts and TV networks.

X a	**Synchronous Transmission** data is transferred in the form of frames Transmission requires a clock signal between the sender and receiver so as to inform the	**Asynchronous Transmission** Data is transmitted 1 byte at a time. Transmission sender and receiver does not require a clock signal as the data sent	Any 5 points:7	7	7

<table>
<tr><td></td><td>receiver about the new byte

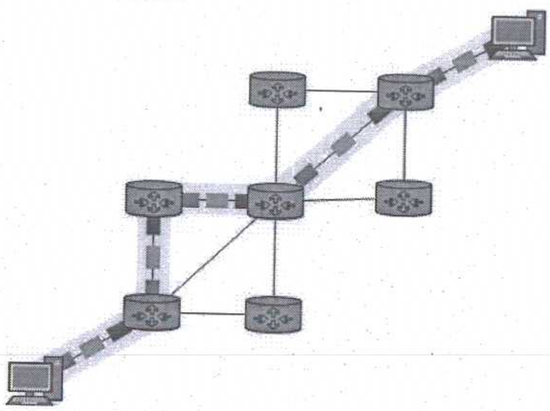
Data transfer rate is Faster
Transmission is complex and expensive & used for transferring the bulk of data

Transmission is efficient and has lower overhead</td><td>here has a parity bit attached to it which indicates the start of the new byte.
Data transfer rate is slower
Transmission is simple and economic and used for transmitting a small amount of data
Transmission is less efficient and has higher overhead</td><td></td><td></td><td></td></tr>
<tr><td>b</td><td colspan="2">

Circuit Switching : When two nodes communicate with each other over a dedicated communication path, it is called circuit switching. There is a need of pre-specified route from which data travels and no other data is permitted. In circuit switching to transfer the data, circuit must be established so that the data transfer can take place.

Circuits can be permanent or temporary. Applications which use circuit switching may have to go through three phases:

- Establish a circuit
- Transfer the data
- Disconnect the circuit

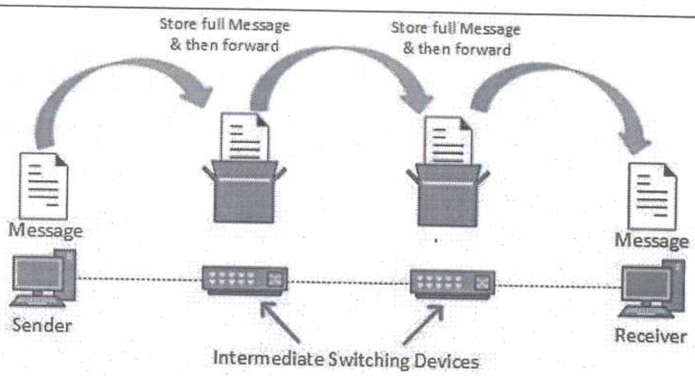


Telephone is the best suitable example of circuit switching

Message Switching : In message switching, the whole message is treated as a data unit and is switching / transferred in its entirety.

A switch working on message switching, first receives the whole message and buffers it until there are resources available to transfer it to the next hop. If the next hop is not having enough resource to accommodate large size message, the message is stored and switch waits.

</td><td>Exp :4*2</td><td>8</td><td>8</td></tr>
</table>



Message switching has the following drawbacks:

- Every switch in transit path needs enough storage to accommodate entire message.
- Because of store-and-forward technique and waits included until resources are available, message switching is very slow.
- Message switching was not a solution for streaming media and real-time applications.