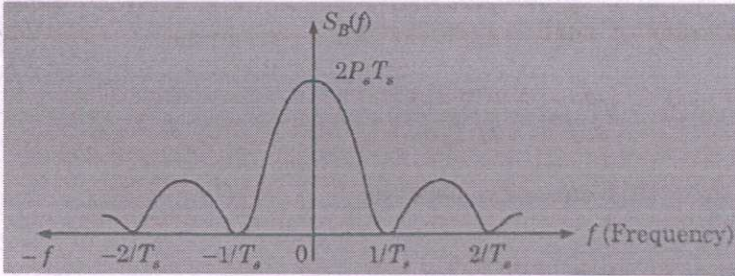
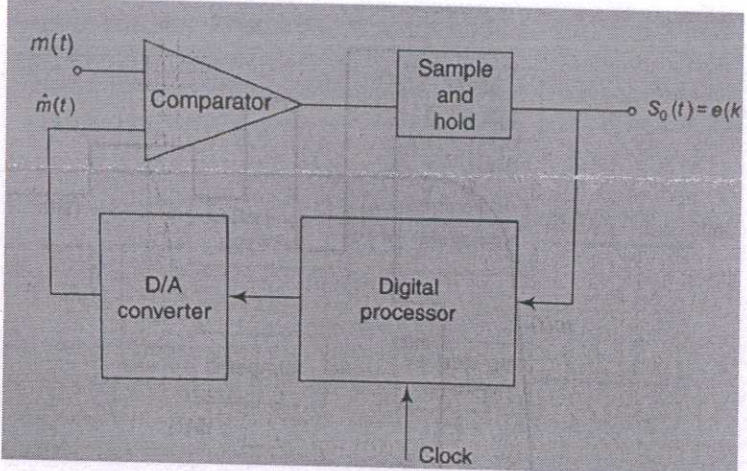


SCHEME OF VALUATION

Scoring Indicators

Revision : 2015 Course Title : Digital Communication		Course Code : 5201		
Qst. No.	Scoring Indicator	Split up score	Sub total	Total
I	PART A			
1	Pulse Amplitude Modulation (PAM), Pulse Width Modulation (PWM), Pulse Position Modulation (PPM)	2	2	2
2	 <p>$T_s = \text{Symbol duration}$</p>	2	2	2
3	<p>The information capacity of a continuous channel of bandwidth B hertz, with AWGN of power spectral density $N_0/2$ is</p> <p>$C = B \log_2 (1 + \text{SNR})$ b/s</p> <p>S is the signal power and N is the noise power</p>	2	2	2
4	In a communication channel, if the bit errors are closely clustered, then it is known as burst error.	2	2	2
5	<p>In private key or symmetric key algorithms, the same secret key is used for both encryption and decryption.</p> <p>In public-key or asymmetric key algorithms, each user has a public key, private key pair. The public key is used for encryption and a private key is used for decryption.</p>	1 + 1	2	2

<p>II PART B</p> <p>1</p>	<p>PAM: Pulse amplitude modulation</p> <ol style="list-style-type: none"> 1. Amplitude of the pulse train is proportional to the amplitude of the modulating signal 2. Bandwidth depends on the width of the pulse 3. Instantaneous power of the transmitter varies 4. Noise interference is high 5. No need for synchronization <p>PWM: Pulse width modulation</p> <ol style="list-style-type: none"> 1. Width of the pulse proportional to the amplitude of modulating signal 2. Bandwidth depends on the rise time of the pulse 3. Instantaneous power of transmitter varies 4. Noise interference is minimum 5. No need for synchronization <p>PPM: Pulse position modulation</p> <ol style="list-style-type: none"> 1. Relative position of the pulse is proportional to the amplitude of the modulating signal 2. Bandwidth depends on the rise time of the pulse 3. Instantaneous power remains constant 4. Noise interference is minimum 5. Additional synchronizing signal must be transmitted 	<p>2 × 3</p>	<p>6</p>	<p>6</p>
<p>2</p>	 <p>In adaptive delta modulation, the step size is not kept fixed. It is always a multiple of the basic step S_0. The processor has an accumulator and at each active edge of the clock waveform, generates a step S which augments or diminishes the accumulator. If the direction of step at</p>	<p>Fig 3 + Exp 3</p>	<p>6</p>	<p>6</p>

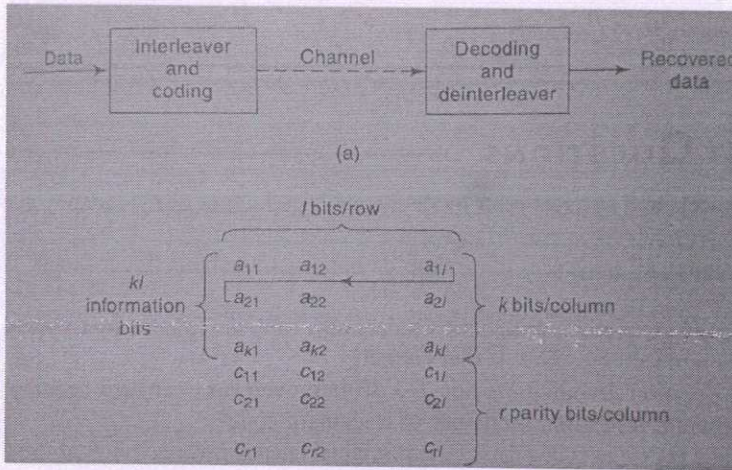
clock edge 'k' is the same as at edge 'k-1', then the processor increases the magnitude of the step by amount S_0 . If the directions are opposite, then the processor decreases the magnitude of step size by S_0 . Thus, when slope overload occurs, the step size becomes progressively larger, thereby allowing $m^{(t)}$ to catch up with $m(t)$ more rapidly.

3 Block interleaving consists of a shift register with 'k' rows and 'l' bits per row. The first bit enters the storage element at a_{11} . At each shift, each bit moves one position to the right. The bit in the rightmost storage element moves to the leftmost storage element in the next row. When the 'kl' bits have entered (register is full) each column is treated as a code word and parity bits are generated. Here the information bits in the code word are 'l' bits apart in the original stream. When the coding is completed, entire content of the information register as well as the parity bits are transmitted over the channel. At the receiver, data is saved in the same order as the transmitter and error correction decoding is performed. Because of this organisation of data bits, even if there is a burst error (of length 'l' bits), only one error occurs in each column and this single error can be corrected.

Fig 3
+
Exp 3

6

6



4

Shannon – Fano algorithm:

1. List the source symbols in the decreasing order of probability.
2. Partition the set into two sets that are close to equiprobables as possible and assign 0 to the upper set, 1 to the lower set.

	<p>3. Continue this process, each time partitioning these sets with nearly equal probabilities as possible until further partitioning is not possible.</p> <p>4. The code word for each symbol is the binary sequence that appears in its row.</p> <p>Example</p> <p>X1 0.5 0</p> <p>X2 0.25 1 0</p> <p>X3 0.125 1 1 0</p> <p>X4 0.125 1 1 1</p> <p>Code words:</p> <p>X1 0</p> <p>X2 10</p> <p>X3 110</p> <p>X4 111</p>	Exp 4 + Example 2	6	6
5	<p>Transmission mode defines the direction of flow of information between two communicating devices.</p> <p>The diagram illustrates three communication modes between a Sender and a Receiver:</p> <ul style="list-style-type: none"> Simplex: A single arrow points from the Sender to the Receiver. Half-Duplex: Two arrows, one pointing from Sender to Receiver and one from Receiver to Sender, with the word "OR" between them, indicating that communication can go in either direction but not at the same time. Full-Duplex: Two arrows, one pointing from Sender to Receiver and one from Receiver to Sender, with the word "AND" between them, indicating that communication can go in both directions simultaneously. <p>Simplex – communication takes place only in one direction (unidirection) Eg: TV, radio</p> <p>Half duplex – Can transmit data in both directions but only in one direction at a time Eg: Walkie-talkie</p>	2 × 3	6	6

Full duplex – Can transmit data simultaneously in both directions
 Eg: Telephone network

6

BPSK Receiver

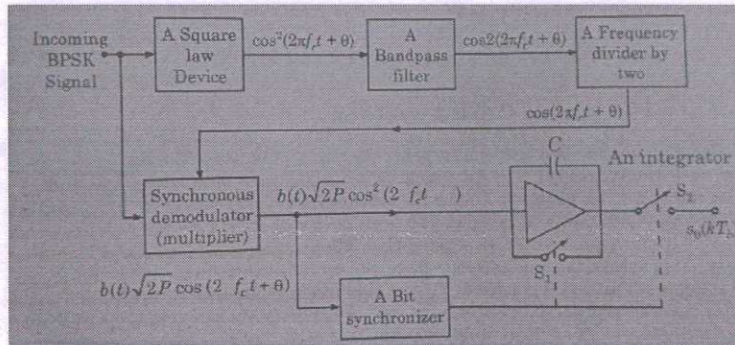


Fig 3 +
Exp 3

6

6

In BPSK receiver, the first step is to recover the carrier signal from the received signal. For this, the received signal is squared and the dc component is removed using a BPF. The output of BPF is given to a frequency divider to regenerate the waveform $\cos(\omega_c t + \theta)$. The recovered carrier is now multiplied with the received signal using a synchronous demodulator whose output is fed to an integrate and dump circuit. The bit synchronizer leaves the switch S1 open during the entire bit interval and closes it at the end of bit interval. The output is made available by switch S2 which samples the capacitor voltage prior to closing of switch S1.

7

Digital Signature

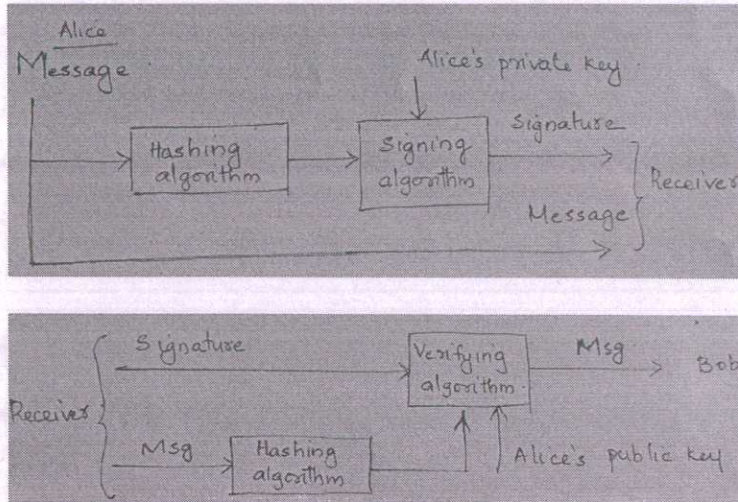
Let M be the message to be signed. Instead of signing the whole message, a digest is made out of the message using hashing algorithm. The sender then signs the hash of the message (message digest) using a signing algorithm and the sender's private key. The message and the signature is then sent to the receiver.

At the receiver side, a digest is first created using the same hashing algorithm. The received signature is then verified using verifying algorithm and sender's public key. If authentic, is accepted else rejected.

Fig 3 +
Exp 3

6

6



III PART - C
(a)

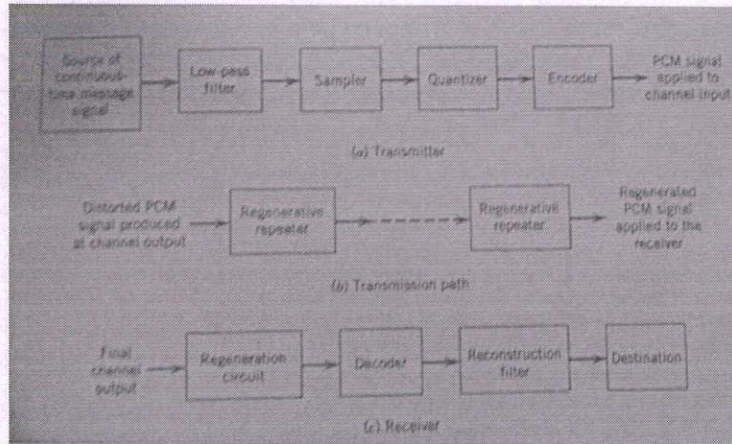


Fig 4 +
Exp 6

10

In PCM, a message signal is represented by a sequence of coded pulse. This is achieved by representing the signal in discrete form in both time and amplitude.

At the transmitter, the message signal is passed through a low pass filter. This is done to bandlimit the signal to prevent aliasing. The bandlimited signal is then given to a sampler which samples the signal according to Nyquist criteria. The discrete time signals at the output of the sampler is then given to a quantizer to convert it to a digital signal. The quantized samples are then represented as a sequence of symbols appropriate for transmission in the encoder.

The regenerative repeater in the transmission path consists of an equalizer, decision making device and a timing circuit. The equalizer removes the amplitude and phase distortion introduced by the channel. The timing

15

	<p>circuit generates the sampling pulses. Each sample is compared with a threshold value in the decision making device. If the sampled value is greater than the threshold value symbol 1 is transmitted else symbol 0 is transmitted.</p> <p>The PCM receiver consists of a regeneration circuit and a decoder. The decoded signal is given to the reconstruction filter to reconstruct the original message signal.</p> <p>(b) The two major sources of noise in PCM system are</p> <ol style="list-style-type: none"> 1. Channel noise 2. Quantization noise <p>Channel noise: It is introduced anywhere between the transmitter output and receiver input. Channel noise introduces bit errors into the received signal (symbol 0 to be mistaken for symbol 1 and vice versa). The presence of channel noise is measured in terms of average probability of symbol error (BER – bit error rate)</p> <p>Quantization noise: It is introduced in the transmitter (quantizer) and is also known as quantization error. The quantization noise can be reduced by increasing the number of representation levels in the quantizer.</p>	2.5×2	5	
<p>IV (a)</p>	<p>The difference between the input signal 'm' and the output signal 'v' of a quantizer is known as quantization noise or quantization error.</p> <p>In a non-uniform quantizer, the representation levels are non-uniformly spaced. In certain applications such as telephonic communication, it is preferable to use non-uniform quantizer. The use of non-uniform quantizer is equivalent to passing the signal through a compressor and then applying the compressed signal to a uniform quantizer. The compression laws that are used in practice are</p> <ol style="list-style-type: none"> 1. μ- law 2. A- law: <p>To restore the signals to their correct relative level a device is used at the receiver. It has characteristics complementary to the compressor. Such a device is called an expander. The combination of compressor and</p>	$2 + 4 + 2$	8	15

expander is called compander and the process is called companding.

(b)

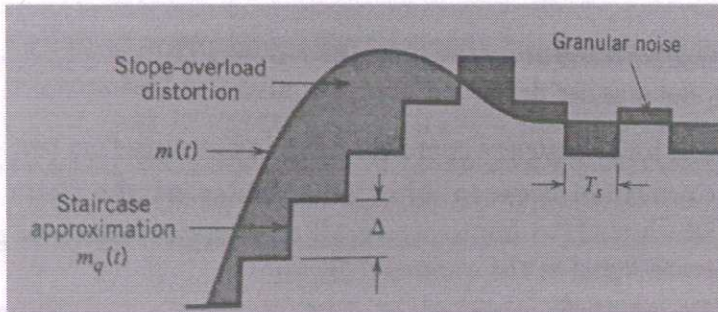


Fig 3 +
Exp 4
(2+2)

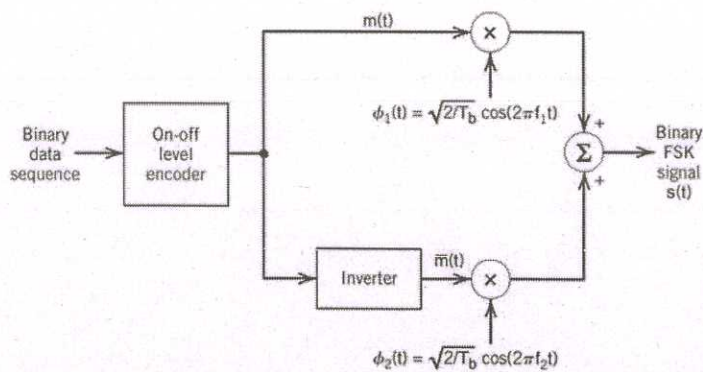
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In delta modulation, if the step size Δ is too small, then it is difficult for the staircase approximation to follow a steep segment of the input waveform resulting in large quantization error. This quantization error is called slope overload distortion.

If the step size Δ is too large then, the approximation will hunt around a relatively flat segment of input waveform. This error is known as granular noise.

V
(a)

In BFSK, the frequency of the carrier is shifted according to the binary symbol. Symbol 1 is represented using frequency f_1 and symbol 0 is represented using frequency f_2 .

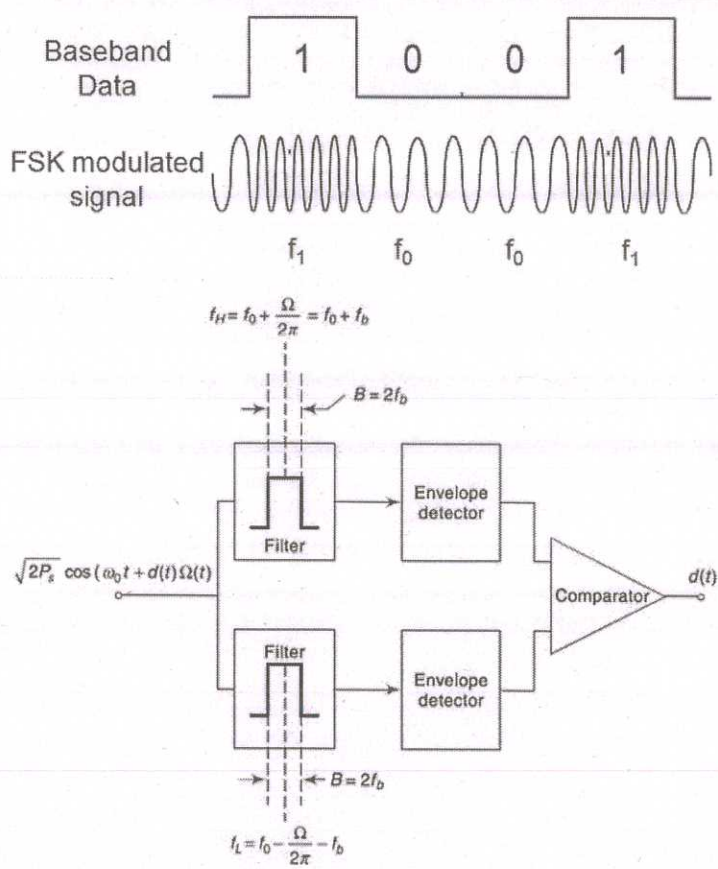


5 (Fig
2 + Exp
3)
+ 5 (Fig
2 + Exp
3)

10

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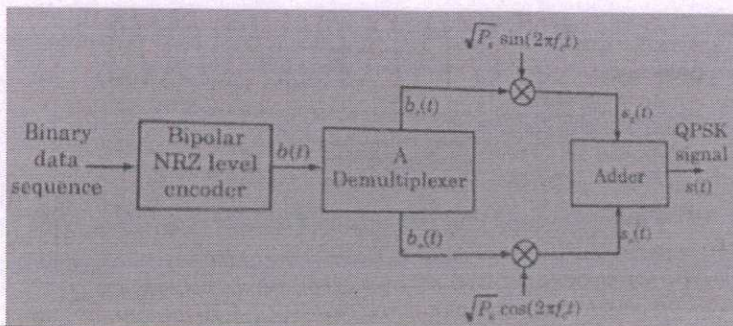
Transmitter: The incoming binary sequence is given to an on-off level encoder. At the output of the encoder, symbol 1 is represented using a constant amplitude and symbol 0 is represented using zero volts. For symbol 1, upper channel is switched on and the frequency f_1 is transmitted. For symbol 0, the lower channel is switched on and frequency f_2 is transmitted.



Non-coherent detection of BFSK

In non-coherent detection, carrier signal is not generated at the receiver. The received signal is applied to two bandpass filters, one tuned to frequency f_1 and the other tuned to frequency f_2 . Each filter is followed by an envelope detector. The resulting outputs of the two envelope detectors are sampled and compared. If $x_1 > x_2$, $y = 1$
 $x_1 < x_2$, $y = 0$.

(b)

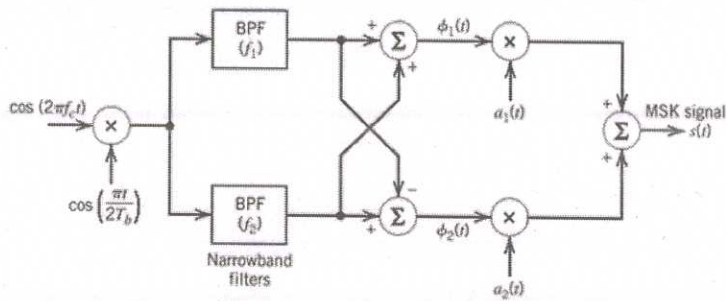


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5

VI
(a)

MSK transmitter

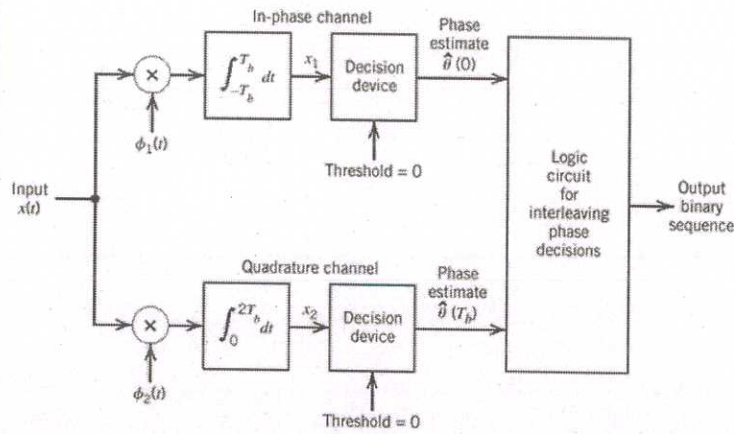


The waveform of MSK exhibits phase continuity that is there is no sudden changes in phase as in QPSK. In the transmitter, two sinusoidal signals are multiplied. The bandpass filter passes only the sum and difference frequencies. The outputs of the BPFs are then added and subtracted such that two signals $\phi_1(t)$ and $\phi_2(t)$ are generated. $\phi_1(t)$ is multiplied with the odd sequence and $\phi_2(t)$ is multiplied with the even sequence. The outputs of the multipliers are then added to generate the MSK signal.

5 (Fig 2 + Exp 3) + 5 (Fig 2 + Exp 3)

10

MSK receiver



At the receiver, the received MSK signal is multiplied with $\phi_1(t)$ and $\phi_2(t)$. The output of the multiplier is the even sequence and the odd sequence. The integrator integrates the output over the period $2T_b$. The decision device samples the integrator output and decides whether the signal is +1 or -1. The logic circuit interleaves the two outputs to form the original binary sequence.

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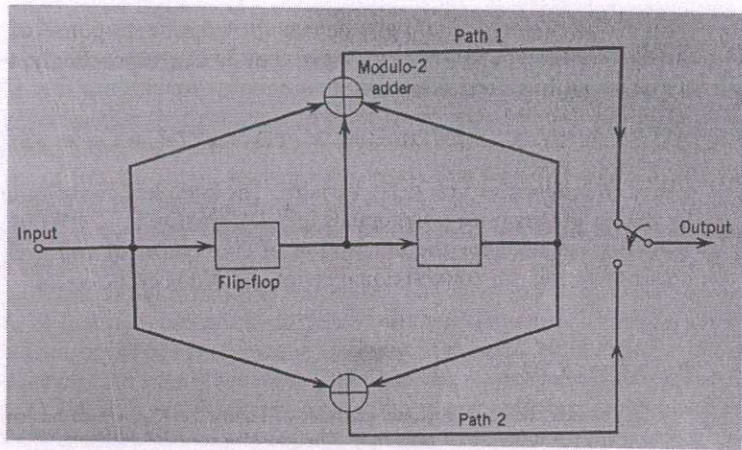
(b)

Advantages of MSK compared to QPSK

1. MSK waveforms are smoother compared to QPSK

	<p>2. MSK has continuous phase whereas, QPSK has sudden phase shift of π or $\pi/2$.</p> <p>3. Side lobes of MSK are smaller</p> <p>4. QPSK requires band pass filtering, whereas it is not required in MSK</p> <p><u>Disadvantages</u></p> <p>1. The generation and detection of MSK is slightly complex.</p> <p>2. The bandwidth requirement of MSK is $1.5f_b$. Bandwidth of QPSK is f_b</p>	1×5	5	
VII (a)	<p>The average information per source symbol of a discrete memoryless source is called entropy</p> <p>Consider a source emitting 'k' symbols x_1, x_2, \dots, x_k with probabilities $p(x_1), p(x_2), \dots, p(x_k)$. In a large sequence of 'L' messages, the number of occurrence of x_1 is $p(x_1)L$.</p> <p>The total amount of information of all x_1 messages = $p(x_1)L \times I(x_1) = p(x_1)L \log(1/p(x_1))$</p> <p>The total information in all L messages = $I = p(x_1)L \log(1/p(x_1)) + p(x_2)L \log(1/p(x_2)) + \dots + p(x_k)L \log(1/p(x_k))$.</p> <p>The average information per symbol = $H(x) = I/L = p(x_1)\log(1/p(x_1)) + p(x_2)\log(1/p(x_2)) + \dots + p(x_k)\log(1/p(x_k))$</p> $= \sum_{i=1}^k p(x_i)\log(1/p(x_i))$	$2 + 6$	8	15
(b)	<p>In single parity bit method, a parity bit (odd / even) is added to each block of message. In case of even parity, the final code word will have even number of ones, whereas in odd parity the code word will have odd number of ones. At the receiver, the number of ones in the received code word checked. If a single bit error has occurred due to channel noise, then the error is detected. If the error occurs in two bits, then it cannot be identified since the number of ones in the code word will remain the same.</p> <p>Give an example</p>	Exp 4 + Examp e 3	7	

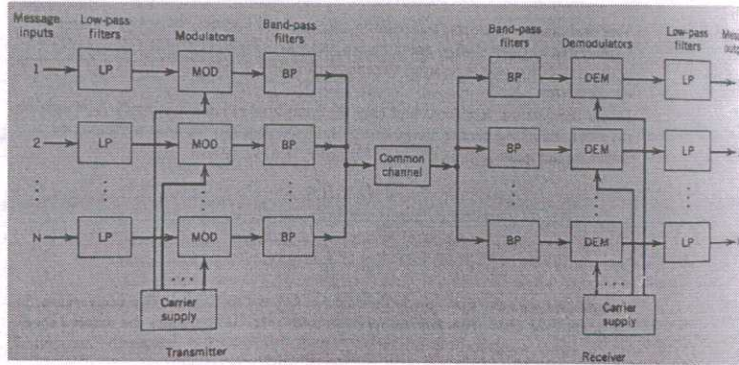
<p>VIII</p> <p>(a)</p>	<p>A family of (n, k) linear block codes with</p> <ol style="list-style-type: none"> 1. Block length $n = 2^m - 1$ 2. Number of message bits $k = 2^m - m - 1$ 3. Number of parity bits $n - k = m$ <p>where $m \geq 3$ are called Hamming codes.</p> <p>Hamming code will have a generator matrix G and a corresponding parity check matrix H. At the transmitter, each message block is multiplied by the generator matrix to generate the corresponding code word C and these code words are transmitted. The receiver will have a decoding table for the Hamming code defined with the error patterns and their corresponding syndrome as entries. The error correction procedure is as follows:</p> <ol style="list-style-type: none"> 1. For the received vector r, compute the syndrome $s = rH^T$. 2. If there are no transmission errors, then the syndrome will be zero or the received vector r is the transmitted code word 3. Else, identify the error pattern e corresponding to the syndrome from the decoding table. 4. Compute the code vector $c = r + e$ 	<p>3 + 7</p>	<p>10</p>	<p>15</p>
<p>(b)</p>	<p>The constraint length of a convolutional code, expressed in terms of message bits, is defined as the number of shifts over which a single message bit can influence the encoder output.</p>	<p>2 + Fig 3</p>	<p>5</p>	<p>15</p>



<p>IX (i)</p>	<p>Message switching:</p> <p>Consider that computer A needs to transmit data to computer B. Communication consists of short messages separated by long intervals. Suppose that the transmission path selected is A-X-Y-Z-B. Lines from X-Y and Y-Z can be used as part of connection between many other computers. Computer A will transmit message to switching center X where it is stored in a buffer. When the line from X –Y becomes available, the message will be transmitted from X to Y. Again, after storage and a possible delay the message will go from Y to Z and then to computer B. Since the system involves storing and forwarding of the messages, a message switched network is referred to as store and forward network.</p> <p>Adv: At any particular time, no complete connection is needed between the communicating parties. Only one of the lines between switching computers will be involved with that message and other lines can handle other messages between other computers.</p> <p>Disadv: There will be a delay between the time of transmission and the time of reception of a message If the message duration is T_m and it must be relayed R times, even ignoring the waiting time, the delay is RT_m.</p> <p>No provision to interrupt long message briefly to allow transmission of a short message. Therefore short messages may be delayed for a long time.</p> <p>Packet switching:</p> <p>In a packet switched network, the message is divided into packets. Each packet consists of a source address, destination address and a sequence number. A typical packet is 1024 bits long. The message is transmitted packet by packet. Each packet is stored in buffers at the nodes and then forwarded. Different packets of a single message may arrive at a destination by different routes, with different delays and out of order. At the destination, the packets are ordered based on their sequence number and depacketized.</p> <p>Disadv: To transmit a given amount of information in unit time, packet switching requires a higher data rate due to the overhead data</p>	<p>3×5</p>	<p>15</p>	<p>15</p>
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The switching hardware should packetize, add overhead, depacketize and reassemble the data. This is a complex process.

Frequency Division Multiplexing:



Each signal input is passed through a low pass filter to remove the insignificant high frequency components. The filtered signals are applied to modulators. The other input to the modulator is carrier signal from the local oscillator. The local oscillator frequencies are chosen such that the frequency band of output of one modulator will not interfere with frequency band of output of other modulators. The bandpass filters following the modulators are used to restrict the band of each modulated wave to the prescribed range. The bandpass filter outputs are combined in parallel to form the input to the common channel.

At the receiving terminal, a bank of bandpass filters, with their inputs connected in parallel is used to separate the message signals. The original message signals are recovered using individual demodulators and a low pass filter.

**X
(a)**

ARQ is used when extremely low error rates are required. The receiver only detects the errors. When an error is detected in a code word, the receiver signals back the transmitter and the word is transmitted again. Thus in an ARQ system a feedback channel must be provided. The 3 basic ARQ systems are

1. Stop – and –wait ARQ
2. Sliding window / go – back – N ARQ
3. Selective repeat / selective reject ARQ

Fig 3 +
List 1 +
Exp 6
(2 × 3)

10

15

Stop – and – wait ARQ:

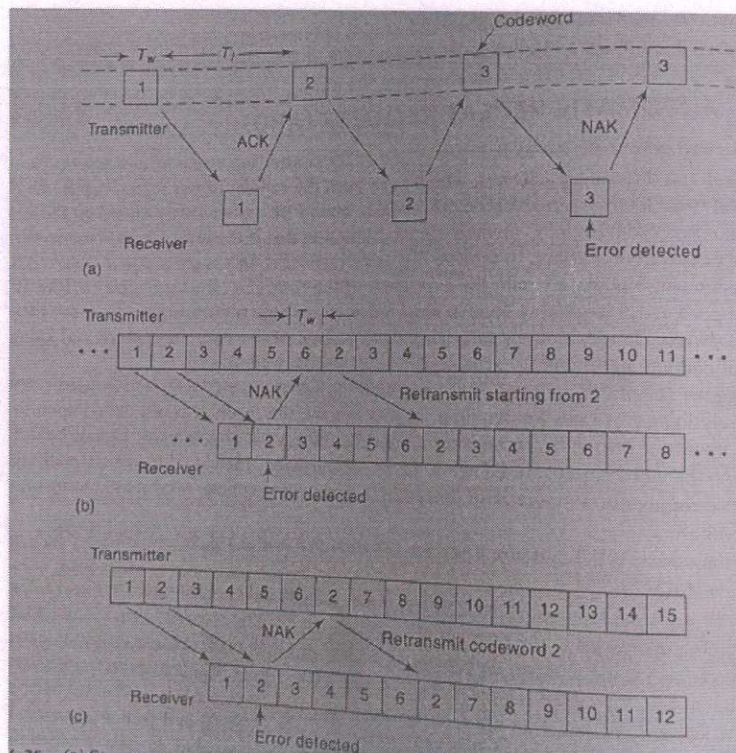
It is the simplest to implement ARQ system. The transmitter sends a code word and waits for the response from the receiver. The receiver checks for error in the received code word. If no error is detected, it sends back the transmitter a positive acknowledgement (ACK) or else a negative acknowledgement is transmitted (NAK). If ACK signal is received, the next code word is transmitted. Else, the transmitter sends the same code word and waits for an acknowledgement before further transmission.

Sliding window:

The transmitter sends messages one after another without delay and does not wait for an ACK signal. Whenever the receiver detects an error, say code word i , a NAK signal is send to the transmitter. The transmitter now returns to that code word i and starts all over again at that word.

Selective repeat ARQ:

The transmitter sends messages one after another without waiting for ACK after each message. When the receiver detects an error in code word say i , it signals the transmitter. The transmitter retransmits the code word i and thereafter returns immediately to its sequential transmission. This system has the highest transmission efficiency but is the most costly to implement.



(b)	<p>RSA algorithm</p> <ol style="list-style-type: none"> 1. Select two large prime numbers p and q, $p \neq q$ 2. Compute $n = p \times q$ 3. Compute $\phi(n) = (p-1)(q-1)$ 4. Select 'e' such that $1 < e < \phi(n)$ 5. Find $d = e^{-1} \text{ mod } \phi(n)$ <p>Public key (e, n) Private key (d)</p> <p>RSA encryption: $C = M^e \text{ mod } n$ RSA decryption: $C^d \text{ mod } n = M$ C: cipher text M: Message</p>	3 + 2	5	
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