SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: TED(15)-6041 DIPLOMA IN ELECTRONICS

Course Title: ADVANCED MICROPROCESSORS

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	PART - A			
I 1.	It's data bus width as well as size of it's internal data registers is 16.	2		
2.	Code segment	2		
3.	Sets carry flag, means after executing STC, carry flag = 1.	2		
4.	Local Descriptor Table (LDT) and Global Descriptor Table (GDT)	1+1	2	
5.	A core is a part of CPU that receives instructions and performs calculations based on those instructions.	2		5x2= 10Marks
	PART - B			
II 1.	Stack Segment = 5555 H → Segment base address.			
	Stack pointer = 1100 H → offset address.			
	physical address = 10x Base address + Offset			
	1. Left shift the 16 bit address in the segment by 4 bits.			
	5555 ⇒ 0101 0101 0101 0101 (0000)			
	2. Add the 16 bit offset address to this shifted base address.			
	So 1100 ⇒ 0001 0001 0000 0000			
	physical address is ;			
	0101 0101 0101 0101 0000 +			
	0001 0001 0000 0000			
	0101 0110 0110 0101 0000			
	Answer is ⇒ 56650 H			

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

Course Title: Advanced Microprocessors

Qn No:	Scoring Indicator	Split up score	Sub total	Total
2.	1. SHL dest, count → Shift logical left by 'count' bits 2. SAL dest, count → Shift arithmetic left by 'count' bits 3. SHR dest, count → Shift logical right by 'count' bits 4. SAR dest, count → Shift arithmetic right by 'count' bits 5. RCL dest, count → Rotate through carry left by 'count' bits 6. RCR dest, count → Rotate through carry right by 'count' bits 7. ROL dest, count → Rotate left by 'count' bits 8. ROR dest, count → Rotate right by 'count' bits. 9. SHL BX, 1 → shift left logical by one position, the word in BX 10. SAL AL, CL → Shift left arithmetic AL, by the count specified in CL (Write any 6 of the above)	1 x 6 = 6	6	6
3.				

D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
X	X	X	X	OF	DF	IF	TF	SF	ZF	X	AC	X	PF	X	CF

X → Reserved for future use.

CF - Carry Flag sets if there is a carry out from the MSB bit during a calculation.

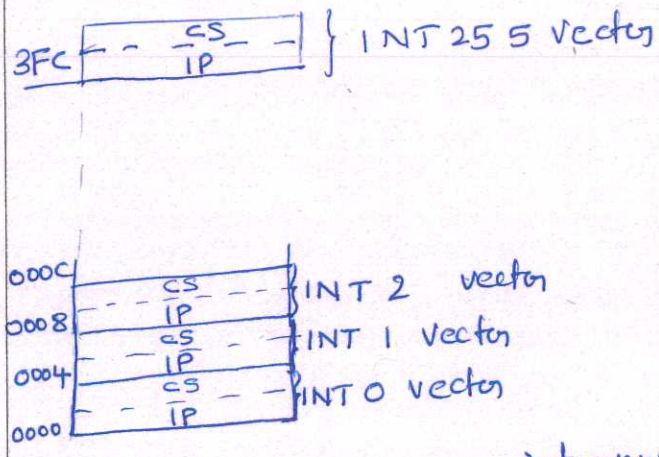
ZF - Zero Flag → when the result of an arithmetic or logic operation is zero, the zero flag gets set.

PF - Parity Flag → Setting of this flag indicates the presents of even no: of bits in the lower 8 bits of the destination.

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

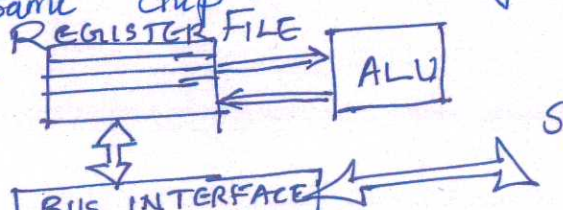
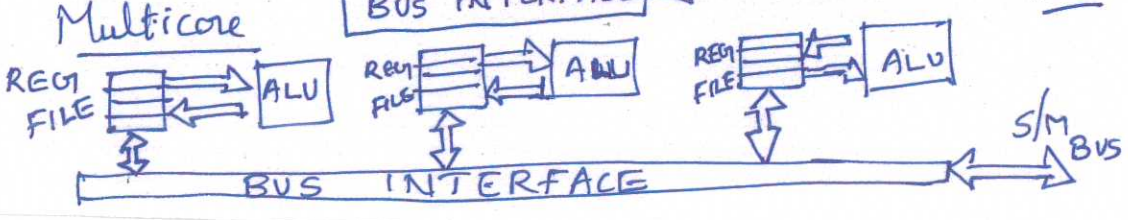
Course Title: Advanced Microprocessors

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	Sign Flag - SF - After an arithmetic or logic operation if the result contains a negative number the sign flag is set. ACF - Auxiliary Carry Flag - It is set when there is a carry out from lower nibbles (4 bits). OF - Overflow Flag → Set when there is an overflow into the MSB (8th or 16th bit). (This Flag indicates that the result of a signed number operation is too large, causing the highest order bit to overflow into the sign bit.) Diagram → 3 explanation → ½ × 6 = 3		6	6
4	Interrupt Vector table of 8086  8086 has 256 interrupt vectors. Each vector is specified by 4 bytes => 256 × 4 = 1024 bytes (1K) of memory are allocated to store the interrupt vectors. The 256 vectors are stored in a table called the 'Interrupt Vector table'			

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: G041

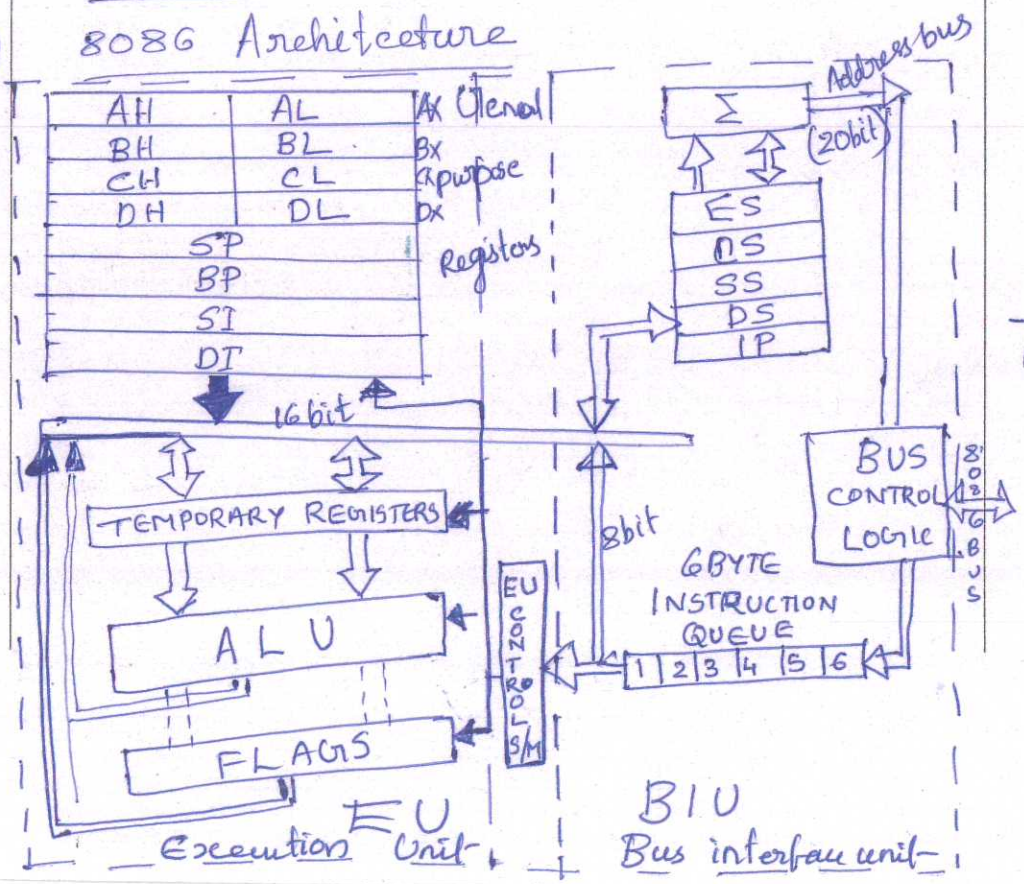
Course Title: Advanced Microprocessors

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	It is stored in RAM locations from 00000H to 003FFH. The interrupts are numbered from 0 to 255, also called type of interrupt. It multiplies the type number by 4, gets the address of its interrupt vector and loads IP and CS with these new values and starts executing ISR it has located.	Diagm → 3 explo. → 3	6	6
5.	1. 32 bit microprocessor 32 bit address and 64 bit data bus. 2. Super Scalar Architecture Two pipelined integer units and1 floating point unit, capable of 'less than' 1 clock / instruction 3. Separate code and data caches. 8K code cache, 8K write back data 4. Advanced design features. Branch prediction.	1½ × 4 = 6	6	6
6.	Single core → A CPU chip with one CPU. microprocessors have been single core since their inception. Multi core → is usually the term used to describe 2 or more CPUs working together on the same chip. Single Core  Multicore 	6 Explan 3 + Diagm 3	6	6

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

Course Title: Advanced µp

Qn No:	Scoring Indicator	Split up score	Sub total	Total
7.	The 80386 can operate in real mode as well as in protected mode. On start up processor is in real mode. In real mode it acts as a faster 8086. Speed increases due to increased clock speed and hardware enhancements. In real mode it can use enhanced instructions. It can use 32 bit register and data bus, and so the B.W. is double that of 8086. Main feature of real mode is that it has access to only 1MB of physical memory. Address calculation is done as in 8086. Register available in real mode is all reg's of 8086 + new reg.s of 80386 ie FS, GS, debug control and test regs.	6	6	6
	PART C			
III a)	8086 Architecture  	7	7	7

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

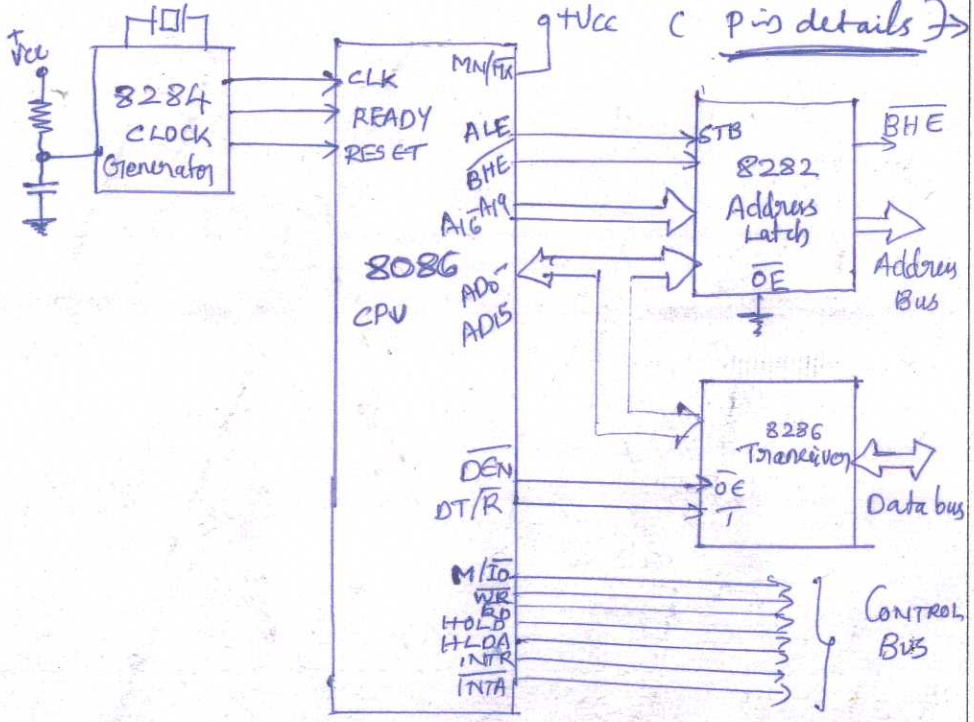
Course Title: Advanced MP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
III b)	Pins in maximum mode;			
	31) $\overline{RQ}$ / GT0 30) $\overline{RQ}$ / $\overline{GT_1}$ 29) $\overline{LOCK}$ 28) $\overline{S_2}$	~~→1~~		
	27) $\overline{S_1}$ 26) $\overline{S_0}$ 25) QS0 24) QS1			
	RQ/GT → Request/ grant pins (Pins 30,31)			
	It is used in multiprocessor configurations. when one processor is using the bus, another processor may request the bus. The request from other proc. is placed on these lines and grant s/l is also placed on these pins. If bus request is placed on both pins, the pin $\overline{RQ_0}$ / $\overline{GT_0}$ gets the priority.	→2		
	$\overline{LOCK}$ (Pin 29) → o/p s/l from 8086. If this processor wants to prevent any other bus master from accessing the bus, this s/l will be asserted low.	→2		
	Status signals $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ (pins 28,27,26)			
	$\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ — control s/l generated 0 0 0 — Interrupt acknowledge ($\overline{INTA}$) 0 0 1 — I/O Read ($\overline{IORC}$) 0 1 0 — I/O Write ($\overline{IOWC}$) 0 1 1 — HALT — 1 0 0 — Instruction fetch $\overline{MRDC}$ 1 0 1 — Memory Read $\overline{MRDC}$ 1 1 0 — Memory Write $\overline{MWTC}$ 1 1 1 — Inactive —	→2		
	Queue Status pins QS0, QS1 (pins 25,24) → i/p pins to 8086.	→2	8	8
	It is useful when a arithmetic co-processor is used in the s/m. The co-processor can interrogate the 8086 about its queue status, on these lines, and decide its course of action accordingly.			

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

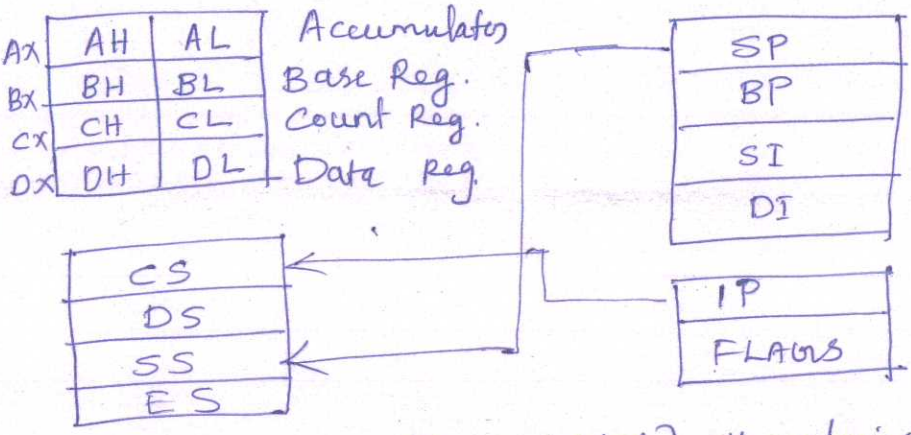
Course Title: AMP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
IV a	→ For minimum mode operation pin 33 MN/$\overline{MX}$ is tied at logic high. → pins 24 to 31 have dual functions. → $\overline{INTA}$, ALE, $\overline{DEN}$, DT/$\overline{R}$, IO/$\overline{M}$, $\overline{WR}$, HLDA, HOLD +Vcc & Pin details → 2			
				
	Diagram → 5	5	7	7
b.	Register Set of 8086 Scratchpad Registers: 8086 has 4, 16 bit general purpose regs labelled as AX, BX, CX, DX. Each of them can also be used as two 8 bit Regs Eg: AX → has two parts AH + AL (16 bit; 8 bit, 8 bit.) AX is the accumulator Reg. For certain special instructions only AX is used. BX → is frequently used as address reg in many based addressing modes. CX → used as counter DX → used in I/O instruction as a pointer to data			

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

Course Title AMP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	Pointer & Index Registers: SP, BP, SI & DI BP and SP are Base & Stack pointer. SI and DI are index registers labelled as ↳ Soure Index & Destination Index. They fun as address registers in various addressing modes. ↳ used as default reg in string instructions  IP - Instruction Pointer (16 bit) It contains the the address of next instruction to be executed. Logical address for an instruction byte is CS:IP form Four Segment Registers: Code seg, Data seg, Stack seg and extra segment. CS → segment of memory where code is stored Code Seg. Reg contains the base address of Code Segment. DS → Data Segment ES → Extra Segment SS → Stack Segment Block diagram each section Flag Register: 16 bit register Conditional Flags available are, CF, ZF, PF, AF, SF, TF, IF, DF, OF	2×4 =	8	8

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 604 Advanced MP

Course Title

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	UNIT - II			
Va.	1. MOV dest, src → copy the contents of source to dest. 2. LEA reg16, mem → Load the offset of mem to reg16 3. XCHG dest, src → Exchange contents of dest & src 4. PUSH src → Transfer one word from src to stacktop 5. POP dest. → Transfer word at current stacktop to dest. 6. LDS reg16, mem → Load to DS & register. 7. LES reg16, mem → Load to ES & register. 8. LAHF → copy bits of 0-7 of Flag reg into AH 9. SAHF → Transfer 0-7 bits of AH into Flags. 10 PUSHF → Push Flag Reg onto Stack 11 POPF → POP word from Stack into Flags 12. XLAT → Replaced the byte in AL with byte (Translate) from a usertable addressed by BX Any 10 →	1x10	10	10
Vb.	Assembler is a software that translates assembly language into machine code on a 1-1 basis ASSUME - ASSUME directive tells the assembler the names of the logical segment to use as the physical segment. Eg: ASSUME CS : CODE, DS : DATA ENDS : → This assembler informs the assembler about the end of a segment. Eg : ENDS code , ENDS data. DB → Define byte. It implies allocating space for data. DB defines a data byte. DW → DW defines a data word. ENDP → End of a procedure. The PROC directive is used with ENDP to 'bracket' a procedure.	1x5	5	5
				15

SCHEME OF VALUATION
(Scoring Indicators)

Revision: 2015 Course Code:

Course Title: 6044

QN NO:	Scoring Indicators	Split up Score	Sub Total	Total
VIa	Two pins on which interrupts can be received → 1) INTR 2) NMI	1.		
	NMI : → +ve edge triggered interrupt. This is a non-maskable interrupt. It does not depend on IF flag. It is a Type 2 interrupt. Highest priority interrupt.	3		
	INTR : → non-vectored interrupt. IF is required to set for an interrupt request on INTR to be honoured (by STI instruction). On being interrupted, the processor goes to an 'INTA' to occur. INTR is a highly level triggered interrupt.	3	7	7
	Priority 1) Software interrupts 2) NMI 3) INTR.			
	→ Interrupt response steps may be included.			
VIb	Interrupt Response of 8086. (ISR)			
	1. save the current pgm. Flag Reg. is pushed onto Stack for later retreival.			
	2. IF is disabled → for ensuring interrupt routine does not get interrupted by other s/ls on INTR line.			
	3. TF is disabled → for ensuring the pgm does not stop after step by step execution.	1 mark each		
	4. CS Register is pushed onto stack	1X8		7+
	5. IP " is pushed onto stack. ↳ both IP & CS are saved, because the new pgm will be in a different code segment.	=8	8	8 = 15
	5. Control is transferred to the location in which the 'ISR' is stored. ISR is executed to Last 'IRET' instruction.			
	6. IP & CS is popped off the stack. Thus address of next instruction is back in the required reg.s.			
	7. Flag Reg. is popped off the stack → Flag status is restored.			
	8. Finally instruction execution resumes from where it had been diverted.			

SCHEME OF VALUATION
(Scoring Indicators)

Revision: 2015 Course Code: 6041

Course Title: AMP

QN NO:	Scoring Indicators	Split up Score	Sub Total	Total

VII a **Paging**: Method of writing data to, and reading it from, 2° storage for use in 1° storage (main memory). any segment can have number of pages.

Address Translation in paged mode — Definition → 2

Logical address from a pgm is converted into a 'Linear address' by segmentation unit, and given to paging unit. This linear address is translated to a 'physical address'. If paging is activated; a 32 bit linear address is composed of;

1) A 10 bit field → DIR → points to a page descriptor in a page directory.
2) A 10 bit PAGE field → used as an index into page table determined by page directory
3) A 12 bit offset → points to required byte with page located

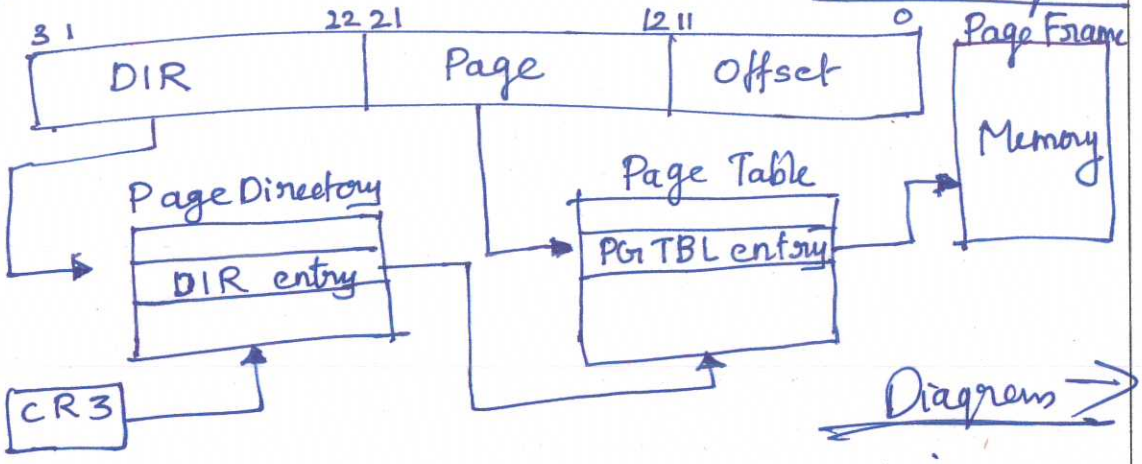


Diagram → 5

→ Base address of current page directory → CR3

A page → is a 4K byte unit of continuous address of physical memory

explanations → 3 — 10

VII b. **5 features of Pentium-Pro**

1. Super pipelining → increases no: of execution steps to 14, from Pentiums 5.
2. Integrated Level 2 Cache
3. 32 bit Optimisation
4. Wider Address bus
5. Creates Multiprocessing

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

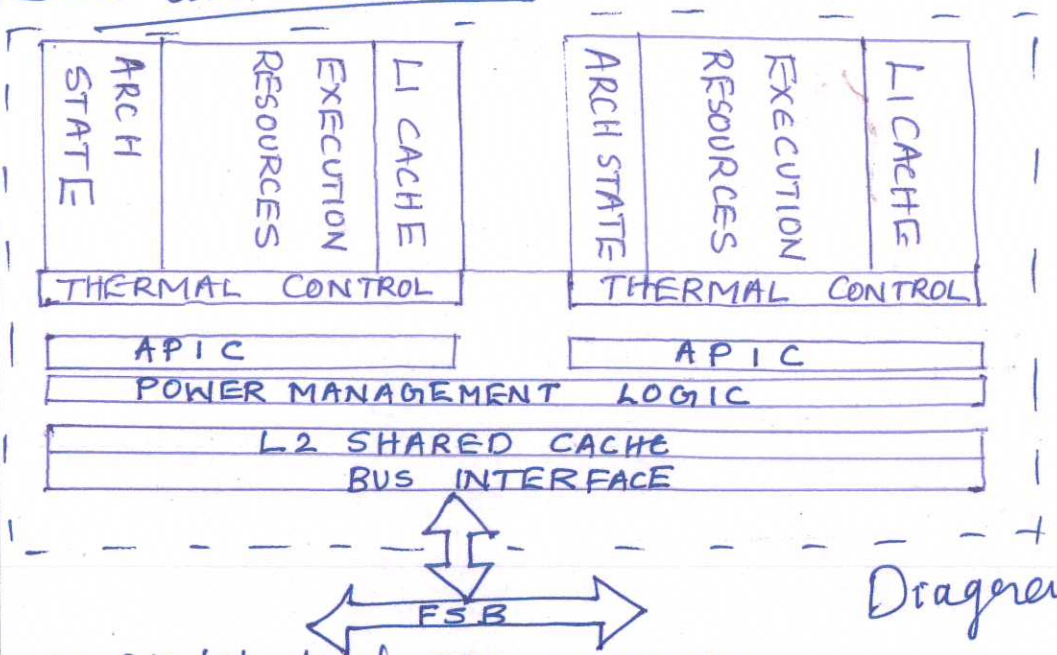
Course Title: AMP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
	6. Out of order completion 7. Superior Branch prediction unit. 8. Register Renaming 9. Speculative Execution Write any 5	1X5	5	15
VIII a)	1. Real mode operation. 2. Protected virtual addressing mode (PVAM) 3. Virtual 8086 mode.	→ 1		
	1. Real mode : In real mode 386 acts as a faster 8086. speed increases due to high clk speed and hardware enhancements. It can use 32bit reg & databus, also BW is double that of 8086. → It has access only to 1MB of memory. → Reg set available in this mode includes all reg. for 8086 + FS&GS, debug Reg., control & Test Regs	3		
	2. PVAM : → concept of virtual memory. In PVAM mode give brief details on; i) Memory Management unit. → Address Translation using paging (brief explanation only) ii) Protection iii) Multi tasking iv) Exceptions & Interrupts	4		
	3. Virtual 8086 mode : This mode divides the computer into multiple address spaces and maintains virtual reg.s for each virtual machine. → entered thru VM bit in EFlags Reg	2	10	

SCHEME OF VALUATION
(Scoring Indicators)

Revision: 2015 Course Code: 6041

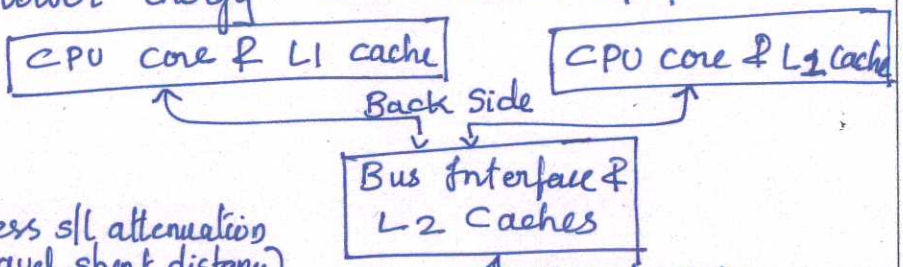
Course Title: A M P

QN NO:	Scoring Indicators	Split up Score	Sub Total	Total
VIII b	Features of 80386 : 1. External, internal data bus 32 bits wide and 32 bit registers. 2. 32 bit address bus. 2^{32} or 4GB addressing capability 3. Scaled addressing mode is available. 4. A set of bit manipulation instruction is available. 5. It can switch from protected mode to real mode without a hardware set also it has 'Paging Mode'.	1 x 5	5	15
IX a	Intel Core-2-duo Processor.  Diagram ↳ 64 bit dual core processor. ↳ 2 processor cores work inside a Core 2 Duo in parallel ↳ Dual core processor with shared Level 2 cache. ↳ Execution Disable bit ↳ Partially Intel Virtualization Technology (VT) ↳ Socket M (starting from Santa Rosa Packet P) ↳ 291 Million transistors. Brief explanation of block diagram also	4 3	7	

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 6041

Course Title: AMP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
~~IX~~ b	↦ The proximity of multiple CPU cores on the same die allows the 'cache coherency' circuitry to operate at a higher clock rate. ↳ multicore CPU designs require less PCB space ↳ Also uses less power than two coupled single core processors. ↳ each core independtly implements optimization such as superscalar execution, pipelining and multithreading. ↳ multicore design can make use of proven CPU core library designs and produces a lower design risk product. ↳ Multi core chips allow higher performance at lower energy. (Used in mobile, Laptops etc) ↳  ↳ Less s/l attenuation (Travel short distance) ↳ Explains Multithreading (Minimum 8 points).	1×8	8	15
X a.	Hyper threading : ↳ This is intel's proprietary simultaneous multithreading (SMT) implementation used to improve parallelization of computations performed on X86 µp. ↳ Hyper threading can be properly utilized only with an OS specifically optimized for it. → Multithreading is the ability of an OS to execute different parts of a program, called threads, simultaneously.	5	5	

SCHEME OF VALUATION
(SCORING INDICATORS)

Revision: 2015 Course Code: 604

Course Title: AMP

Qn No:	Scoring Indicator	Split up score	Sub total	Total
X b.	Comparison of Core i_3, i_5 and i_7 processors			

Feature	Core i_3	Core i_5	Core i_7
No: of cores	2	4	4
clock speed	3.4 GHz - 4.2 GHz	2.4 - 3.8 GHz	2.9 - 4.2 GHz
Cache memory	3 - 4 MB	4 - 6 MB	8 MB
Hyper Threading	Yes	No	Yes
Turbo boost	No	Yes	Yes
K model	No	Yes	Yes

Core ~~i5,i3~~ over → First Core i3 launched in 2010.
use less heat and energy as earlier processors.
↳ i5 processors have ability to work with integrated memory. Turbo Technology that boost up the working speed of computational sms.
↳ It provides 64 bit architecture.
↳ i5 over i3 can be explained.

↳ Core i7 processor : Comparatively faster than the old ones.
↳ multitasking.
↳ Dual core technology.
↳ Turbo boost technology & Hyperthreading

↳ i7 over i5 also can be mention.

Comparison table → 4
Explanation on i_3 → 2
i_5 → 2
i_7 → 2 — 10 — 15