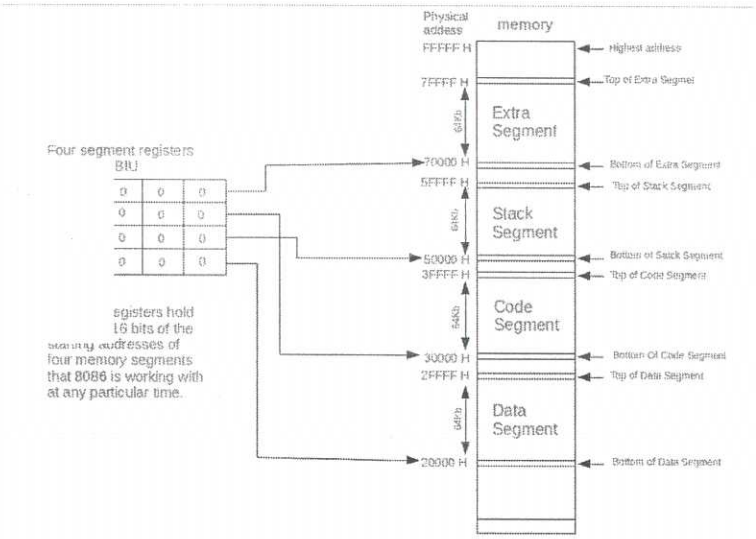
REVISION : 2015 COURSE CODE : 6041

COURSE TITILE: ADVANCED MICROPROCESSORS

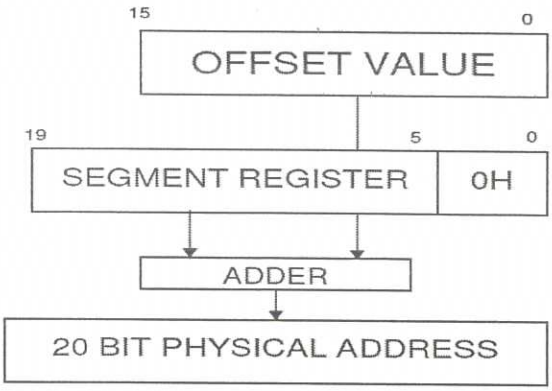
Question no	Scoring indicators	Split up score	Sub total	Total
	PART -- A			
I 1.	The process of fetching the next instruction when the first instruction executes is known as pipelining.	2	2	
2.	Assembler directives are instructions to the assembler regarding the program to be assembled. They are called pseudo instructions.	2	2	10
3.	Real mode, Protected virtual address mode, System Management mode.	2	2	
4.	Less computing capacity, Runs slower than multicore processors	2	2	
5.	If the multiple cores of a multicore processor are of same processing capacity they are called Homogeneous or symmetric cores	2	2	
	PART-B			
II . 1	First 16 bit processor, 40 pin DIP, 16 bit data bus, 20 bit address bus, 1MB physical memory, can operate in Minimum and Maximum modes, Memory segmentation(Any 6 points)	6	6	
2.	General purpose registers AX,BX,CX,DX, Pointer and Index registers SI,DI,BP,SP, Segment registers CS,DS,SS,ES, and IP registers	6	6	
3.	Type 0 Divide by zero interrupt, Type 1 Single step interrupt, Type 2 NMI interrupt, Type 3 Breakpoint interrupt, Type4 overflow interrupt.	6	6	

4.	MOV SI,1100H
	MOV AX,[SI]
	MOV DX,[SI+2]
	MOV BL,[SI+4]
	DIV BL
	MOV [SI+6],AL
	MOV [SI+7],AH
	HLT
		6	6	

5.	In 80386 when paging is enabled, each segment is divided into equal sized pages.The segmentation unit will generate a 32 bit linear address which is converted to a 32 bit physical address.The selector ,descriptor and offset is used for address	6	6	

	calculation. Pages are of size 4Kb.			
6.	Superscalar Architecture, Dynamic branch prediction, pipelined Floating point unit,64 bit data bus, Separate code and data cache ,32 bit processor,32 bit address bus,4GB physical memory.	6	6	
7.	In a multicore processor CPU consists of two or more CPUs that read and execute the actual program instructions. The individual cores can execute multiple instructions in parallel, increasing the performance. In Homogeneous multicore all cores are of similar type. In Heterogeneous multicore all cores are not identical.	6	6	
	PART -- C			
III. a.	 Fig 4 marks+ exp 3 marks			
III. (b)	The 20 bit physical address is calculated by adding the 16 bit segment base address to the offset. The offset address of code segment is stored in IP register. For stack segment it is in SP. For extra and data segment any register can be used.	4 marks		

IV. (a)



4 marks

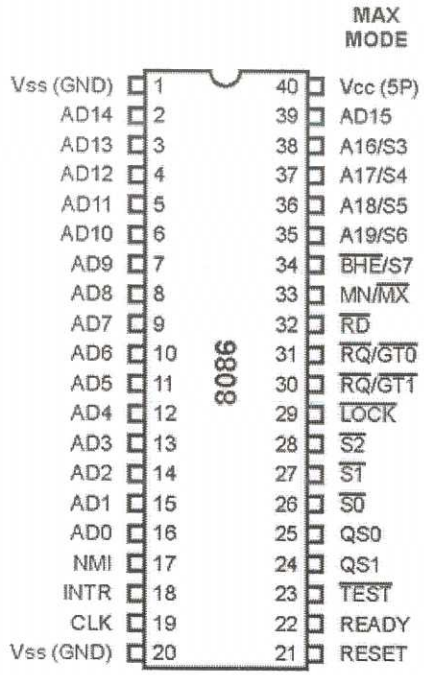
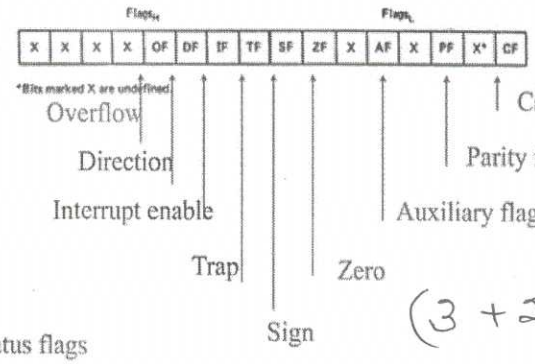
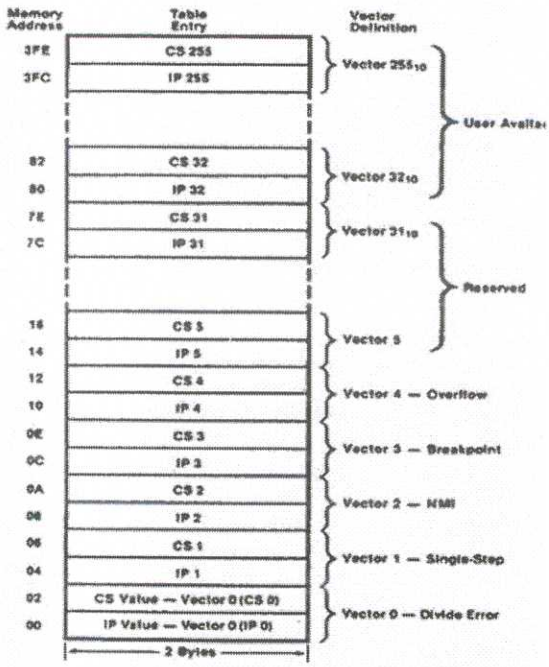
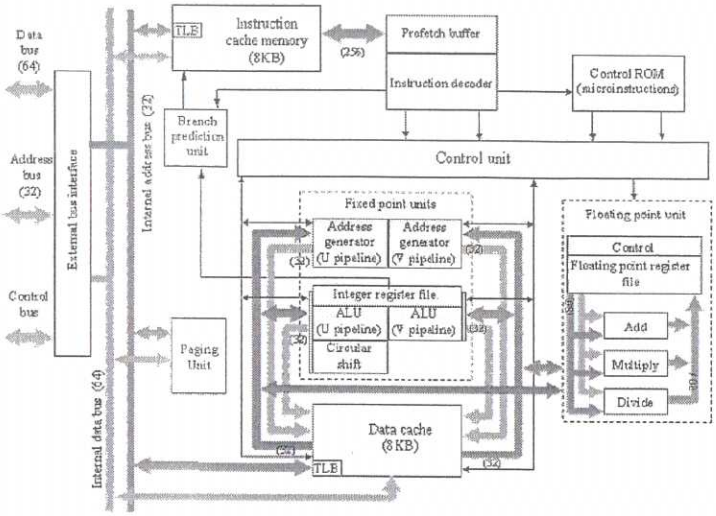


Diagram 5 + Exp 5 Mark

IV (b)	 6 are status flags 3 are control flag	(3 + 2 Marks)		5
V. (a)		fig-4 Exp-3		7
V (b)	8086 checks for interrupt at the end of each instruction cycle. If an interrupt is detected it performs the following operations. 1.SP is decremented by two and content of flag register is pushed to memory. 2.Interrupt flag is disabled 3. SP is decremented by 2 and the CS content is pushed to memory. 4.SP is decremented by two and content of IP is pushed to memory. 5.The processor runs an interrupt acknowledge cycle to find the type and number of interrupt. The address of ISS is got from the interrupt vector table. The ISS is executed. The contents which are pushed to stack is poped back.	8	8	8
(VI)(a)	Register addressing mode, immediate, Direct, Register indirect, Based , Indexed, Based index, string, Relative, Implied, Direct I/O port and indirect I/O port addressing (Any five with eg)	5x2		10

~~VI (a)~~
 	
VI.(b)
	MOV SI,1100H
	MOV AX,[SI]
	MOV BX,[SI+2]
	MUL BX
	MOV [SI+4],AX
	MOV [SI+6],DX
	HLT
		5	5	5

VI I(a)	32 bit processor, 32 bit AB, 32 bitDB, physical memory of 4GB, virtual memory of 64 TB, available in DX and SX versions, supports segmentation and paging, three operating modes	5 Marks		
VII (b)	Three operating modes Real mode, PVAM mode and Virtual 8086 mode. When reset 80386 enters the real mode. In this mode it appears as a fast 8086. The main purpose of this mode is to initialize the system for protected mode of operation. Paging is disabled and physical memory is 1MB only. 80386 enters PVAM when PE bit in control register is set to one. In PVAM mode both Segmentation and Paging are enabled 4GB physical memory and 64 Tb virtual memory space. Each physical address is represented by 48 –bit virtual address. The processor can switch from PVAM to virtual 8086 mode by setting the VM bit in the EFLAG register. The virtual 8086 mode permits the execution of 8086 applications with all protection features of 80386.	10 Mark		
VIII (b)	Three way superscaler architecture, five parallel execution units, 12 stage super pipeline, Dual cavity ceramic package, Out of order execution and speculative execution, error checking and corrective codes, Improved power management, integrated level II cash memory of 256 k/512k/1Mb. Internal thermal protection	5 Ma		

VIII (a)			feg -6 Mar Exp -4		
IX (a)	Hyperthreading allows a Single Processor to execute two threads simultaneously, but not on all conditions. Hyperthreading does not double the performance of a system, it can increase performance by better utilizing idle resources leading to greater throughput for certain important workload types.For each processor core that is physically present, the operating system addresses two virtual (logical) cores and shares the workload between them when possible. The main function of hyper-threading is to increase the number of independent instructions in the pipeline; it takes advantage of superscalar architecture, in which multiple instructions operate on separate data in parallel. With HTT, one physical core appears as two processors to the operating system, allowing concurrent scheduling of two processes per core. In addition, two or more processes can use the same resources: if resources for one process are not available, then another process can continue if its resources are available.		8 Mark		
IX (b)	A multi-core processor is a computer processor integrated circuit with two or more separate processing units, called cores, which each read and execute program instructions, as if the computer had several processors.[1] The instructions are ordinary CPU instructions (such as add,				

		move data, and branch) but the single processor can run instructions on separate cores at the same time, increasing overall speed for programs that support multithreading or other parallel computing techniques.[2] Manufacturers typically integrate the cores onto a single integrated circuit die(known as a chip multiprocessor or CMP) or onto multiple dies in a single chip package. The microprocessors currently used in almost all personal computers are multi-core.	7		
X	(a)	64-bit Address Flat Memory Model. Explicit Parallel Instruction Computing. Large Register Files. Automatic Register Stack Engine. Predication. Software Pipelining Support. Register Rotation. Sophisticated Branch Architecture. . The Itanium architecture is based on explicit instruction-level parallelism, in which the compiler decides which instructions to execute in parallel. This contrasts with other superscalar architectures, which depend on the processor to manage instruction dependencies at runtime.	8 Mark		15 Marks
X	(b)	i3 processor have dual core and i5 & i7 processor have quad core. i5 benefits from technology known as Turbo boost. The more no of cores, more task can be performed at same time. i3 clock speed is 3.4 GHz. i5 at 2.4 GHz and i7 at 2.7 GHz. So i3 is faster.	7	7	

CODE: 6041 VERSION: A

COURSE: ADVANCED MICROPROCESSORS

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SL.NO	Module	Type of questions							
		Part A		Part B		Part C		Total	
		No of questions	Score	No of questions	Score	No of questions	Score	No of questions	Score
1	I	1	2	2	12	2	30	5	44
2	II	1	2	2	12	2	30	5	44
3	III	1	2	2	12	2	30	5	44
4	IV	2	4	1	6	2	30	5	40
Total		5	10	7	42	8	120	20	172

QUESTION WISE ANALYSIS

COURSE: ADVANCED MICROPROCESSORS

VERSION: A

Question No	Specific outcome (as per syllabus)	Module	Content details	Score	Time in minute
I. 1	1.1.2	1	Architecture of 8086	2	2
2	2.2.6	2	Assembler Directives	2	2
3	3.2.3	3	Operating modes of Pentium	2	2
4	4.1.3	4	Limitations of single core	2	2
5	4.1.5	4	Multicore Processors	2	2
II 1	1.1.1	1	Features of 8086	6	10
2	1.1.5	1	Register set of 8086	6	10
3	2.1.4	2	Types of Interrupts	6	10
4	2.2.8	2	Assembly language programs	6	10
5	3.1.4	3	Paging mechanism in 80386	6	10
6	3.2.1	3	Features of Pentium	6	10
7	4.1.4	4	Issues In multicore processing	6	10
III a	1.1.3	1	Memory segmentation	8	16
b	1.1.4	1	Physical address generation	7	14
IV a	1.1.8	1	Maximum mode pins	10	20
b	1.1.6	1	Flag Register	5	10
V a	2.1.3	2	Interrupt vector table	8	16
b	2.1.2	2	Interrupt response	7	14
VI a	2.2.2	2	Addressing modes	10	20
b	2.2.4	2	Instruction set	5	10
VII a	3.1.1	3	Features of 80386	5	10
b	3.1.3	3	Operating modes of 80386	10	20
VIII a	3.2.2	3	Architecture of Pentium	10	20
b	3.2.4	3	Features of Pentium Pro	5	10
IX. a	4.1.1	4	Hyper Threading Technology	8	16
b	4.1.6	4	Differentiate single and multicore	7	14
X a	4.1.10	4	Features of IA processors	8	16
b	4.1.11	4	Compare i3,i5 and i7	7	14