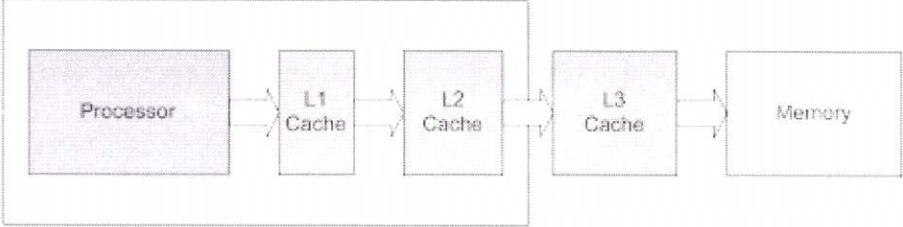
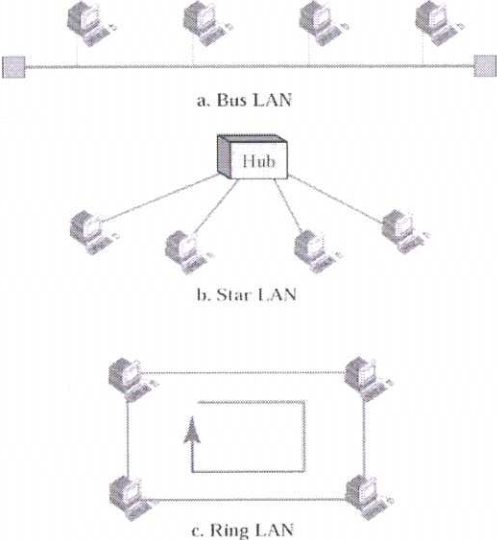


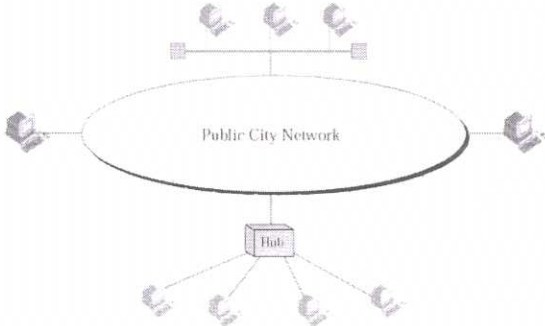
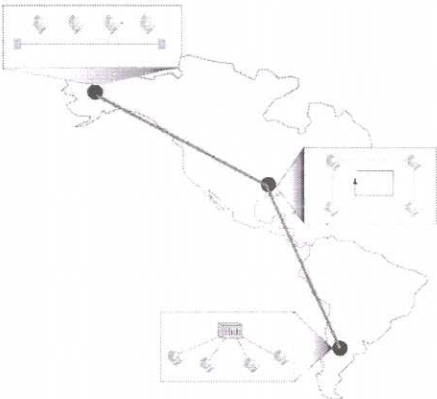
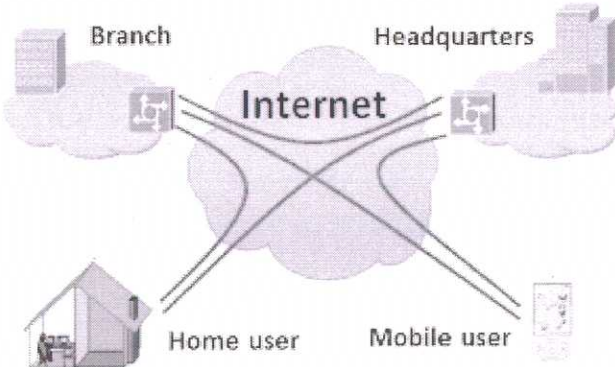
Sixth Semester Diploma Examination In Engineering / Technology  
Electronics Engineering

**COMPUTER HARDWARE AND NETWORKING**

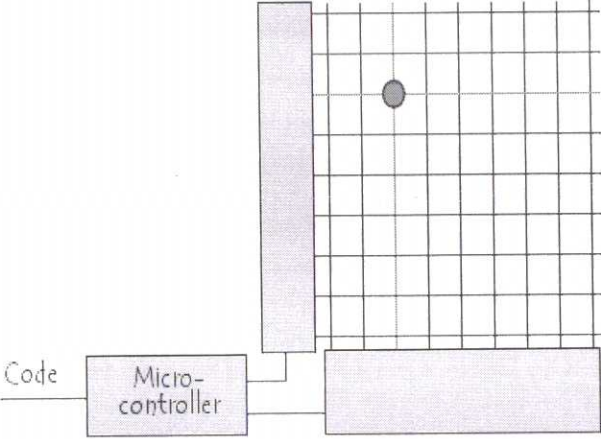
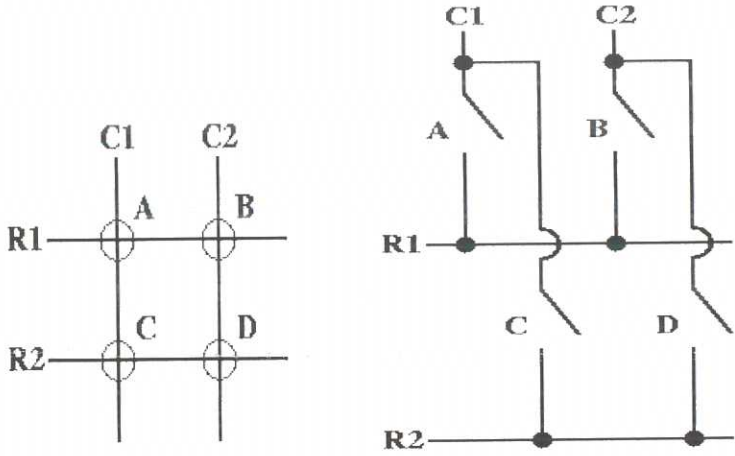
			Marks
Part - A			
I	1.	<p>ATX SMPS output voltages</p> <ul style="list-style-type: none"> <li>• +3.3V, +5V, +12V, 0V, -5V, -12V, +5V VSB, PS_ON, PW_OK and +3.3V Sense</li> </ul>	2
I	2.	<p>Impact printer</p> <ul style="list-style-type: none"> <li>• is a type of printer that works by direct contact of an ink ribbon with paper</li> <li>• eg. daisywheel printer, dot-matrix printer</li> </ul> <p>Non-impact printer</p> <ul style="list-style-type: none"> <li>• prints without banging a ribbon onto paper</li> <li>• use a some other technique to place ink or another substance on the paper</li> <li>• eg. inkjet printer, laserjet printer</li> </ul>	2  1 (explanation) + 1 (example)
I	3.	<p>Memory refresh</p> <ul style="list-style-type: none"> <li>• is most often associated with dynamic random access memory</li> <li>• a DRAM cell is a capacitor with some amount of charge on it</li> <li>• because a capacitor is leaky, it has to be refreshed by charging it to maintain the required level and store information without loss</li> </ul>	2
I	4.	<p>Electrostatic discharge (ESD)</p> <ul style="list-style-type: none"> <li>• is the sudden flow of electricity between two electrically charged objects caused by contact, electrical short or dielectric breakdown</li> <li>• occurs when differently charged objects are brought close together or when the dielectric between them breaks down, often creating a visible spark</li> </ul>	2
I	5.	<p>Hub</p> <ul style="list-style-type: none"> <li>• is a very basic network device that connects all the computers together in a network</li> <li>• sends all the network data to all the computers connected to it, without using any intelligence of its own</li> </ul>	2
Part - B			
II	1.	<p>VGA monitor</p> <p>The diagram illustrates the internal signal and power paths of a VGA monitor. On the left, a 'Min DB15 Connector' provides 'Analog Video Inputs' for HSync, VSync, Red, Green, and Blue. These signals pass through 'Horizontal Scan' and 'Vertical Scan' stages, then through 'Red Video Amp', 'Green Video Amp', and 'Blue Video Amp' respectively. The outputs of these amplifiers are connected to the 'Deflection Yoke' (indicated by a dashed box), which drives the electron gun. The 'Deflection Yoke' is also connected to an 'EHT Supply' (Electron Gun Heater) and a 'Switchmode Power Supply'. The 'Switchmode Power Supply' is connected to a '240V AC' power source.</p>	6

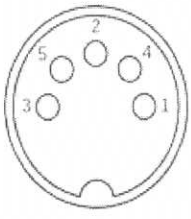
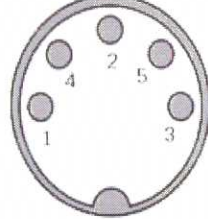
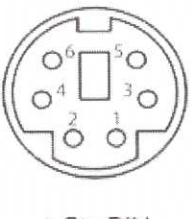
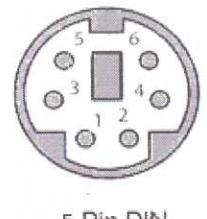
II	2.	<p>Cache memory</p> <ul style="list-style-type: none"> <li>• is high-speed static random access memory (SRAM) that a computer microprocessor can access more quickly than it can access regular random access memory (RAM)</li> <li>• is typically integrated directly into the CPU chip or placed on a separate chip that has a separate bus interconnect with the CPU</li> <li>• purpose is to store program instructions and data that are used repeatedly in the operation of programs or information that the CPU is likely to need next</li> <li>• fast access to these instructions increases the overall speed of the program</li> </ul>  <pre> graph LR     Processor[Processor] --&gt; L1[L1 Cache]     L1 --&gt; L2[L2 Cache]     L2 --&gt; L3[L3 Cache]     L3 --&gt; Memory[Memory]     </pre> <p>Classification</p> <ol style="list-style-type: none"> <li>1.Level 1 (L1) Cache - is primary cache built directly into the processor chip</li> <li>2.Level 2 (L2) Cache - is advanced transfer cache on processor chip</li> <li>3.Level 3 (L3) Cache - is separate from processor chip on the motherboard</li> </ol>	<p>6</p> <p>3 (explanation) + 3 (classification - list or figure)</p>
II	3.	<p>PROM (programmable ROM)</p> <ul style="list-style-type: none"> <li>• refers to the kind of ROM that the user can burn information into</li> <li>• for every bit of the PROM, there exists a fuse and is programmed by blowing the fuses permanently</li> <li>• is one time programmable</li> <li>• if the information burned is wrong, the PROM must be discarded</li> <li>• burning ROM, requires special equipment called a ROM burner or ROM programmer</li> </ul> <p>EPROM (erasable programmable ROM)</p> <ul style="list-style-type: none"> <li>• allows making changes in the contents of PROM after it is burned</li> <li>• can program the memory chip and erase it thousands of times</li> <li>• ultraviolet light is used to erase the content of EPROM</li> <li>• EPROM chip has to be removed from the circuit to erase and reprogram it</li> </ul> <p>EEPROM (electrically erasable programmable ROM)</p> <ul style="list-style-type: none"> <li>• can be programmed (modified) or erased while it is still in the circuit</li> <li>• uses an electric charge to erase the ones</li> <li>• method of erasure is electrical and therefore instant</li> <li>• contents can be programmed and erased while it is still in the system board</li> <li>• does not require physical removal of the memory chip from its socket</li> <li>• does not require an external erasure and programming device</li> <li>• system board must incorporate the circuitry to program the EEPROM</li> </ul>	<p>6</p> <p>2 marks each</p>
II	4.	<p>Seek Time</p> <ul style="list-style-type: none"> <li>• is the amount of time it takes for a hard drive's read / write head to move from one track to the track where the sector of the piece of data to be accessed resides on the surfaces of the platters and to reach the physical location of a piece of data</li> </ul> <p>Latency</p> <ul style="list-style-type: none"> <li>• is the average time for the sector being accessed to rotate into position under a head, after a completed seek</li> </ul>	<p>6</p> <p>3 each</p>

II	5.	<table border="1" data-bbox="387 286 1211 965"> <thead> <tr> <th>Parameters</th> <th>Blue ray</th> <th>DVD</th> <th>CD</th> </tr> </thead> <tbody> <tr> <td rowspan="2">Storage capacity</td> <td>25 GB (single-layer)</td> <td>4.7 GB (single-layer)</td> <td>700 MB (single-layer)</td> </tr> <tr> <td>50 GB (dual-layer)</td> <td>8.5 GB (dual-layer)</td> <td>-</td> </tr> <tr> <td>Track pitch</td> <td>0.32 <math>\mu\text{m}</math></td> <td>0.74 <math>\mu\text{m}</math></td> <td>1.6 <math>\mu\text{m}</math></td> </tr> <tr> <td>Laser wavelength</td> <td>405 nm (blue laser)</td> <td>650 nm (red laser)</td> <td>780 nm (infra red laser)</td> </tr> <tr> <td>Numerical aperture</td> <td>0.85</td> <td>0.6</td> <td>0.45</td> </tr> <tr> <td>Data transfer rate</td> <td>36.0 Mbps</td> <td>11.08 Mbps</td> <td>1.41 Mbps</td> </tr> <tr> <td>Protection layer</td> <td>0.1 mm</td> <td>0.6 mm</td> <td>1.2 mm</td> </tr> <tr> <td>Disc diameter</td> <td>120 mm</td> <td>120 mm</td> <td>120 mm</td> </tr> <tr> <td>Disc thickness</td> <td>1.2 mm</td> <td>1.2 mm</td> <td>1.2 mm</td> </tr> <tr> <td>Number of data layers</td> <td>One or Two</td> <td>One or Two</td> <td>One</td> </tr> </tbody> </table>	Parameters	Blue ray	DVD	CD	Storage capacity	25 GB (single-layer)	4.7 GB (single-layer)	700 MB (single-layer)	50 GB (dual-layer)	8.5 GB (dual-layer)	-	Track pitch	0.32 $\mu\text{m}$	0.74 $\mu\text{m}$	1.6 $\mu\text{m}$	Laser wavelength	405 nm (blue laser)	650 nm (red laser)	780 nm (infra red laser)	Numerical aperture	0.85	0.6	0.45	Data transfer rate	36.0 Mbps	11.08 Mbps	1.41 Mbps	Protection layer	0.1 mm	0.6 mm	1.2 mm	Disc diameter	120 mm	120 mm	120 mm	Disc thickness	1.2 mm	1.2 mm	1.2 mm	Number of data layers	One or Two	One or Two	One	6  (1 mark each - any 6)
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II	6.	<p>LAN - local area network</p> <ul style="list-style-type: none"> <li>• a group of computers that share a common connection and are usually in a small area or even in the same building</li> <li>• are usually connected by Ethernet cables and have high speed connections</li> <li>• example an office or home network</li> </ul> <div style="text-align: center;">  <p>a. Bus LAN</p> <p>b. Star LAN</p> <p>c. Ring LAN</p> </div> <p>MAN - metropolitan area network</p> <ul style="list-style-type: none"> <li>• is a larger network that connects computer users in a particular geographic area or region</li> <li>• spans a physical area larger than a LAN but smaller than a WAN</li> <li>• example a large university may have a large network</li> </ul>	6  2 each - (1 explanation, 1 figure)																																											

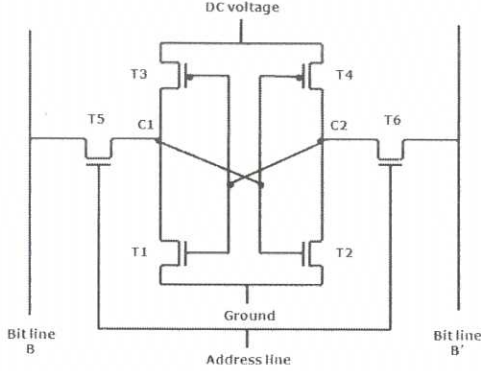
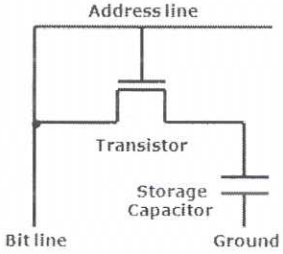
		 <p>WAN - wide area network</p> <ul style="list-style-type: none"> <li>• is the largest network and can interconnect networks throughout the world</li> <li>• is not restricted to a geographical location</li> <li>• spans a large physical distance</li> <li>• Internet is the largest WAN, spanning the Earth</li> </ul> 	
II	7.	<p>Virtual Private Network - VPN</p> <ul style="list-style-type: none"> <li>• is programming that creates a safe and encrypted connection over a less secure network, such as the public internet</li> <li>• uses "virtual" connections routed through the Internet from the private network to the remote site or users</li> <li>• works by using the shared public infrastructure while maintaining privacy through security procedures and tunneling protocols</li> <li>• ensures security - anyone intercepting the encrypted data can't read it</li> </ul> 	<p>6 3 (explanation) + 3 (figure)</p>

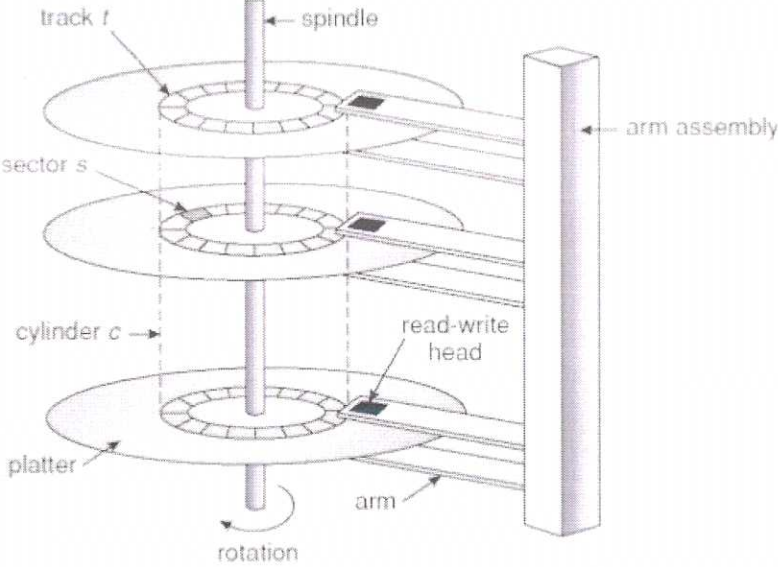
Part - C			
III	1.	<p>SMPS</p>	7
			5 (figure) + 2 (waveforms)
III	2.	<p>Flat bed scanner</p> <ul style="list-style-type: none"> <li>• has a glass window, where the object to be scanned is placed</li> <li>• has an inbuilt source of light, most commonly LED or fluorescent, to illuminate the document</li> <li>• a moving belt and motor mechanism slides the scan head, that consists of the light source and an angled mirror, across the entire surface of the entire document, ensuring a uniform exposure</li> <li>• the light shined on the document reflects back onto the angled mirror</li> <li>• then the image of the document reflects onto another fixed mirror and gets reflected again onto a lens</li> <li>• the lens then projects the captured image on to the CCD array</li> <li>• encoding takes place in the CCD array</li> <li>• detects differences in reflected light as different shades of color</li> <li>• turns shades of light reflected off the document into digital pixel information</li> <li>• gets decoded by the computer and the document is reflected on the screen, exactly the way it is</li> <li>• saved as a digital file, such as a JPG, PNG, PDF, etc.</li> </ul>	8
			4 (explanation) + 4 (figure)

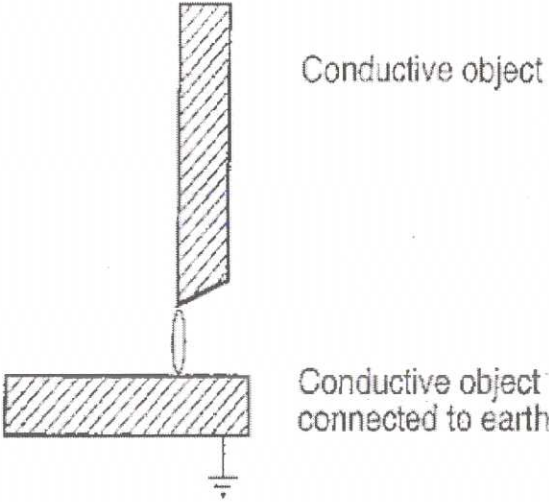
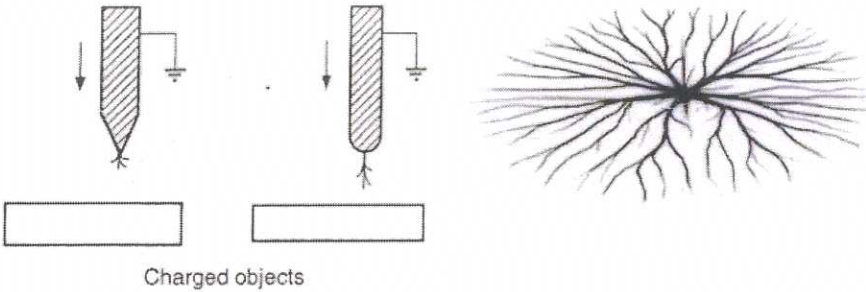
IV	I.	<p><b>Matrix Keyboard Organization</b></p> <ul style="list-style-type: none"> <li>• uses a matrix with the rows and columns made up of wires, each key acts like a switch</li> <li>• when a key is pressed, a column wire makes contact with a row wire and the circuit is completed</li> <li>• keyboard controller detects this closed circuit and registers it as a key press</li> </ul>  <ul style="list-style-type: none"> <li>• consider a keyboard having only 4 keys - A, B, C, and D</li> <li>• each key has a unique grid location - key A is at node C1R1, key B is at node C2R1, key C is at node C1R2, key D is at node C2R2</li> </ul>  <ul style="list-style-type: none"> <li>• to detect key presses, the keyboard controller will scan all columns, activating each one by one</li> <li>• when a column is activated, the controller detects which rows are "activated"</li> </ul> <ul style="list-style-type: none"> <li>• assume a single key press - the A key is pressed</li> <li>• key A corresponds to node C1R1, switch A is closed, C1R1 is activated</li> <li>• the controller activates column C1 and detects which rows are activated</li> <li>• the row R1 is activated, node C1R1 is detected</li> <li>• since C1R1 corresponds to the key 'A', the controller knows that the key 'A' is pressed</li> </ul>	<p>8</p> <p>4 (explanation) + 4 (figure)</p>
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IV	2.	<p>Keyboard connectors</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;"> <p><b>DIN Connector</b></p>  <p>5 Pin DIN Keyboard Connector Male at Keyboard side</p> </div> <div style="text-align: center;">  <p>5 Pin DIN Keyboard Connector Female at Motherboard side</p> </div> <div style="text-align: center;"> <p><b>Mini DIN Connector</b></p>  <p>5 Pin DIN Keyboard Connector Female at Motherboard side</p> </div> <div style="text-align: center;">  <p>5 Pin DIN Keyboard Connector Male at Keyboard side</p> </div> </div> <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr style="background-color: #e0e0e0;"> <th style="width: 15%;">Pin No.</th> <th style="width: 40%;">Function</th> <th style="width: 15%;">Pin No.</th> <th style="width: 30%;">Function</th> </tr> </thead> <tbody> <tr> <td>Pin 1</td> <td>Keyboard Clock</td> <td>Pin 1</td> <td>Keyboard Data</td> </tr> <tr> <td>Pin 2</td> <td>Keyboard Data</td> <td>Pin 2</td> <td>Not Connected</td> </tr> <tr> <td>Pin 3</td> <td>Reset (Not Used)</td> <td>Pin 3</td> <td>Ground</td> </tr> <tr> <td>Pin 4</td> <td>Ground</td> <td>Pin 4</td> <td>+5V Supply</td> </tr> <tr> <td>Pin 5</td> <td>+5V Supply</td> <td>Pin 5</td> <td>Keyboard Clock</td> </tr> <tr> <td></td> <td></td> <td>Pin 6</td> <td>Not Connected</td> </tr> </tbody> </table>	Pin No.	Function	Pin No.	Function	Pin 1	Keyboard Clock	Pin 1	Keyboard Data	Pin 2	Keyboard Data	Pin 2	Not Connected	Pin 3	Reset (Not Used)	Pin 3	Ground	Pin 4	Ground	Pin 4	+5V Supply	Pin 5	+5V Supply	Pin 5	Keyboard Clock			Pin 6	Not Connected	<p>7</p> <p>3 (figure) + 4 (pin details)</p>
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		Pin 6	Not Connected																												
V	1.	<p>POST (Power-on self-test).</p> <ul style="list-style-type: none"> <li>• each time the computer boots up the computer must pass the POST</li> <li>• the common steps a POST performs each time the computer starts are             <ul style="list-style-type: none"> <li>• test the power supply to ensure that it is turned on and that it releases its reset signal</li> <li>• CPU must exit the reset status mode and thereafter be able to execute instructions</li> <li>• BIOS checksum must be valid, meaning that it must be readable</li> <li>• CMOS checksum must be valid, meaning that it must be readable</li> <li>• CPU must be able to read all forms of memory such as the memory controller, memory bus, and memory module</li> <li>• the first 64 KB of memory must be operational and have the capability to be read and written to and from and capable of containing the POST code</li> <li>• I/O bus / controller must be accessible</li> <li>• I/O bus must be able to write / read from the video subsystem and be able to read all video RAM</li> </ul> </li> <li>• if the computer does not pass any of the above tests, it will receive an irregular POST</li> <li>• an irregular POST is a beep code that is different from the standard one or two beeps</li> </ul>	<p>7</p>																												

V	2.	<p><b>Chipset</b></p> <ul style="list-style-type: none"> <li>• CPU is the brain of the computer</li> <li>• but the hard-working groups of smaller chips around the CPU are important</li> <li>• this group of chips is called a chipset</li> <li>• defines the whole system because all the components, in one way or the other, rely on the capabilities of the chipset</li> <li>• is normally composed of             <ul style="list-style-type: none"> <li>• northbridge chip</li> <li>• southbridge chip</li> </ul> </li> </ul> <div data-bbox="566 627 1037 1108" style="text-align: center;"> <pre> graph TD     CPU[Central Processing Unit] --- NB[Northbridge]     NB --- SB[Southbridge]     NB --- RAM[RAM (Memory)]     NB --- AGP[AGP/PCIe (Graphics)]     SB --- ACPI[APM/ACPI (power management)]     SB --- PCI[PCI/PCIe Bus]     SB --- Audio[AC 97/HDA (audio)]     SB --- Ports[SATA/USB/LAN ports]     SB --- Other[Other devices]             </pre> </div> <p><b>North Bridge Chip</b></p> <ul style="list-style-type: none"> <li>• also called MCH - Memory Controller Hub</li> <li>• is connected directly to the CPU</li> <li>• has basically the following functions             <ol style="list-style-type: none"> <li>Memory controller</li> <li>AGP bus controller</li> <li>PCI Express x16 controller</li> <li>Interface for data transfer with south bridge</li> </ol> </li> </ul> <p><b>South Bridge Chip</b></p> <ul style="list-style-type: none"> <li>• also called ICH - I/O Controller Hub</li> <li>• is connected to the north bridge</li> <li>• is in charge basically of controlling I/O devices and on-board devices like             <ol style="list-style-type: none"> <li>Hard disk drive ports (Parallel and Serial ATA ports)</li> <li>USB ports</li> <li>On-board audio</li> <li>On-board LAN</li> <li>PCI bus</li> <li>PCI Express lanes</li> <li>Real time clock (RTC)</li> <li>CMOS memory</li> <li>Legacy devices like interrupt controller and DMA controller</li> </ol> </li> <li>• is also connected to two other chips available on the motherboard</li> <li>• the ROM chip - more known as BIOS</li> <li>• the Super I/O chip - in charge of controlling legacy devices like serial ports, parallel port and floppy disk drive</li> </ul>	<p>8</p> <p>2 (figure) + 3 + 3</p>
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<p>VI</p>	<p>1.</p>	<p>SRAM - Static Random Access Memory</p> <ul style="list-style-type: none"> <li>• is made up of CMOS technology and uses six transistors</li> <li>• construction is comprised of two cross-coupled inverters to store data (binary) similar to flip-flops</li> <li>• extra two transistors for access control</li> <li>• can hold the data as long as power is supplied to it</li> </ul>  <p>DRAM - Dynamic Random Access Memory</p> <ul style="list-style-type: none"> <li>• is a type of RAM which is constructed using capacitors and few transistors</li> <li>• capacitor is used for storing the data where bit value 1 signifies that the capacitor is charged and a bit value 0 means that capacitor is discharged</li> <li>• term dynamic indicates that the charges are continuously leaking even in the presence of continuous supplied power</li> <li>• to retain data for a long time, it needs to be repeatedly refreshed</li> </ul> 	<p>8</p> <p>4 (explanation) + 4 (figure)</p>
<p>VI</p>	<p>2.</p>	<p>Expansion card</p> <ul style="list-style-type: none"> <li>• is a PCB that fits into an expansion slot in a computer</li> <li>• is used to give computer additional capabilities, such as enhanced video performance via a graphics card, etc.</li> </ul> <p>Sound card</p> <ul style="list-style-type: none"> <li>• deals with everything to do with sounds and audio signals within the computer that are under the control of programs on the computer</li> <li>• can include allowing applications on the computer to play music, programs which edit videos or audio, presentation software, games equipment and any other type of program which plays audio</li> </ul> <p>Video card</p> <ul style="list-style-type: none"> <li>• is responsible for generating images to a visual display such as a computer monitor or laptop screen</li> <li>• a dedicated video card allows for higher quality graphics and better speeds</li> </ul>	<p>7</p> <p>1 (definition) + 3 each (any two relevant examples)</p>

	<ul style="list-style-type: none"> <li>• can offer such functions as the rendering of high-quality 3D and 2D graphics, the ability to connect to a TV and the ability to display graphics across multiple display screens</li> </ul> <p>Network card</p> <ul style="list-style-type: none"> <li>• allows a computer to connect to a computer network such as a LAN or WAN</li> <li>• almost all computers have a network interface built directly into the motherboard</li> </ul>	
VII	<p>1. Hard disks structure</p> <ul style="list-style-type: none"> <li>• use rigid platters, composed of a substrate and a magnetic medium</li> <li>• substrate is the platter's base material and must be non-magnetic and capable of being machined to a smooth finish</li> <li>• to allow data storage, both sides of each platter are coated with a magnetic material</li> <li>• stores data in magnetic patterns on each platter surface</li> <li>• inside of a hard disk drive must be kept as dust-free</li> <li>• the platters are sealed in a case with the interior kept in a partial vacuum             <ul style="list-style-type: none"> <li>• sealed chamber is often referred to as the head disk assembly (HDA)</li> </ul> </li> </ul>  <ul style="list-style-type: none"> <li>• two, three or more platters are stacked on top of each other with a common spindle</li> <li>• the whole assembly turns at several thousand revolutions per minute</li> <li>• a gap between the platters makes room for magnetic read / write head, mounted on the end of an actuator arm</li> <li>• is so close to the platters that it's only the rush of air pulled round by the rotation of the platters that keeps the head away from the surface of the disk</li> <li>• there is a read / write head for each side of each platter, mounted on arms which can move them towards the central spindle or towards the edge</li> <li>• arms are moved by the head actuator, which contains a voice-coil</li> <li>• information is recorded on the circular tracks and the track is divided into sectors</li> <li>• capacity of the hard disk depends upon the total number of usable surface, bytes stored per sector, sectors per track, tracks per surface</li> </ul>	<p>7</p> <p>4 (explanation) + 3 (figure)</p>

VII	2.	<p>Types of ESD</p> <ol style="list-style-type: none"> <li>1. Spark <ul style="list-style-type: none"> <li>• occurs when a heavy electric field creates an ionized conductive channel in air</li> <li>• can cause minor discomfort to people, severe damage to electronic equipment and fires and explosions if the air contains combustible gases or particles</li> <li>• best known example of a natural spark is lightning</li> </ul> </li> <li>2. Corona discharge <ul style="list-style-type: none"> <li>• occurs between a highly curved electrode, for example the tip of a needle or a small diameter wire, and an electrode of low curvature such as a flat plate</li> </ul> </li> </ol>  <ol style="list-style-type: none"> <li>3. Brush discharge <ul style="list-style-type: none"> <li>• occurs between an electrode with a curvature between 5 mm and 50 mm and a voltage of about 500 KV/m</li> <li>• the resulting discharge paths have the shape of a brush</li> </ul> </li> </ol> 	8  6 (explanation - 2 each) + 2 (figure)
VIII	1.	<p>FAT 32</p> <ul style="list-style-type: none"> <li>• is composed of four different sections : <ol style="list-style-type: none"> <li>1. Reserved sectors <ul style="list-style-type: none"> <li>• first reserved sector (logical sector 0) is the Boot Sector (Volume Boot Record -VBR)</li> <li>• includes an area called the BIOS Parameter Block and usually contains the operating system's boot loader code</li> </ul> </li> </ol> </li> </ul>	10  5 each (3 - explanation + 2 - figure)

2. FAT region

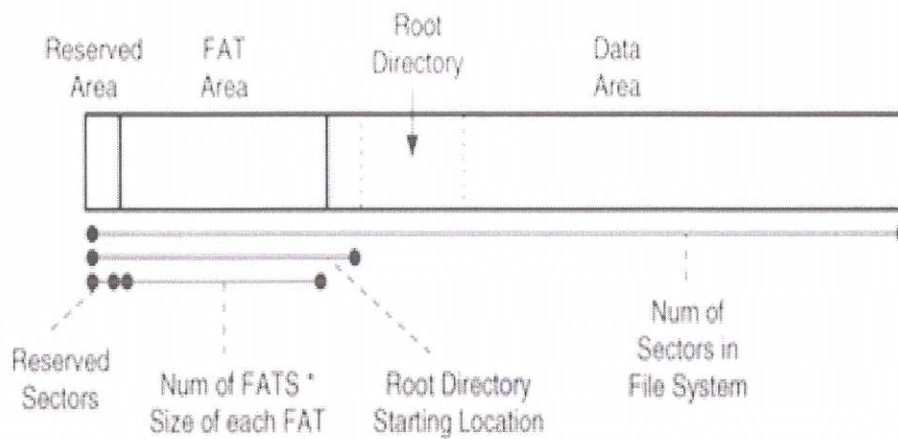
- typically contains two copies of the File Allocation Table for the sake of redundancy checking by disk repair utilities
- are maps of the Data Region, indicating which clusters are used by files and directories

3. Root directory region

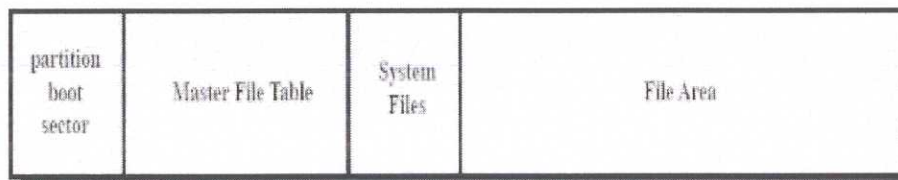
- is a Directory Table that stores information about the files and directories located in the root directory
- is in the Data Region, along with files and other directories, allowing it to grow without any a constraint

4. Data region

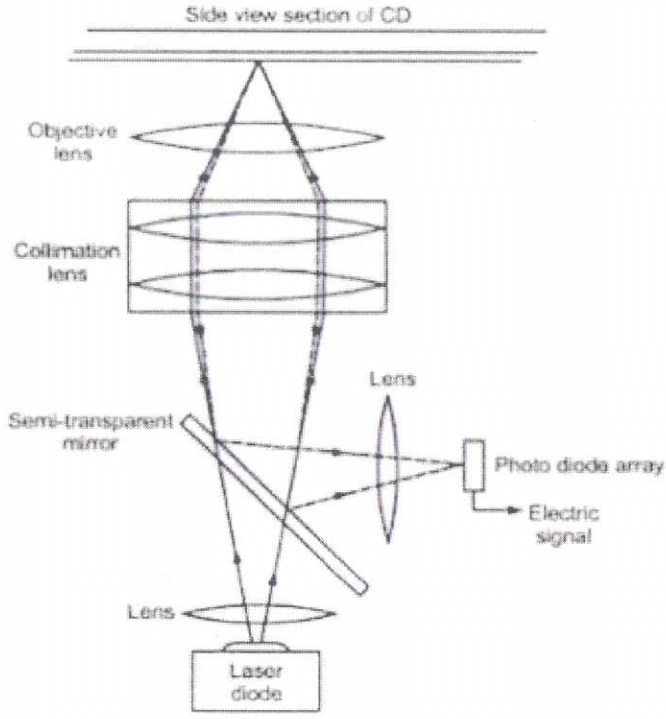
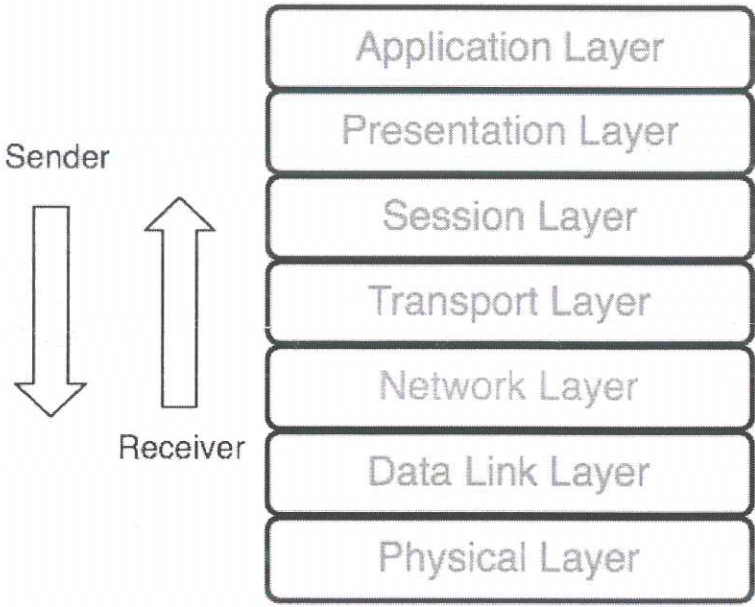
- is where the actual file and directory data is stored and takes up most of the partition



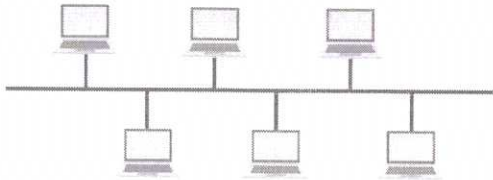
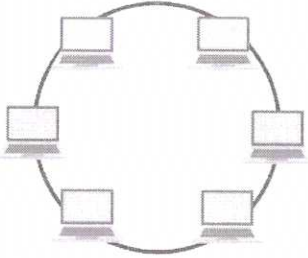
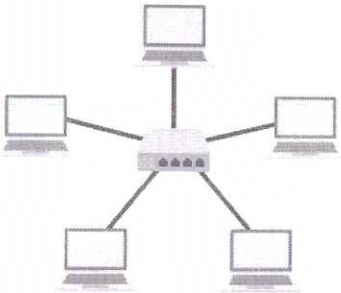
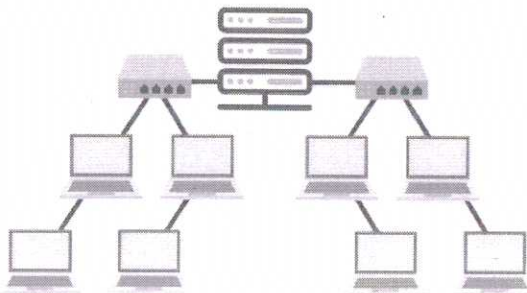
NTFS

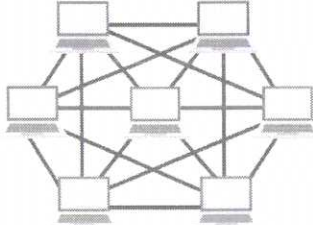
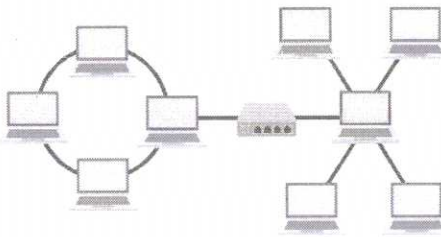
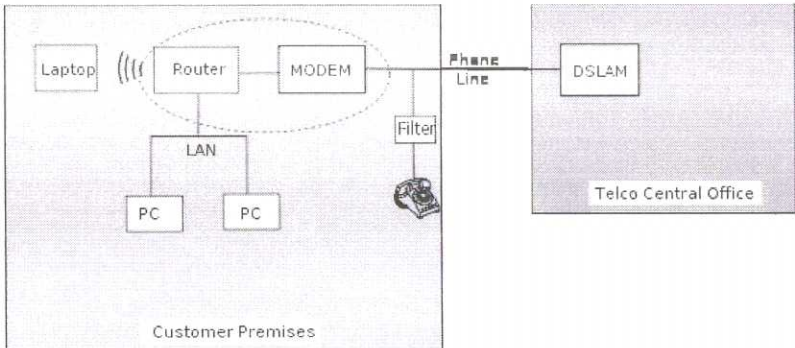


- disk is divided into two parts
  - first 12% of the disk are assigned to so-called MFT area - the space which MFT metafile grows into
  - any data recording into this area is impossible
  - the rest 88% of the disks represent usual space for files storage (File area)
- main data structure in each volume is the Master File Table or MFT
- contains a linear sequence of fixed-size 1 KB records
- each MFT record describes one file or directory that contains the file's attributes (name, timestamp, list of disk addresses where blocks are located)
- system files - a mirror of the first 16 records of the MFT, placed in the middle of the disk partition

VIII	2.	<p>Optical recording</p> 	5
IX	1.	<p>OSI reference model</p>  <p>1. Application Layer</p> <ul style="list-style-type: none"> <li>• is the layer that actually interacts with the operating system or application whenever the user chooses to transfer files, read messages or performs other network-related activities.</li> </ul>	<p>9</p> <p>2 (figure) + 7                  (1 for each layer explanation)</p>

		<p>2.Presentation Layer</p> <ul style="list-style-type: none"> <li>• converts incoming and outgoing data from one presentation format to another</li> <li>• converts data into a standard format that the other layers can understand</li> </ul> <p>3.Session Layer</p> <ul style="list-style-type: none"> <li>• sets up, coordinates and terminates conversations, exchanges and dialogs between the applications at each end</li> <li>• establishes, maintains and ends communication with the receiving device</li> </ul> <p>4.Transport Layer</p> <ul style="list-style-type: none"> <li>• ensures complete data transfer, maintains flow control of data and provides for error checking and recovery of data between the devices</li> </ul> <p>5.Network Layer</p> <ul style="list-style-type: none"> <li>• handles the routing of the data</li> <li>• sending data in the right direction to the right destination on outgoing transmissions and receiving incoming transmissions at the packet level</li> </ul> <p>6.Data Link Layer</p> <ul style="list-style-type: none"> <li>• appropriate physical protocol is assigned to the data, define type of network and the packet sequencing, furnishes transmission protocol knowledge and management</li> </ul> <p>7.Physical Layer</p> <ul style="list-style-type: none"> <li>• is the level of the actual hardware</li> <li>• defines the physical characteristics of the network such as connections, voltage levels and timing</li> </ul>	
IX	2.	<p>Infrared LANs</p> <ul style="list-style-type: none"> <li>• use very high frequencies, just below visible light in the electromagnetic spectrum, to carry data</li> <li>• an individual cell is limited to a single room, because infrared light does not penetrate opaque walls</li> <li>• three transmission techniques commonly used for IR data transmission.             <ol style="list-style-type: none"> <li>1. Directed-beam IR ( or line-of-sight) configuration - used to create point-to-point links</li> <li>2. Omni directional configuration - involves a single base station that is within line of sight of all other stations on the LAN</li> <li>3. Diffused configuration (or reflective) - IR transmitters are focused and aimed at a point on a diffusely reflecting ceiling</li> </ol> </li> </ul> <p>Narrowband microwave LANs</p> <ul style="list-style-type: none"> <li>• transmits and receives user information on a specific radio frequency</li> <li>• keeps the radio signal frequency as narrow as possible just to pass the information</li> <li>• undesirable crosstalk between communication channels is avoided by carefully co-ordinating different users on different channel frequencies</li> <li>• radio receiver filters out all radio signals except the ones on its designated frequency</li> <li>• have two bandwidths             <ol style="list-style-type: none"> <li>1. Licensed Narrowband RF - has the advantage that it guarantees interference free communication</li> <li>2. Unlicensed Narrowband RF - can be used for narrowband transmission at lower power 0.5 watts or less</li> </ol> </li> </ul>	<p>6</p> <p>3 each</p>

X	<p>1. Network topologies</p> <ul style="list-style-type: none"><li>• are categorized into the following types</li><li>1. Bus</li><li>2. Ring</li><li>3. Star</li><li>4. Tree</li><li>5. Mesh</li><li>6. Hybrid</li></ul> <p>Bus Topology</p>  <p>Ring Topology</p>  <p>Star Topology</p>  <p>Tree Topology</p> 	<p>9</p> <p>1 (list) + 8 (figure - 2 each)</p>
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		<p>Mesh Topology</p>  <p>Hybrid Topology</p> 	
X	2.	<p>Digital Subscriber Line (DSL)</p>  <ul style="list-style-type: none"> <li>• is a broadband technology that supports interactive services including internet access</li> <li>• is a technology which works with existing twisted cable technology to support high bandwidth data to subscribers</li> <li>• to provide DSL connection on existing telephone network, a network element called Digital Subscriber Line access multiplexer (DSLAM) is installed in the exchange and a modem is placed in subscriber end</li> <li>• DSLAM provides multiple DSL connection for access of available bandwidth in the network</li> <li>• connection is made between DSLAM to main distribution frame (MDF)</li> <li>• from MDF connections provided to the subscribers via twisted copper lines to splitter that sits in the customer end</li> <li>• splitter, a low pass filter removes the plain old telephone signal (POTS) from DSL signal</li> <li>• high frequency DSL signal is then given to DSL modem</li> <li>• then the signal is taken through Ethernet port to subscriber end</li> </ul>	6  3 (figure) + 3 (explanation)