

COURSE TITLE : **COMPUTER ARCHITECTURE**
COURSE CODE : **3131**
COURSE CATEGORY : **B**
PERIODS/WEEK : **4**
PERIODS/SEMESTER : **60**
CREDITS : **4**

TIME SCHEDULE

MODULE	TOPICS	PERIODS
1	Computer Function and Internal Memory	15
2	External Memory and Input/Ouptut	15
3	Processor Structure	15
4	Control Unit Organization	15

Course General Outcomes:

Sl.	G.O	On completion of this course the student will be able :
1	1	To understand Von Neumann Machine
	2	To know Computer Memory Systemmmplement Branch, Call and time delay
2	1	To understand External Memory
	2	To understand I/O Devices
3	1	To understand Processor Structure and Functions
4	1	To understand Control Unit Organization
	2	To know Parallel Processing

Specific Outcomes:

MODULE –I Computer Function and Internal Memory

- 1.1 To understand Von Neumann Machine
 - 1.1.1 To describe Von Neumann Machine
 - 1.1.2 To explain various Computer functions
 - 1.1.3 To describe Interconnection structures
 - 1.1.4 To describe Bus Interconnection
- 1.2 To know Computer Memory System
 - 1.2.1 To list Cache Memory Principles
 - 1.2.2 To explain Semiconductor Main Memory
 - 1.2.3 To List Advanced DRAM types

MODULE – II External Memory and Input/Output

- 2.1 To understand External Memory
 - 2.1.1 To Describe the organization of Magnetic Disk
 - 2.1.2 To list and describe RAID
 - 2.1.3 To explain Optical Memory
- 2.2 To understand I/O Devices
 - 2.2.1 To explain different external Devices
 - 2.2.2 To describe I/O Modules – Programmed IO, Interrupt Driven IO, DMA

MODULE – III Processor Structure

- 3.1 To understand Processor Structure and Functions
 - 3.1.1 To describe Processor organization
 - 3.1.2 To illustrate Register organization
 - 3.1.3 To explain Instruction Cycle
 - 3.1.3 To explain Instruction Pipelining

MODULE –IV Control Unit Organization

- 4.1 To understand Control Unit Organization
 - 4.1.1 To describe Micro operations
 - 4.1.2 To explain the control of the Processor
 - 4.1.3 To explain the Hardwired implementation

- 4.1.4 To describe Micro programmed control
- 4.2 To know Parallel Processing
 - 4.2.1 To explain Parallel processing
 - 4.2.2 To describe Multiple processor organization

CONTENT DETAILS

MODULE –I Computer Function and Internal Memory

The Von Neumann Machine – Computer Components - Computer functions – Instruction Fetch and Execute – Interrupts – I/O Function- Interconnection structures - Bus Interconnection – Bus Structure –Multiple Bus Hierarchies –Elements of Bus Design
Characteristics of Memory System –The Memory Hierarchy - Cache Memory Principles - Elements of Cache Design -- Semiconductor Main Memory – Organization –DRAM and SRAM –Types of ROM - Advanced DRAM types- synchronous DRAM – Rambus DRAM – DDR SDRAM – Cache DRAM

MODULE – II External Memory and Input/Output

Magnetic Disk - Magnetic Read and Write Mechanism – Data Organization and formatting – Physical Characteristics – RAID – Level 0,1,2,3,4,5,6 - Optical Memory – Compact Disk – Digital Versatile Disk – High Definition Optical Disks
External Devices – Keyboard /Monitor – Disk Drive -- I/O Modules – Module function – I/O Module Structure - Programmed IO, Interrupt Driven IO, DMA

MODULE – III Processor Structure

Processor organization - Register organization – User visible Registers – Control and Status Registers - Instruction Cycle –The Indirect Cycle – Data Flow - Instruction Pipelining

MODULE –IV Control Unit Organization

Micro operations – Fetch Cycle – Indirect Cycle - Interrupt Cycle – Execute Cycle – Instruction Cycle - Control of the Processor - Hardwired implementation - Micro programmed control
Parallel processing - Multiple processor organization

Text Book(s)

1. Computer Organization and Architecture– William Stallings Pearson Education , Eighth Edition

References:

1. Computer Organization - Carl Hamacher- Mc Graw Hill, fifth edition.
2. Computer Architecture and Organization-John Hayes- Mc Graw Hill-1998.
3. Computer System Architecture -Morris Mano- Prentice Hall of India- 2002.,

Web Site

<http://nptel.ac.in/course> :s/Webcourse-contents/IIT-%20Guwahati/comp_org_arc/web/